

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add appendix A. - rrp	98-06-09	R. MONNIN
B	Drawing updated to reflect current requirements. - rrp	05-03-14	R. MONNIN
C	Add dose rate footnote under paragraph 1.5 and Table I. Delete Accelerated aging, Neutron and Dose rate induced latchup tests. - ro	05-12-05	R. MONNIN
D	Under paragraph 1.5, delete dose rate latch up and substitute Single event latch up limit. Delete paragraph 4.4.4.2 Dose rate burnout. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. - ro	10-11-09	C. SAFFLE
E	Add device type 02 and figure A-2. Make change to paragraph 3.2.4 and delete table III. Make changes to footnote 3/ and add footnotes 4/ and 5/ as specified under paragraph 1.5. Make changes to footnotes 1/ and 2/ as specified table I. Add paragraph A.1.5. Delete device class M references. - ro	13-07-30	C. SAFFLE
F	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	19-07-09	C. SAFFLE



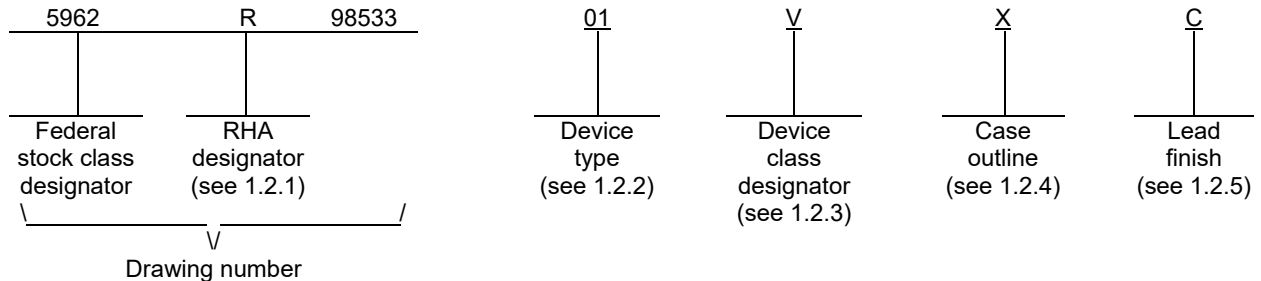
REV																				
SHEET																				
REV	F	F	F	F	F	F	F													
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REV STATUS OF SHEETS	REV			F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY RAJESH PITHADIA	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>			
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY RAJESH PITHADIA				
	APPROVED BY RAYMOND MONNIN				
	DRAWING APPROVAL DATE 98-01-06				
AMSC N/A	REVISION LEVEL F	<p>MICROCIRCUIT, LINEAR, RADIATION HARDENED, VERY LOW NOISE QUAD, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON</p> <table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-98533</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-98533
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-OP470ARH	Radiation hardened , dielectrically isolated, very low noise, quad, operational amplifier
02	HS-OP470AEH	Radiation hardened, dielectrically isolated, very low noise, quad, operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDFP3-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Voltage between V+ and V-	40 V
Differential input voltage	7 V
Voltage at either input terminal	+Vs to -Vs
Peak output current	Indefinite (one amplifier shorted to GND)
Junction temperature (T _J)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-case (θ _{JC})	30°C/W
Thermal resistance, junction-to-ambient (θ _{JA})	116°C/W

1.4 Recommended operating conditions.

Supply voltage range	±5 V to ±15 V
Input low voltage range	0 V to +0.8 V
Common-mode input voltage (V _{CMIN})	≤ 1/2 (V+ - V-)
Load resistance (R _L)	≥ 2 kΩ
Ambient operating temperature range (T _A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):	
Device type 01	100 krads(Si) <u>2/</u>
Device type 02	100 krads(Si) <u>3/</u>
Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):	
Device type 02	50 krads(Si) <u>3/</u>
Single event latch up (SEL)	No latch up <u>4/</u>

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).
- 3/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si), and condition D to a maximum total dose of 50 krads(Si).
- 4/ Devices use dielectrically isolated (DI) technology and latch up is physically not possible.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Timing diagrams. The timing diagrams shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V _{IO}	V _{CM} = 0 V, <u>3/</u> M, D, P, L, R	1, 3	01, 02	-2.1	2.1	mV
			2		-2.6	2.6	
			1		-2.6	2.6	
Input bias current	+I _{IB}	V _{CM} = 0 V, <u>3/</u> +R _S = 10 kΩ, -R _S = 100 Ω M, D, P, L, R	1	01, 02	-130	130	nA
			2		-105	105	
			3		-235	235	
			1		-630	630	
	-I _{IB}	V _{CM} = 0 V, <u>3/</u> +R _S = 100 Ω, -R _S = 10 kΩ M, D, P, L, R	1		-130	130	
			2		-105	105	
			3		-235	235	
			1		-630	630	
Input offset current	I _{IO}	V _{CM} = 0 V, <u>3/</u> +R _S = 10 kΩ, -R _S = 10 kΩ M, D, P, L, R	1	01, 02	-42	42	nA
			2		-28	28	
			3		-235	235	
			1		-630	630	
Large signal voltage gain	+A _{VOL}	V _{OUT} = 0 V and +10 V, <u>3/</u> R _L = 2 kΩ M, D, P, L, R	1	01, 02	110		kV/V
			2		150		
			3		75		
			1		40		
	-A _{VOL}	V _{OUT} = 0 V and -10 V, <u>3/</u> R _L = 2 kΩ M, D, P, L, R	1		110		
			2		150		
			3		75		
			1		40		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Common mode rejection ratio	+CMRR	V+ = 3 V, V- = -27 V, <u>3/</u> ΔVCM = +12 V, VOUT = -12 V	1, 2, 3	01, 02	80		dB	
	-CMRR	V+ = 27 V, V- = -3 V, <u>3/</u> ΔVCM = -12 V, VOUT = +12 V			80			
Output voltage swing	+VOUT	RL = 2 kΩ <u>3/</u>	1, 2, 3	01, 02	11		V	
		RL = 10 kΩ <u>3/</u>			12			
	-VOUT	RL = 2 kΩ <u>3/</u>				-11		
		RL = 10 kΩ <u>3/</u>				-12		
Output current	+IOUT	VOUT = -5 V, <u>3/</u>	1, 2, 3	01, 02	10		mA	
		M, D, P, L, R	1		8			
	-IOUT	VOUT = +5 V <u>3/</u>	1, 2, 3			-10		
		M, D, P, L, R	1			-8		
Quiescent power supply current	+ICC	IOUT = 0 mA <u>3/</u>	1, 2, 3	01, 02		5.5	mA	
	-ICC	IOUT = 0 mA <u>3/</u>	1, 2, 3		-5.5			
Power supply rejection ratio	+PSRR	ΔVSUP = 10 V, <u>3/</u> V- = -15 V, V+ = 10 V and 20 V	1, 2, 3	01, 02	80		dB	
	-PSRR	ΔVSUP = 10 V, <u>3/</u> V+ = 15 V, V- = -10 V and -20 V	1, 2, 3		80			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise and fall time	TR	VOUT = 0 V to 200 mV, <u>4/</u> 10% ≤ TR ≤ 90%, see figure 2	4, 5, 6	01, 02		200	ns
	TF	VOUT = 0 V to -200 mV, <u>4/</u> 10% ≤ TR ≤ 90%, see figure 2	4, 5, 6			200	
Settling time	TS	AVCL = -1, <u>5/ 6/ 7/</u> see figure 2	9	01, 02		6	μs
Quiescent power consumption	PC	VOUT = 0 V, <u>5/ 6/ 8/</u> IOUT = 0 mA	4, 5, 6	01, 02		165	mW
Slew rate	+SR	VOUT = -3 V to +3 V, <u>4/</u> see figure 2	4, 5	01, 02	1.7	V/μs	
			6		1.35		
			M, D, P, L, R		4		1.2
	-SR	VOUT = +3 V to -3 V, <u>4/</u> see figure 2	4, 5		1.7		
			6		1.35		
			M, D, P, L, R		4		1.2
Overshoot	+OS	VOUT = 0 V to 200 mV, <u>4/</u> see figure 2	4	01, 02	45	%	
			5, 6		50		
	-OS		4		45		
			5, 6		50		
Differential input resistance	RIN	VCM = 0 V <u>5/ 6/</u>	4	01, 02	250	kΩ	
Input noise voltage density	EN	RS = 20 Ω, <u>5/ 6/</u> fo = 1000 Hz	4	01, 02	6	nV / √Hz	
Input noise current density	IN	RS = 2 MΩ, <u>5/ 6/</u> fo = 1000 Hz	4	01, 02	3	pA / √Hz	
Full power bandwidth	FPBW	VPK = 10 V <u>5/ 6/ 9/</u>	4	01, 02	32	kHz	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Minimum closed loop stable gain	CLSG	RL = 2 kΩ, <u>5/ 6/</u> CL = 50 pF	4, 5, 6	01, 02	1		V/V
Output resistance	ROUT	Open loop <u>5/ 6/</u>	4	01, 02		150	Ω
Channel separation	CS	RS = 1 kΩ, <u>5/ 6/</u> AVCL = 100 V/V, VIN = 100 mV RMS at 10 kHz, referenced to input	4	01, 02	90		dB

1/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation for condition A and levels M, D, P, and L for condition D. However, device type 02 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.

2/ RHA device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

3/ Unless otherwise specified, device tested at: supply voltage = ±15 V, source resistance (RS) = 100 Ω, load resistance (RL) = 100 kΩ, VOUT = 0 V.

4/ Unless otherwise specified, device tested at: supply voltage = ±15 V, source resistance (RS) = 50 Ω, load resistance (RL) = 2 kΩ, load capacitance (CL) = 50 pF, AVCL = 1 V/V.

5/ Unless otherwise specified, device tested at: supply voltage = ±15 V, load resistance (RL) = 2 kΩ, load capacitance (CL) = 50 pF, AVCL = 1 V/V.

6/ If not tested, shall be guaranteed to the limits specified in table I herein.

7/ Settling time measured from the 90% point of a 10 V input pulse to within 10 mV of the settled value.

8/ Quiescent power consumption based upon quiescent supply current test maximum. No load on outputs.

9/ Full power bandwidth guarantee based on slew rate measurement using FPBW = slew rate / (2πV_{PK}).

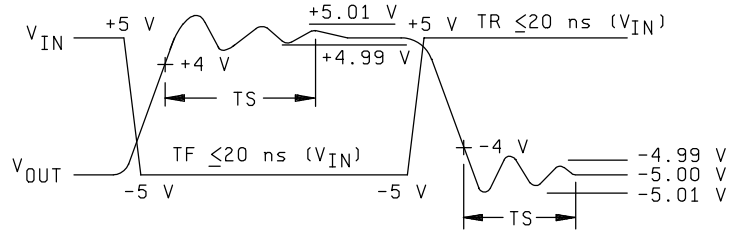
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Device types	01 and 02
Case outline	X
Terminal number	Terminal symbol
1	OUT 1
2	-IN 1
3	+IN 1
4	V+
5	+IN 2
6	-IN 2
7	OUT 2
8	OUT 3
9	-IN 3
10	+IN 3
11	V-
12	+IN 4
13	-IN 4
14	OUT 4

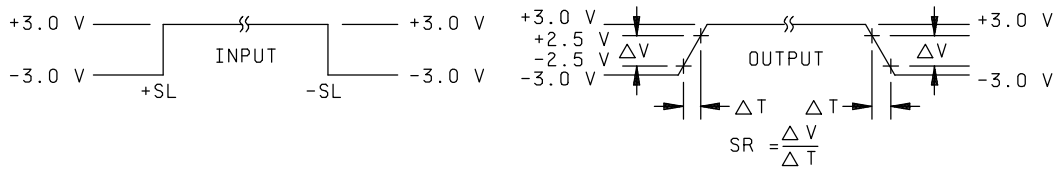
FIGURE 1. Terminal connections.

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SETTLING TIME WAVEFORM



SLEW RATE WAVEFORMS



OVERSHOOT, RISE AND FALL TIME

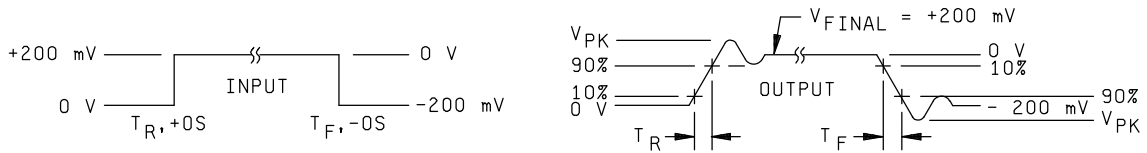


FIGURE 2. Timing diagrams.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4	1, 4
Final electrical parameters (see 4.2)	1,2,3,4, <u>1/</u> 5,6,9	1,2,3, <u>1/ 2/</u> 4,5,6,9
Group A test requirements (see 4.4)	1,2,3,4,5,6,9	1,2,3,4,5,6,9
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6,9	1,2,3,4,5, <u>2/</u> 6,9
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	1, 4	1, 4

- 1/ PDA applies to subgroup 1. For class V to subgroups 1 and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. (TA = +25°C)

Parameters	Symbol	Delta limits
Input offset voltage	V _{IO}	±2 mV
Input bias current	+I _{IB} / -I _{IB}	±75 nA
Input offset current	I _{IO}	±75 nA

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01 and 02. In addition, for device type 02 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

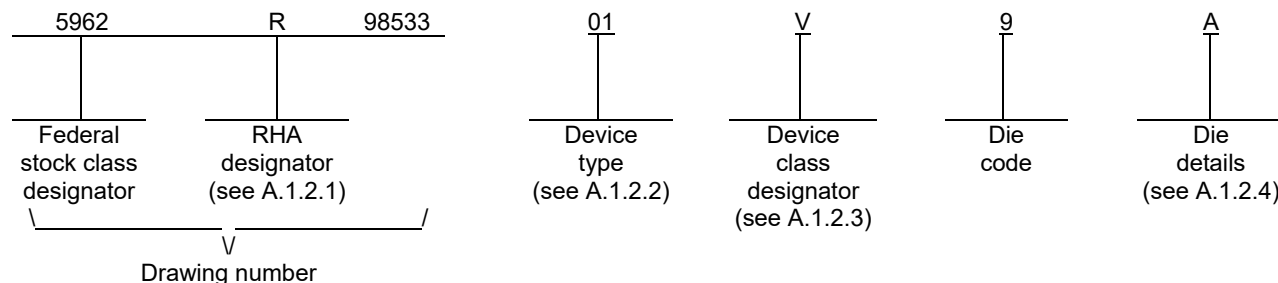
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-OP470ARH	Radiation hardened, dielectrically isolated, very low noise, quad, operational amplifier
02	HS-OP470AEH	Radiation hardened, dielectrically isolated, very low noise, quad, operational amplifier

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02	A-2

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02	A-2

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 and 4.4.4.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

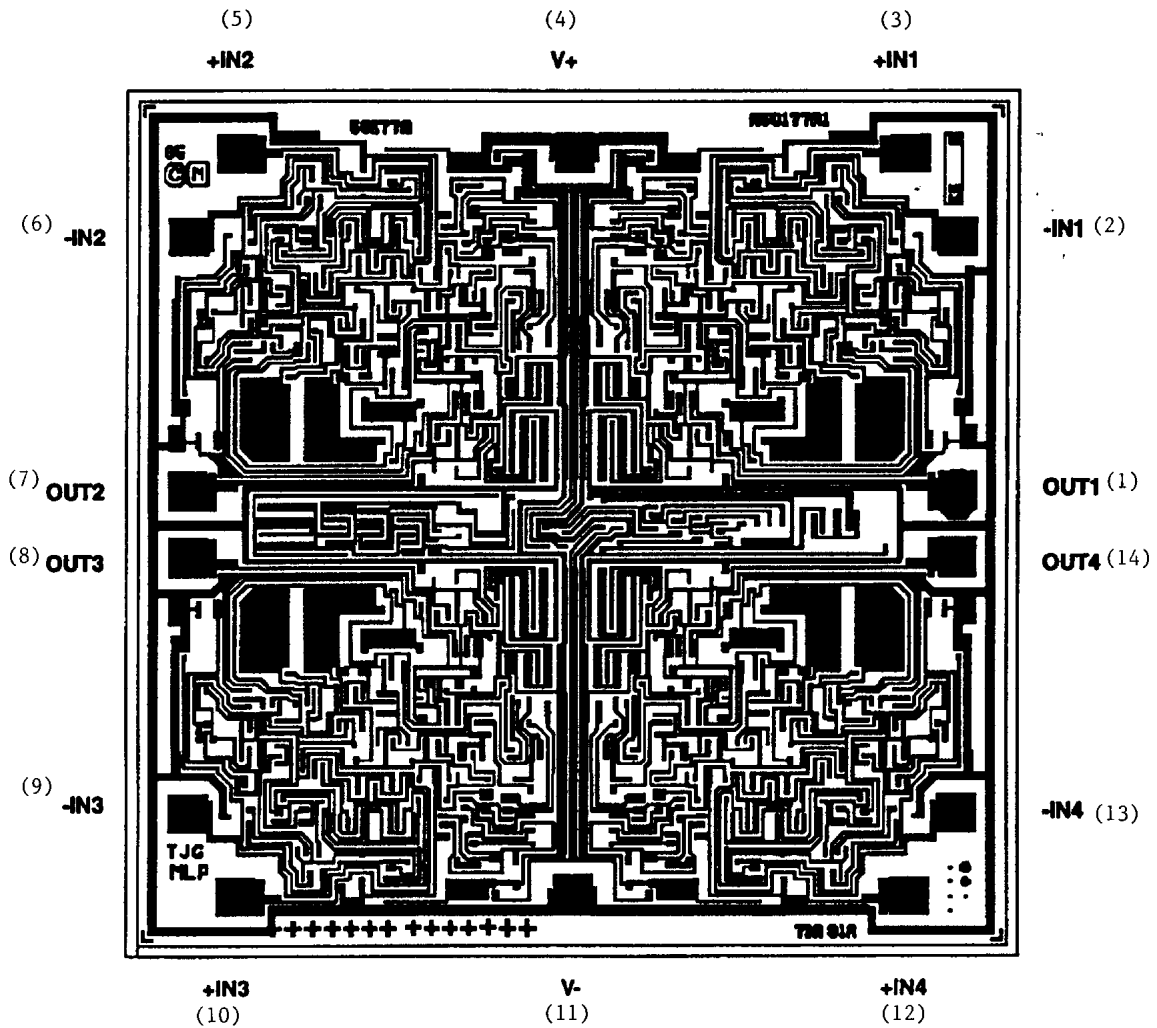
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see Figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

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Die physical dimensions.

Die size: 2420 μm x 2530 μm

Die thickness: 483 μm \pm 25.4 μm

Interface materials.

Top metallization: AlCu

Thickness: 16.0 $\text{k}\text{\AA}$ \pm 2 $\text{k}\text{\AA}$

Backside metallization: None.

Glassivation.

Type: Nitride over Silox (SiO_2 , 5% Phos)

Thickness: Silox: 12 $\text{k}\text{\AA}$ \pm 2.0 $\text{k}\text{\AA}$

Nitride: 3.5 $\text{k}\text{\AA}$ \pm 1.5 $\text{k}\text{\AA}$

Substrate: Dielectric Isolation (DI) Silicon

Assembly related information.

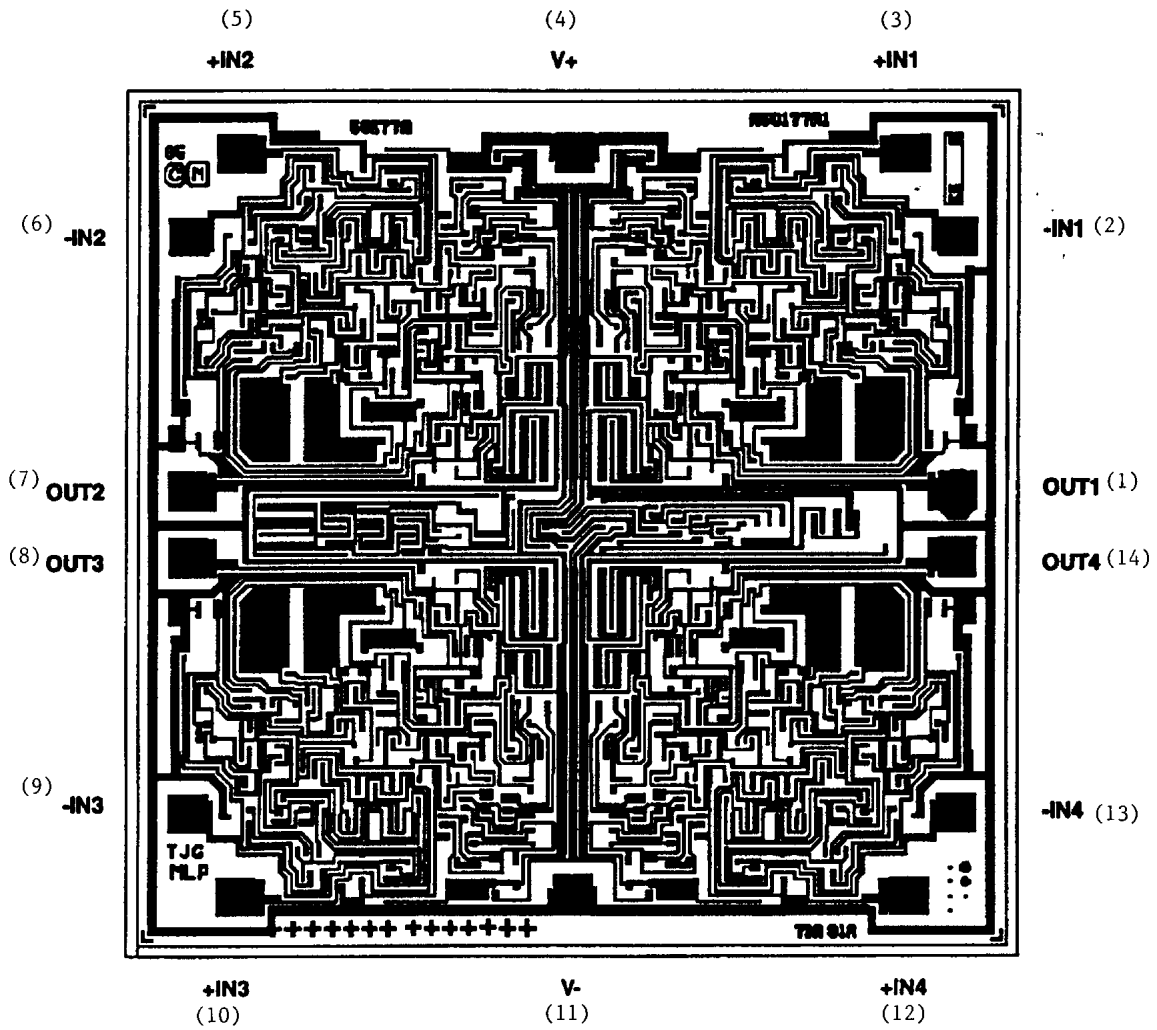
Substrate potential: Unbiased

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

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NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see Figure 1).

FIGURE A-2. Die bonding pad locations and electrical functions.

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Die physical dimensions.

Die size: 2420 microns x 2530 microns
Die thickness: 483 $\mu\text{m} \pm 25.4 \mu\text{m}$

Interface materials.

Top metallization: Al/Cu 16.0 kÅ ± 2 kÅ
Backside metallization: None

Glassivation.

Type: Silox (SiO₂) 1:6:1
Thickness: 8 kÅ ± 0.8 kÅ (1 kÅ undoped, 6 kÅ doped, cap 1 kÅ undoped)

Substrate: Dielectrically Isolated (DI)

Assembly related information.

Substrate potential: Unbiased
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-09

Approved sources of supply for SMD 5962-98533 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9853301QXC	<u>3/</u>	HS9-OP470ARH-8
5962R9853301VXC	<u>3/</u>	HS9-OP470ARH-Q
5962R9853301V9A	<u>3/</u>	HS0-OP470ARH-Q
5962R9853302VXC	34371	HS9-OP470AEH-Q
5962R9853302V9A	34371	HS0-OP470AEH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

Vendor name and address

34371

Renesas Electronics America, Inc.
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.