

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Appendix A for microcircuit die. - ro	98-05-29	R. MONNIN
B	Make changes to boilerplate to add class T devices. - ro	98-12-03	R. MONNIN
C	Make changes to AE and BPOE delta limits as specified in table IIB. - ro	02-01-08	R. MONNIN
D	Add device type 02. - ro	02-12-19	R. MONNIN
E	Make corrections to U _{tempo} , B _{tempo} , and G _{tempo} tests unit column as specified under Table I. Delete I/O from Table IIB. Add a new footnote under 1.5 and Table I. Delete latch up under 1.5 and 4.4.4.2. - ro	05-04-25	R. MONNIN
F	Add device type 03. Delete dose rate burnout paragraph. Make changes to paragraphs 1.2.2, 1.5, 4.4.4.1, A.1.2.2, A.1.2.4, Table I, and figure 1. Add paragraph A.1.5. - ro	12-03-15	C. SAFFLE
G	Delete Table III and make changes to paragraph 3.2.4. Delete references to device class M requirements. Update document paragraphs to current MIL-PRF-38535 requirements. - ro	17-07-06	C. SAFFLE



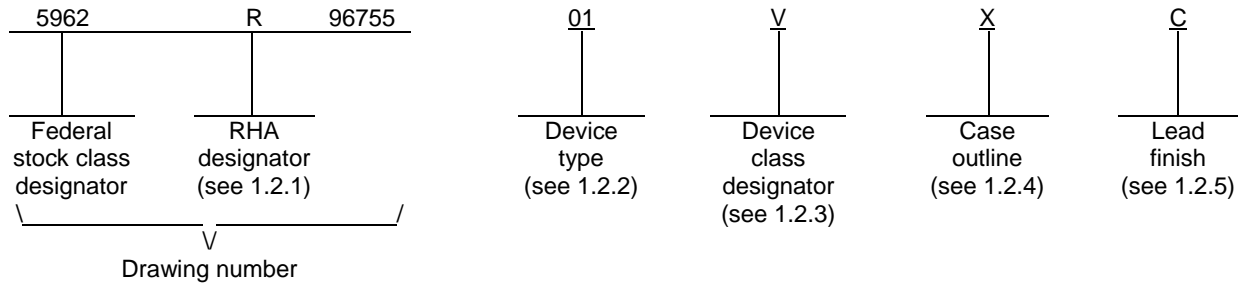
REV																				
SHEET																				
REV	G	G	G	G	G	G	G													
SHEET	15	16	17	18	19	20	21													
REV STATUS OF SHEETS	REV			SHEET			G	G	G	G	G	G	G	G	G	G	G	G	G	
							1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY DAN WONNELL	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY SANDRA ROONEY																		
	APPROVED BY MICHAEL A. FRYE	<p align="center">MICROCIRCUIT, DIGITAL-LINEAR, RADIATION HARDENED, HIGH SPEED, 12-BIT D/A CONVERTER, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 96-02-05																		
	REVISION LEVEL G		SIZE A	CAGE CODE 67268	5962-96755														
		SHEET 1 OF 21																	

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-565ARH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output
02	HS-565BRH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output
03	HS-565BEH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
J	CDIP2-T24	24	Dual-in-line
X	CDFP4-F24	24	Flat pack

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/

VCC to power ground	0 V to +18 V
VEE to power ground	0 V to -18 V
Voltage on DAC output on IDAC pin	-3 V to +12 V
Digital input (BIT 12 IN – BIT 1 IN pins) to power ground	-1 V to +7 V
REF IN to REF GND	±12 V
Bipolar offset to REF GND	±12 V
10 V SPAN R to REF GND	±12 V
20 V SPAN R to REF GND	±24 V
Maximum package power dissipation (TA = +125°C): 2/	
Case outline J	0.83 W
Case outline X	0.62 W
Junction temperature (TJ)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θJC):	
Case outline J	17°C/W
Case outline X	15°C/W
Thermal resistance, junction-to-ambient (θJA):	
Case outline J	60°C/W
Case outline X	80°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (VCC)	+11.4 V to +16.5 V
Negative supply voltage range (VEE)	-11.4 V to -16.5 V
Digital input low voltage range	0 V to +0.8 V
Digital input high voltage range	+2.0 V to +5.5 V
Ambient operating temperature range (TA)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ If the power exceeds package dissipation capability, provide heat sinking or derate linearity at the following rate (the derating is based on θJA): case outline J use 16.67 mW/°C and case outline X use 12.5 mW/°C.

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1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 Rads(Si)/s):	
Device types 01 and 02	100K Rads(Si) <u>3/</u>
Device type 03	100K Rads(Si) <u>4/</u>
Maximum total dose available (dose rate ≤ 0.01 Rads(Si)/s):	
Device type 03	50K Rads(Si) <u>4/</u>

The manufacturer supplying RHA device types 01, 02, and 03 on this drawing has performed characterization testing to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1. Therefore these parts may be considered ELDRS free at a level of 50K Rads(Si). The manufacturer will perform only high dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, condition A for device types 01 and 02. The manufacturer will perform high dose rate and low dose rate lot acceptance testing on a wafer by wafer basis in accordance with MIL-STD-883, method 1019, conditions A and D for device type 03.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3/ The manufacturer supplying device types 01 and 02 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a level of 50K Rads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100K Rads(Si).

4/ The manufacturer supplying device type 03 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a level of 50K Rads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100K Rads(Si), and condition D to a maximum total dose of 50K Rads(Si).

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Calibration diagrams. The calibration diagrams shall be as specified on figures 2, 3, and 4.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C VCC = +15 V, VEE = -15 V VSSD = VSSA = 0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution			1,2,3	All		12	Bits
Accuracy	ILE	Error relative to full scale	1,2,3	All		±0.75	LSB
			M,D,P,L,R	1	All		
Digital input high current	I _{IH}	V _{IN} = 5.5 V	1,2,3	All		+1.0	μA
Digital input low current	I _{IL}	V _{IN} = 0 V	1,2,3	All	-20		μA
			M,D,P,L,R	1	All	-40	
Digital input high voltage	V _{IH}	<u>2/</u>	1,2,3	All	2.0		V
			M,D,P,L,R	1	All	2.5	
Digital input low voltage	V _{IL}	<u>2/</u>	1,2,3	All		0.8	V
			M,D,P,L,R	1	All		
Differential nonlinearity	DLE	Monotonicity guaranteed	1,2,3	All		±0.50	LSB
			M,D,P,L,R	1	All		
Positive supply current	I _{CC}		1,2,3	All		+11.8	mA
Negative supply current	I _{EE}		1,2,3	All	-14.5		mA
Reference output voltage	REF OUT		1,2,3	All	9.9	10.1	V
Reference output current	I _{REF}	Available for external loads	1,2,3	All	1.5		mA
Output current unipolar	I _{OUT1}	All bits on	1,2,3	All	-1.6	-2.4	mA
Output current bipolar	I _{OUT2}	All bits on or off	1,2,3	All	±0.8	±1.2	mA
Output offset error unipolar	V _{OS}	R ₂ = 50 Ω fixed, see figure 2	1,2,3	All		±0.05	% of F.S.
Output offset error bipolar	BPOE	R ₃ , R ₄ = 50 Ω fixed, see figure 3	1,2,3	01		±0.15	% of F.S.
			1	02, 03		±0.15	
			2,3			±0.18	
			M,D,P,L,R	1	All		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C VCC = +15 V, VEE = -15 V VSSD = VSSA = 0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply gain <u>3/</u> sensitivity	+PSS		1,2,3	All		10	ppm of FS %ΔVCC
	-PSS					25	ppm of FS %ΔVEE
Temperature coefficient <u>4/</u> unipolar zero	Utempo	With internal reference	1,2,3	All		2	ppm of FSR / °C
Temperature coefficient <u>4/</u> bipolar zero	Btempo	With internal reference	1,2,3	All		20	ppm of FSR / °C
Temperature coefficient <u>4/</u> gain (full scale)	Gtempo	With internal reference	1,2,3	All		50	ppm of FSR / °C
Full scale error unipolar	AE	R2 = 50 Ω fixed, see figure 2	1,2,3	01		±0.25	% of F.S.
			1	02, 03		±0.25	
			2,3			±0.4	
			M,D,P,L,R	All		±0.85	
Full scale error bipolar	BPAE	R3, R4 = 50 Ω fixed, see figure 3	1,2,3	01		±0.25	% of F.S.
			1	02, 03		±0.25	
			2,3			±0.4	
			M,D,P,L,R	All		±0.85	
Zero error bipolar	BPZE	R3, R4 = 50 Ω fixed, see figure 3	1,2,3	01		±0.10	% of F.S.
			1	02, 03		±0.10	
			2,3			±0.18	
			M,D,P,L,R	All		±0.25	
Output compliance voltage	VOC	<u>5/</u>	1,2,3	All	-1.5	10	V
Programmable output voltage range	VOR	See figures 2, 3, and 4 <u>5/</u>	1,2,3	All	0	5	V
					-2.5	2.5	
					0	10	
					-5	5	
					-10	10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C VCC = +15 V, VEE = -15 V VSSD = VSSA = 0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain adjustment range	GADJ	<u>5/</u>	1,2,3	All	±0.25		% of F.S.
Bipolar zero adjustment range	BZADJ	<u>5/</u>	1,2,3	All	±0.15		% of F.S.
Reference input impedance	RREF	<u>5/</u>	1,2,3	All	15	25	kΩ
Output resistance	ROUT	Exclusive of span <u>5/</u> resistors	1,2,3	All	1.8	3.2	kΩ
Settling time	TS1	High Z external load <u>5/</u>	9,10,11	All		500	ns
	TS2	75 Ω external load <u>5/</u>				250	
Full scale transition rise time	tR	<u>5/</u>	9,10,11	All		30	ns
Full scale transition fall time	tF	<u>5/</u>	9,10,11	All		60	ns

1/ RHA device types 01 and 02 supplied to this drawing meet all levels M, D, P, L, and R irradiation for condition A. However, device types 01 and 02 are only tested at the "R" level in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device type 03 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation for condition A and levels M, D, P, and L for condition D. However, device type 03 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.

2/ This parameter is an applied condition of test.

3/ PSS is tested in reference to a VCC = +15 V and VEE = -15 V.

4/ Test shall be performed only at final electrical test.

5/ These tests are controlled via design and are not directly tested. These parameters are characterized on initial design release and upon design changes which affect these characteristics.

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Device types	01, 02, 03
Case outlines	J and X
Terminal number	Terminal symbol
1	NC
2	NC
3	VCC
4	REF OUT
5	REF GND
6	REF IN
7	-VEE
8	BIPOLAR RIN
9	IDAC OUT
10	10 V SPAN
11	20 V SPAN
12	PWR GND
13	BIT 12 IN (LSB)
14	BIT 11 IN
15	BIT 10 IN
16	BIT 9 IN
17	BIT 8 IN
18	BIT 7 IN
19	BIT 6 IN
20	BIT 5 IN
21	BIT 4 IN
22	BIT 3 IN
23	BIT 2 IN
24	BIT 1 IN (MSB)

FIGURE 1. Terminal connections.

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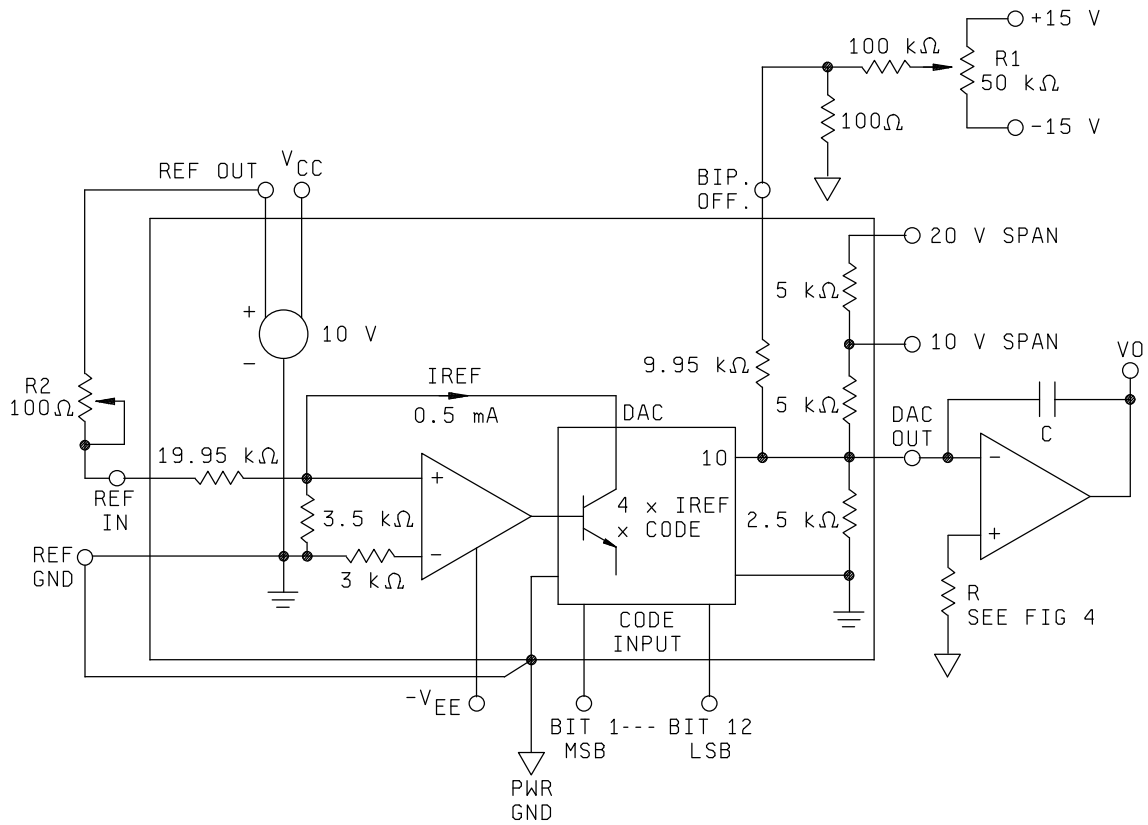


FIGURE 2. Calibration circuit, unipolar voltage output.

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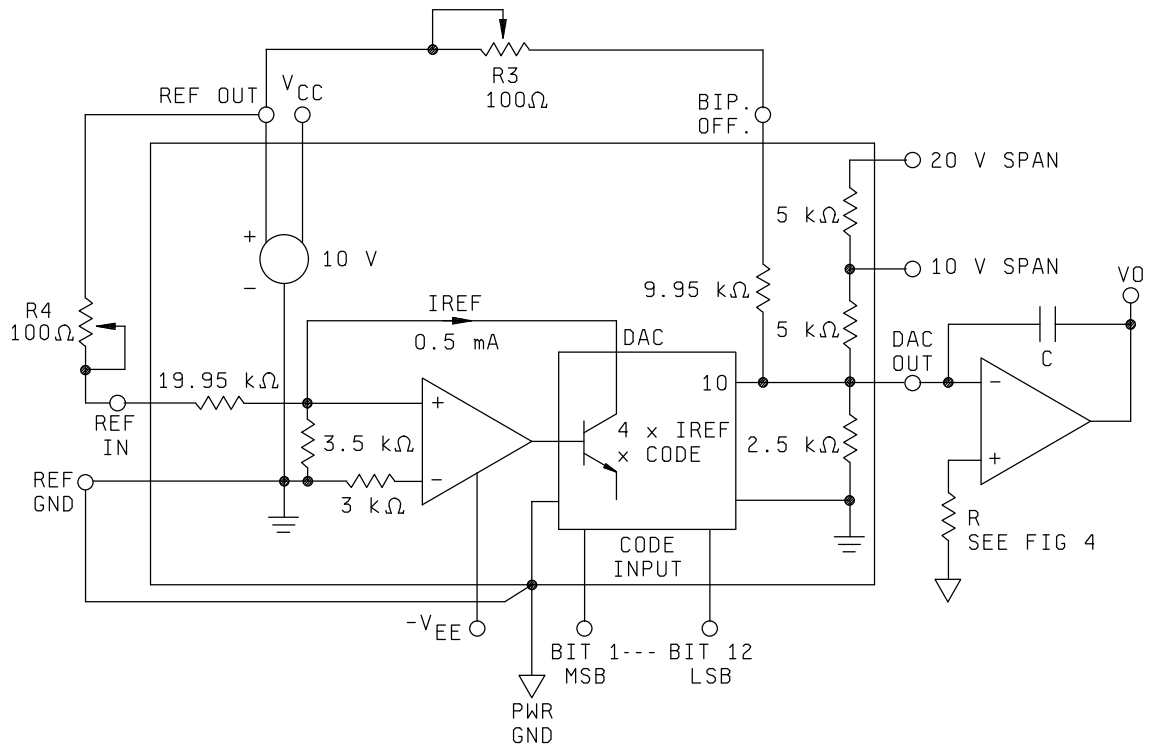


FIGURE 3. Calibration circuit, bipolar voltage output.

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Model	Circuit connections				Calibration		
	Output range	10 V SPAN pin to	20 V SPAN pin to	Resistor (R)	Apply input code	Adjust	To set VO
Unipolar (see figure 2)	0 V to +10 V	VO	10 V SPAN pin	1.43 k Ω	All 0's All 1's	R1 R2	0 V +9.99756 V
	0 V to +5 V	VO	IDAC OUT pin	1.1 k Ω	All 0's All 1's	R1 R2	0 V +4.99878 V
Bipolar (see figure 3)	± 10 V	NC	VO	1.69 k Ω	All 0's All 1's	R3 R4	-10 V +9.99512 V
	± 5 V	VO	10 V SPAN pin	1.43 k Ω	All 0's All 1's	R3 R4	-5 V +4.99756 V
	± 2.5 V	VO	IDAC OUT pin	1.1 k Ω	All 0's All 1's	R3 R4	-2.5 V +2.49878 V

FIGURE 4. Operations modes and calibration.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1	1	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3 <u>1/ 2/</u>	1,2,3 <u>1/ 2/ 3/</u>	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,9, <u>4/</u> 10,11	1,2,3,9, <u>4/</u> 10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1	1	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1	1	As specified in QM plan

1/ PDA applies to subgroup 1. For class V to subgroups 1 and Δ.

2/ Temperature coefficient parameters only tested at final electrical test.

3/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table I).

4/ Subgroups 9, 10, and 11 are guaranteed to the limits in table I if not tested.

TABLE IIB. Post burn-in delta parameters. TA = +25°C.

Parameters	Symbol	Delta limits
Positive supply current	ICC	±1.18 mA
Negative supply current	IEE	±1.45 mA
Output current unipolar	IOUT1	±240 μA
Output current bipolar	IOUT2	±240 μA
Output offset error unipolar	VOS	±0.02 %
Full scale error unipolar	AE	±0.25 %
Output offset error bipolar	BPOE	±0.13%
Zero error bipolar	BPZE	±0.10 %
Digital input low current	IIL	±1.0 μA
Digital input high current	IiH	±40 nA

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing high dose rate shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, and 03. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein for device type 03.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K Rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

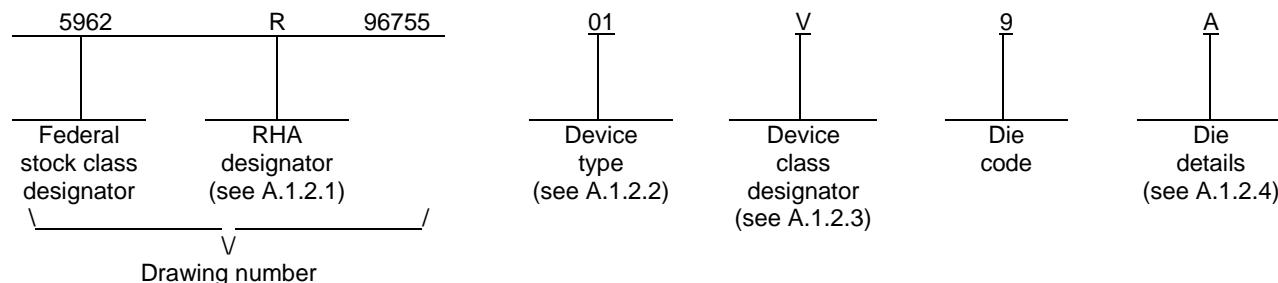
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-565ARH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output
02	HS-565BRH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output
03	HS-565BEH	Radiation hardened, dielectrically isolated, high speed, 12-bit, digital-to-analog converter, with current output

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01, 02, 03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01, 02, 03	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01, 02, 03	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01, 02, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, and 4.4.4.2.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

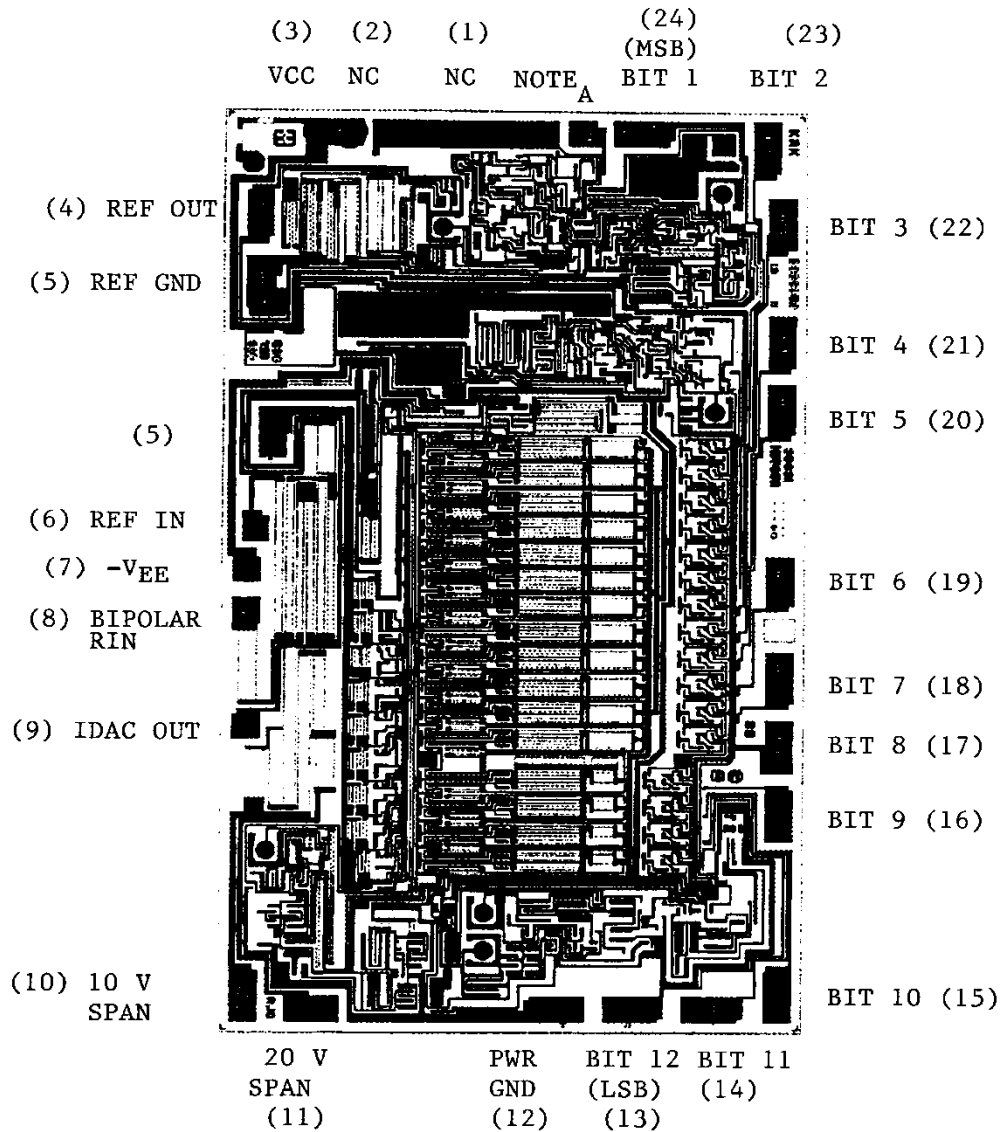
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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Note: Pad numbers reflect terminal numbers when placed in case outlines J and X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

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Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 4600 microns x 2750 microns
Die thickness: 19 ± 1 mils

Interface materials.

Top metallization: Al/Cu 16.0 kÅ ± 2 kÅ
Backside metallization: None

Glassivation.

Type: SiO₂
Thickness: 8 kÅ ± 1.0 kÅ

Substrate: Dielectrically isolated (DI)

Assembly related information.

Substrate potential: Insulator
Special assembly instructions: Pin number 5 is connected to two bonding pads.
Note A refers to pin A which is connected to die attach pad.

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-07-06

Approved sources of supply for SMD 5962-96755 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9675501VJC	<u>3/</u>	HS1-565ARH-Q
5962R9675501VXC	<u>3/</u>	HS9-565ARH-Q
5962R9675501V9A	<u>3/</u>	HS0-565ARH-Q
5962R9675501TJC	<u>3/</u>	HS1-565ARH-T
5962R9675501TXC	<u>3/</u>	HS9-565ARH-T
5962R9675502VJC	34371	HS1-565BRH-Q
5962R9675502VXC	34371	HS9-565BRH-Q
5962R9675502V9A	34371	HS0-565BRH-Q
5962R9675503VJC	34371	HS1-565BEH-Q
5962R9675503VXC	34371	HS9-565BEH-Q
5962R9675503V9A	34371	HS0-565BEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

34371

Vendor name
and address

Intersil Corporation
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.