REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R199-97.	97-02-28	Monica L. Poelking
B	Changes in accordance with NOR 5962-R426-97.	97-08-08	Raymond Monnin
C	Incorporate revisions A and B. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	03-07-02	Thomas M. Hess
D	Update radiation features in section 1.5 and paragraphs 4.4.4.1 – 4.4.4.5. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	10-06-23	Thomas M. Hess
E	Update boilerplate paragraphs to MIL-PRF-38535 requirements throughout. Deleted class M requirements throughout. Update device suppliers information – RDC	20-01-31	Muhammad A. Akbar

REV																				
SHEET																				
REV	E	E	E	E	E	E	E													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Larry T. Gauder

CHECKED BY
Monica L. Poelking

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
95-12-07

REVISION LEVEL
E

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, RADIATION HARDENED CMOS, QUAD EXCLUSIVE OR GATE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96646**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

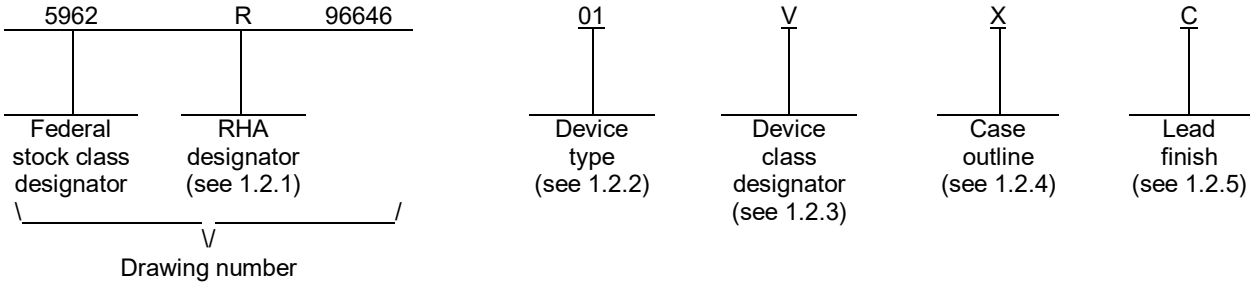
5962-E458-19

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4030B	Radiation hardened CMOS, quad exclusive OR gate
02	4030BN	Radiation hardened CMOS, quad exclusive OR gate with neutron irradiated die

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	CDIP2-T14	14	Dual-in-line
X	CDFP3-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.5 V dc to +20 V dc
Input voltage range	-0.5 V dc to V_{DD} + 0.5 V dc
DC input current, any one input	±10 mA
Device dissipation per output transistor	100 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case C	24°C/W
Case X	30°C/W
Thermal resistance, junction-to-ambient θ_{JA}):	
Case C	74°C/W
Case X	116°C/W
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D) at T_A = +125°C: 4/	
Case C	0.68 W
Case X	0.43 W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	3.0 V dc to +18 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage (V_{IN})	0 V to V_{DD}
Output voltage (V_{OUT})	0 V to V_{DD}

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad (Si)/s)	= 100 krads(Si)
Single event phenomenon (SEP):	
No SEU occurs at effective LET (see 4.4.4.4)	≤ 75 MeV/(mg/cm^2) 5/
No SEL occurs at effective LET (see 4.4.4.4)	≤ 75 MeV/(mg/cm^2) 5/
Dose rate induced upset (20 ns pulse)	= 5 x 10^8 rads (Si)/s 5/
Dose rate induced latch-up	= 2 x 10^8 rads (Si)/s 5/
Dose rate survivability	= 5 x 10^{11} rads (Si)/s 5/
Neutron irradiated	= 1 x 10^{14} neutrons/cm^2 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to + 125°C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:

Case C	13.5 mW/°C
Case X	8.6 mW/°C

5/ Guaranteed by design or process but not tested.
6/ Device type 02 only.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Supply current	I_{DD}	V_{DD} = 5 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		1.0	µA
				2 1/		30	
		V_{DD} = 10 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		2.0	
				2 1/		60	
		V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		2.0	
				2 1/		120	
		V_{DD} = 20 V, V_{IN} = 0.0 V or V_{DD}	All	1		2.0	
				2		200	
		M, D, P, L, R 2/	All	1		7.5	
		V_{DD} = 18 V, V_{IN} = 0.0 V or V_{DD}	All	3		2.0	
Low level output current (sink)	I_{OL}	V_{DD} = 5 V V_O = 0.4 V V_{IN} = 0.0 V or V_{DD}	All	1	0.53		mA
				2 1/	0.36		
				3 1/	0.64		
		V_{DD} = 10 V V_O = 0.5 V V_{IN} = 0.0 V or V_{DD}	All	1	1.4		
				2 1/	0.9		
				3 1/	1.6		
		V_{DD} = 15 V V_O = 1.5 V V_{IN} = 0.0 V or V_{DD}	All	1	3.5		
				2 1/	2.4		
				3 1/	4.2		
High level output current (source)	I_{OH}	V_{DD} = 5 V V_O = 4.6 V V_{IN} = 0.0 V or V_{DD}	All	1		-0.53	mA
				2 1/		-0.36	
				3 1/		-0.64	
		V_{DD} = 5 V V_O = 2.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-1.8	
				2 1/		-1.15	
				3 1/		-2.0	
		V_{DD} = 10 V V_O = 9.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-1.4	
				2 1/		-0.9	
				3 1/		-1.6	
		V_{DD} = 15 V V_O = 13.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-3.5	
				2 1/		-2.4	
				3 1/		-4.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Output voltage, high	V_{OH}	V_{DD} = 5 V, no load 1/	All	1, 2, 3	4.95		V
		V_{DD} = 10 V, no load 1/		1, 2, 3	9.95		
		V_{DD} = 15 V, no load 3/		1, 2, 3	14.95		
Output voltage, low	V_{OL}	V_{DD} = 5 V, no load 1/	All	1, 2, 3		50	mV
		V_{DD} = 10 V, no load 1/		1, 2, 3		50	
		V_{DD} = 15 V, no load		1, 2, 3		50	
Input voltage, low	V_{IL}	V_{DD} = 5 V V_{OH} > 4.5 V, V_{OL} < 0.5 V	All	1, 2, 3		1.5	V
		V_{DD} = 10 V V_{OH} > 9.0 V, V_{OL} < 1.0 V 1/		1, 2, 3		3	
		V_{DD} = 15 V V_{OH} > 13.5 V, V_{OL} < 1.5 V		1, 2, 3		4	
Input voltage, high	V_{IH}	V_{DD} = 5 V V_{OH} > 4.5 V, V_{OL} < 0.5 V	All	1, 2, 3	3.5		V
		V_{DD} = 10 V V_{OH} > 9.0 V, V_{OL} < 1.0 V 1/		1, 2, 3	7		
		V_{DD} = 15 V V_{OH} > 13.5 V, V_{OL} < 1.5 V		1, 2, 3	11		
Input leakage current, low	I_{IL}	V_{IN} = V_{DD} or GND, V_{DD} = 20 V	All	1	-100		nA
		V_{IN} = V_{DD} or GND, V_{DD} = 20 V		2	-1000		
		V_{IN} = V_{DD} or GND, V_{DD} = 18 V		3	-100		
Input leakage current, high	I_{IH}	V_{IN} = V_{DD} or GND, V_{DD} = 20 V	All	1		100	
		V_{IN} = V_{DD} or GND, V_{DD} = 20 V		2		1000	
		V_{IN} = V_{DD} or GND, V_{DD} = 18 V		3		100	
N threshold voltage	V_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA	All	1	-0.7	-2.8	V
		M, D, P, L, R 2/	All	1	-0.2	-2.8	
N threshold voltage, delta	ΔV_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA, M, D, P, L, R 2/	All	1		±1.0	
P threshold voltage	V_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA	All	1	0.7	2.8	
		M, D, P, L, R 2/	All	1	0.2	2.8	
P threshold voltage, delta	ΔV_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA M, D, P, L, R 2/	All	1		±1.0	
Input capacitance	C_{IN} 1/	Any input, See 4.4.1c	All	4		7.5	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Functional tests		V_{DD} = 2.8 V, V_{IN} = V_{DD} or GND	All	7	$V_{OH} > V_{DD}/2$	$V_{OL} < V_{DD}/2$	V
		V_{DD} = 20 V, V_{IN} = V_{DD} or GND		7			
		V_{DD} = 18 V, V_{IN} = V_{DD} or GND	All	8A			
		M, D, P, L, R 2/	All	7			
		V_{DD} = 3.0 V, V_{IN} = V_{DD} or GND	All	8B			
		M, D, P, L, R 2/	All	7			
Propagation delay time, input to output 4/	t_{PHL}, t_{PLH}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		280	ns
				10, 11		378	
		M, D, P, L, R 2/	All	9		378	
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND	All	9 1/		130	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9 1/		100	
Transition time 4/	t_{THL}, t_{TLH}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		200	ns
				10, 11		270	
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND	All	9 1/		100	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9 1/		80	

1/ These tests are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which affect these characteristics.

2/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ For accuracy, voltage is measured differentially to V_{DD}. Limit is 0.050 V max.

4/ Load capacitance (C_L) = 50 pF, load resistance (R_L) = 200 kΩ, and input rise and fall times (t_r, t_f) < 20 ns.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	V_{DD} = 3.0 V 4/ Effective LET No single event upsets (SEU)	Bias V_{DD} = 18.0 V for Single event latch-up (SEL) test No SEL at effective LET = 5/ 6/
01	LET = 75 MeV/(mg/cm^2) 7/	LET = 75 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.5 herein.
2/Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at worst case temperature, T_A = +25˚C ±10°C.
4/ Tested at worst case temperature, T_A = +125˚C ±10°C for latch-up.
5/ Tested to a LET of ≤ 75 MeV/(mg/cm^2), with no latch-up (SEL).
6/ Tested to a LET of ≤ 75 MeV/(mg/cm^2) with no single event upsets (SEU).
7/ Guaranteed by design or process but not tested.

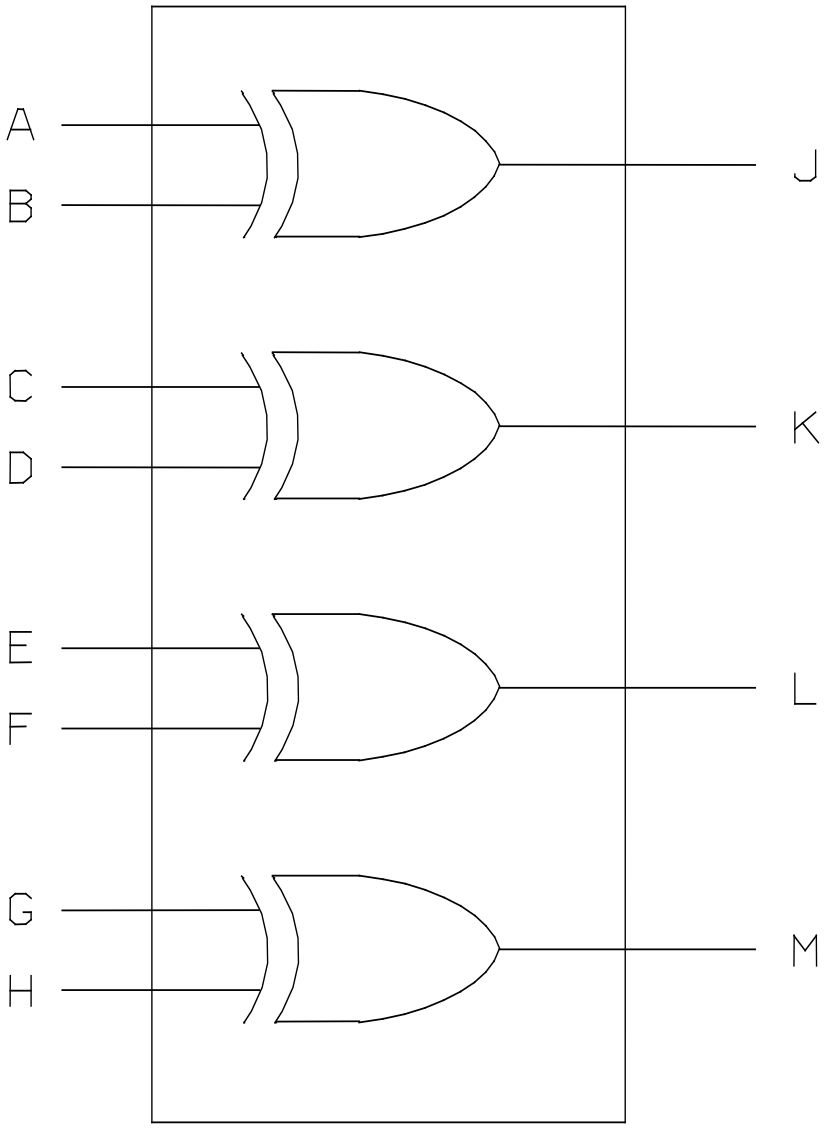
Device types	All
Case outlines	C and X
Terminal number	Terminal symbol
1	A
2	B
3	J = A ⊕ B
4	K = C ⊕ D
5	C
6	D
7	V_{SS}
8	E
9	F
10	L = E ⊕ F
11	M = G ⊕ H
12	G
13	H
14	V_{DD}

FIGURE 1. Terminal connections.

Inputs		Outputs
A, C, E, G	B, D, F, H	J, K, L, M
L	L	L
H	L	H
L	H	H
H	H	L

H = High logic level
L = Low logic level

FIGURE 2. Truth table.



$J = A \oplus B \quad M = G \oplus H$
$K = C \oplus D \quad L = E \oplus F$

FIGURE 3. Block diagram.

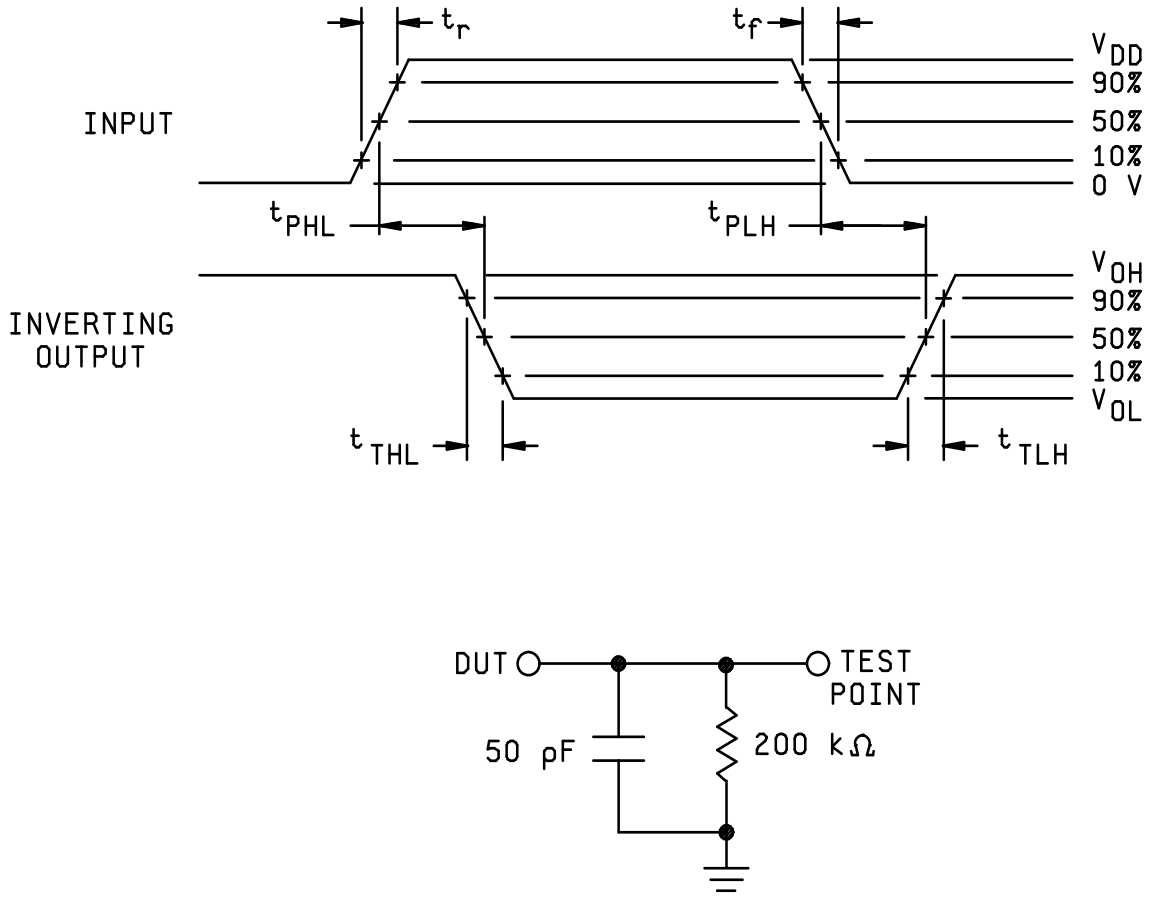


FIGURE 4. Load circuit and switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. Tests shall be sufficient to validate the limits defined in table IA herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, 9 and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter	Symbol	Delta limits
Supply current	I_{DD}	±0.2 μA
Output current (sink) V_{DD} = 5.0 V	I_{OL}	±20%
Output current (source) V_{DD} = 5.0 V, V_{OUT} = 4.6 V	I_{OH}	±20%

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. Neutron irradiation for device 02, 04, and 06 shall be conducted in wafer form using a neutron fluence of approximately 1 x 10^{14} neutrons/cm^2.

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.4 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process change which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime, when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA , Columbus, Ohio 43218-3990, or telephone (614) 692-8108.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

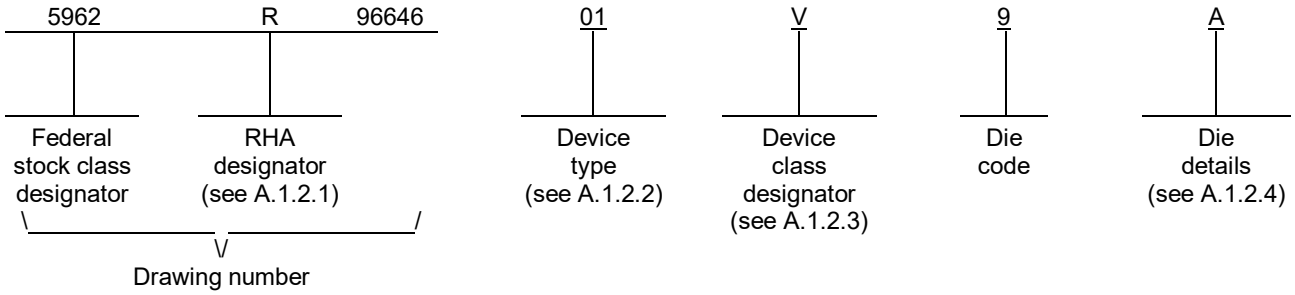
c. Number of transients (SET).

d. Occurrence of latchup (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4030B	Radiation hardened, CMOS, quad exclusive OR gate
02	4030BN	Radiation hardened, CMOS, quad exclusive OR gate with neutron irradiated die

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

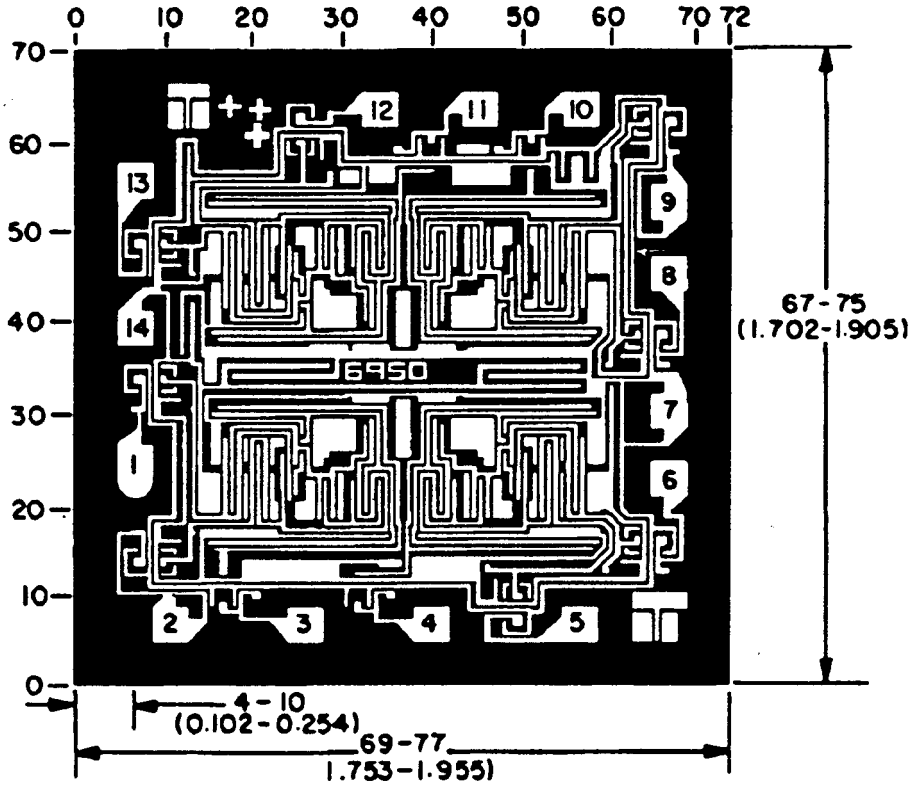
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-8108.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and maritime - VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	1778 x 1829 microns
Die thickness:	20 ±1 mils

Interface materials.

Top metallization:	Al
Thickness	11.0kÅ – 14.0kÅ
Backside metallization:	None

Glassivation.

Type:	PSG
Thickness:	10.4kÅ - 15.6kÅ

Substrate: Single Crystal Silicon

Assembly related information.

Substrate potential:	Floating or tied to V_{DD}
Special assembly instructions:	Bond pad #14 (V_{DD}) first.

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-01-31

Approved sources of supply for SMD 5962-96646 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9664601VCC	34371	CD4030BDMSR
5962R9664601VXC	34371	CD4030BKMSR
5962R9664601V9A	34371	CD4030BHSR
5962R9664602VCC	3/	CD4030BDNSR
5962R9664602VXC	3/	CD4030BKNSR
5962R9664602V9A	3/	CD4030BHNSR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406