REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changed the maximum Operating Supply Current and Enable Supply Current parameters of Table I for radiation level. – ksr.	98-10-02	Raymond Monnin
B	Removed references to device class M. Updated document to reflect current MIL-PRF-38535 requirements. – glg	13-08-21	Charles F. Saffle
C	10 Year Review boilerplate update to current MIL-PRF-38535 requirements. – llb	24-01-29	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
Jeff Bowling

CHECKED BY
Jeff Bowling

APPROVED BY
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DRAWING APPROVAL DATE
97-10-20

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

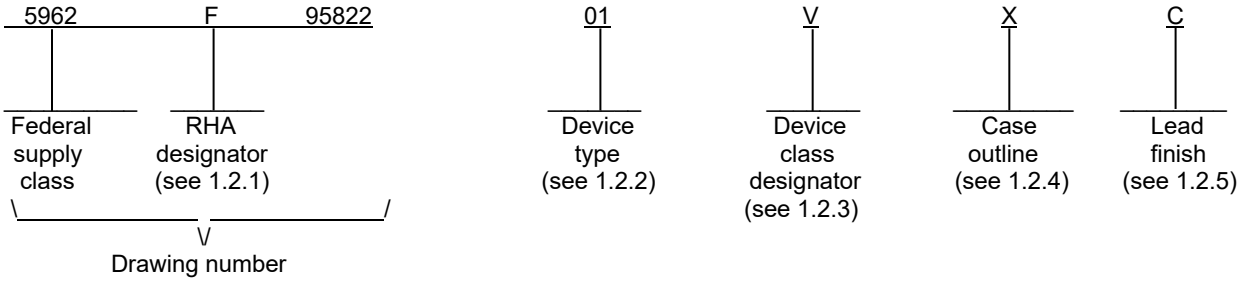
MICROCIRCUIT, MEMORY, DIGITAL, CMOS/SOS, RADIATION HARDENED, 64K X 1 STATIC RAM, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **67268**	**5962-95822**
		SHEET	1 OF 20	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	65643ARH	64K X 1 Radiation hardened CMOS/SOS SRAM	50 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	24	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V to +7.0 V dc
Input, output, or I/O voltage	-0.3 V dc to V_{DD} +0.3 V dc
Maximum package power dissipation (P_D) at T_A = +125°C	0.78 W 3/
Lead temperature (soldering, 10 seconds maximum)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	8.8°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	64.0°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0.0 V dc
Input high voltage (V_{IH})	0.8V_{DD} to V_{DD}
Input Low voltage (V_{IL})	0.0 V dc to 0.2V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Data retention supply voltage	2.0 V dc minimum
Input rise and fall time	5 ns maximum

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	≥ 300 KRads(Si)
Dose rate upset (20 ns pulse)	1 x 10^{11} Rads(Si)/sec 4/
Dose rate survivability	≥ 1 x 10^{12} Rads(Si)/sec 4/
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets	≥ 100 MeV/(cm^2/mg) 4/
Latch-up	None 4/
Cosmic ray upset immunity	< 1 x 10^{-10} errors/bit-day 4/ 5/

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate: case outline X - - - 15.6 mW/°C.

4/ Guaranteed by process or design, but not tested.

5/ Single event upset error rates are obtained using Adams 10% worst case environment under worst case conditions.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.5 Functional tests. Functional tests used to test this device shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/		Unit
						Min	Max	
High level output voltage	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -8.0 mA		1, 2, 3	01	2.4		V
		V_{IN} = GND or V_{DD}	M, D, P, L, R, F	1 2/		3/		
	V_{OH2}	V_{DD} = 4.5 V, I_{OH} = -100 mA		1, 2, 3	01	V_{DD} - 0.4		V
		V_{IN} = GND or V_{DD}	M, D, P, L, R, F	1 2/		3/		
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8 mA		1, 2, 3	01		0.4	V
		V_{IN} = GND or V_{DD}	M, D, P, L, R, F	1 2/			3/	
Input leakage current	I_{IN}	V_{DD} = 5.5 V		1, 2, 3	01	-1	1	µA
		V_{IN} = GND or V_{DD}	M, D, P, L, R, F	1 2/		3/	3/	
High impedance output leakage current	I_{OZ}	V_{DD} = 5.5 V, V_{IN} = V_{DD} or GND,		1, 3	01	-10	10	µA
		V_{OUT} = GND or V_{DD}, $\overline{E}$ = V_{DD}		4/		-20	20	
				2		-60	60	
			M, D, P, L, R, F	1 2/		-10	10	
Operating supply current 5/	I_{DDOP}	V_{DD} = 5.5 V, f = 2 MHz		1	01		25.5	mA
		V_{IN} = GND or V_{DD}		4/			23.5	
		$\overline{E}$ = GND, I_{OUT} = 0 mA		2			26.5	
				3			28.5	
			M, D, P, L, R, F	1 2/			32	
Standby supply current	I_{DDSB}	V_{DD} = 5.5 V, I_{OUT} = 0 mA		1, 3	01		500	µA
		V_{IN} = GND or V_{DD}		4/			4	
		$\overline{E}$ = V_{DD}		2			13	
			M, D, P, L, R, F	1 2/			10	
Enable supply current	I_{DDEN}	V_{DD} = 5.5 V, I_{OUT} = 0 mA		1	01		21.5	mA
		V_{IN} = GND or V_{DD}		4/			21.5	
		$\overline{E}$ = V_{DD}		2			24.5	
				3			25.5	
			M, D, P, L, R, F	1 2/			30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/		Unit
						Min	Max	
Data retention current	I_{DDDR}	V_{DD} = 5.5 V, I_{OUT} = 0 mA		1, 3	01		50	µA
		V_{IN} = GND or V_{DD}		4/			1	mA
		$\overline{E}$ = V_{DD}		2			4	
			M, D, P, L, R, F	1 2/			6	
Data retention voltage	V_{DR}			1, 2, 3	01	2.0		V
			M, D, P, L, R, F	1 2/		3/		
Input capacitance 6/	C_{IN}	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		10	pF
I/O capacitance 6/	$C_{I/O}$	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		10	pF
Functional tests	FT	See 4.4.1d, V_{DD} = 4.5 V and 5.5 V, f = 1 MHz,		7, 8A, 8B	01			
		V_{IN} = GND or V_{DD}	M, D, P, L, R, F	7 2/		3/		
Noise immunity functional Test	FN	V_{DD} = 4.5 V, f = 1 MHz, V_{IH} = 0.8 V_{DD},		7, 8A, 8B	01			
		V_{IL} = 0.2V_{DD}	M, D, P, L, R, F	7 2/		3/		
Read/write cycle 6/	t_{AVAX}	See figure 3, V_{DD} = 4.5 V 8/		9, 10, 11	01	50		ns
			M, D, P, L, R, F	9 2/		3/		
Address access time	t_{AVQV}			9, 10, 11	01		50	ns
			M, D, P, L, R, F	9 2/			3/	
Output hold from address 6/	t_{AXQX}			9, 10, 11	01	0		ns
			M, D, P, L, R, F	9 2/		3/		
Chip enable access time	t_{ELQV}			9, 10, 11	01		50	ns
			M, D, P, L, R, F	9 2/			3/	
Chip enable to output active 6/	t_{ELQX}			9, 10, 11	01	0		ns
			M, D, P, L, R, F	9 2/		3/		
Chip enable to output in high-Z 6/	t_{EHQZ}			9, 10, 11	01		15	ns
			M, D, P, L, R, F	9 2/			3/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Address setup time	t_{AVEL}	See figure 3, V_{DD} = 4.5 V 8/	9, 10, 11	01	5		ns
		M, D, P, L, R, F	9 2/		3/		
	t_{AVWL}		9, 10, 11	01	10		ns
		M, D, P, L, R, F	9 2/		3/		
Address setup time	t_{AVEL}	see figure 4, V_{DD} = 4.5 V 7/	9, 10, 11	01	5		ns
		M, D, P, L, R, F	9 2/		3/		
	t_{AVWL}		9, 10, 11	01	10		ns
		M, D, P, L, R, F	9 2/		3/		
Write enable pulse width	t_{WLWH}		9, 10, 11	01	25		ns
		M, D, P, L, R, F	9 2/		3/		
Write recovery time	t_{WHAX}		9, 10, 11	01	0		ns
		M, D, P, L, R, F	9 2/		3/		
Address hold time	t_{EHAX}		9, 10, 11	01	0		ns
		M, D, P, L, R, F	9 2/		3/		
Data set-up time	t_{DVWH}		9, 10, 11	01	30		ns
	t_{DVEH}	M, D, P, L, R, F	9 2/		3/		
Write enable high to output active 6/	t_{WHQX}	see figure 4, V_{DD} = 4.5 V and 5.5 V 7/	9, 10, 11	01	0		ns
		M, D, P, L, R, F	9 2/		3/		
Data hold time	t_{WHDX}	see figure 4, V_{DD} = 4.5 V 7/	9, 10, 11	01	0		ns
	t_{EHDX}	M, D, P, L, R, F	9 2/		3/		
Write enable to output high-Z 6/	t_{WLQZ}		9, 10, 11	01		15	ns
		M, D, P, L, R, F	9 2/			3/	
Chip enable to end of write	t_{ELWH}		9, 11	01	30		ns
			10 8/		38		
		M, D, P, L, R, F	9 2/		3/		
Chip enable pulse width	t_{ELEH}		9, 11	01	30		ns
			10 8/		38		
		M, D, P, L, R, F	9 2/		3/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Write enable to end of write	t_{WLEH}		9, 10, 11	01	30		ns
		M, D, P, L, R, F	9 2/		3/		
Address valid to end of write	t_{AVWH}	see figure 4, V_{DD} = 4.5 V 7/	9, 11	01	30		ns
			10 8/		38		
		M, D, P, L, R, F	9 2/		3/		
	t_{AVEH}		9, 11	01	35		ns
			10 8/		40		
		M, D, P, L, R, F	9 2/		3/		

1/ Device also receives 100% testing and group A sample inspection at +85°C. Unless otherwise specified, the limit is the same as defined at +125°C.

2/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C. The M, D, P, L, R, F levels in the test condition column are the postirradiation limits for the device types specified in the device type column.

3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.

4/ Limit at +85°C.

5/ For each 1MHz increase in address frequency, there is a 3mA(typical) increase in operating supply current.

6/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

7/ AC measurements assume rise and fall times of 5 ns or less, timing reference levels of 2.0 V, input pulse levels of 0 to V_{DD}, and the output load = 1 TTL equivalent load and $C_L \ge 50$ pF. For $C_L > 50$ pF, access times are derated 0.15ns/pF.

8/ Limits at +85°C and +125°C.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7*, 9 Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7*, 9 Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 8/	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 8/
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 8/	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 8/
8	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B 8/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 8/ Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1, 7, and 9.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.5.
8/ In addition, testing is performed at +85°C.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{IN}	±150 nA of specified value in Table I
I_{OZ}	±2 µA of specified value in Table I
I_{DDSB}	±150 µA of specified value in Table I
V_{OL}	±60 mV of specified value in Table I
V_{OH1}	±400 mV of specified value in Table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

Case X

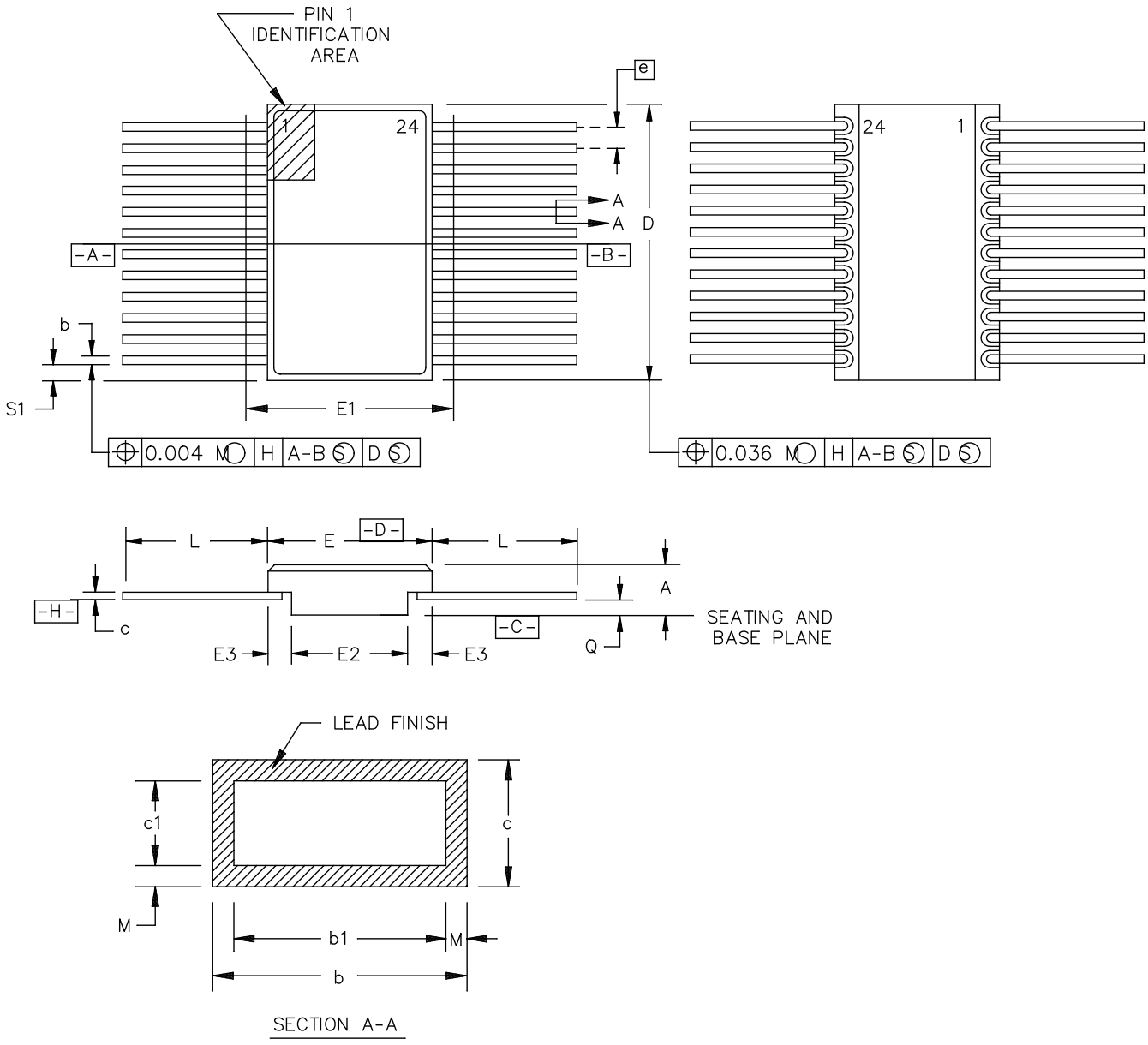


FIGURE 1. Case outline.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.78	2.92	.070	.115
B	0.38	0.56	.015	.022
b1	0.38	0.48	.015	.019
c	0.10	0.23	.004	.009
c1	0.10	0.15	.004	.006
D	14.99	15.49	.590	.610
E	12.45	12.95	.490	.510
E1	---	13.20	---	.520

Symbol	Millimeters		Inches	
	Max	Min	Min	Max
E2	9.40	9.91	.370	.390
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
L	8.38	8.89	.330	.350
M	---	0.04	---	.0015
Q	0.66	1.14	.026	.045
S1	0.13	---	.005	---
N	24			

NOTES:
1. Although dimensions are in inches, the US government preferred system of measurement is the SI metric system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. Dimensions D and E1 allow for off-center lid, meniscus, and glass overrun.
3. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. The minimum shall be reduced by 0.038 mm (0.0015 inch) maximum when solder dip lead finish is applied.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. Measure dimension S1 at all four corners.
6. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom or the package to cover the leads.

FIGURE 1. Case outline - continued.

Device types	All
Case outlines	X,Y
Terminal number	Terminal symbol
1	A_0
2	A_1
3	A_2
4	A_3
5	A_4
6	A_5
7	A_6
8	A_7
9	NC
10	Q
11	$\overline{W}$
12	GND
13	$\overline{E}$
14	D
15	A8
16	A9
17	A10
18	A11
19	A12
20	A13
21	A14
22	A15
23	NC
24	V_{DD}

FIGURE 2. Terminal connections.

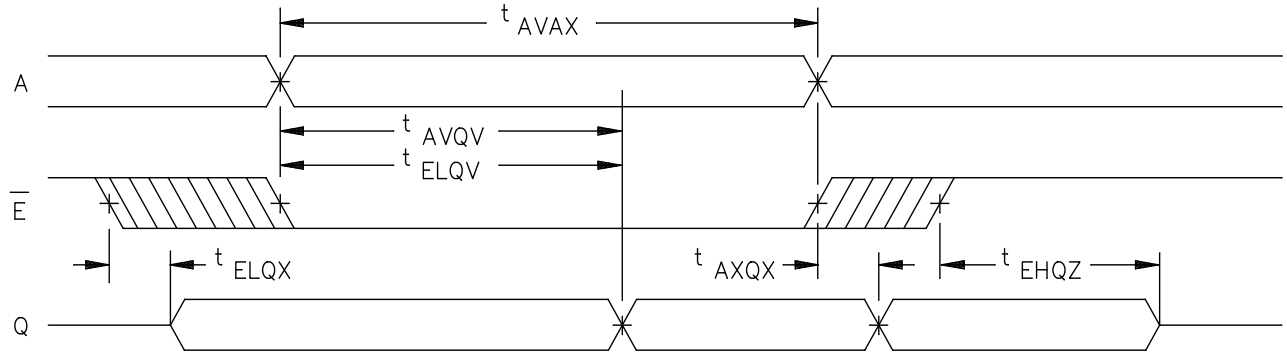
Read modes

Mode	$\overline{E}$	$\overline{W}$	Outputs	Power
Not selected	H	X	High Z	Standby
Read	L	H	Data out	Active
Write	L	L	High Z	Active

NOTES:
1. L = logic low voltage level; H = logic high voltage level; X can be H or L.
2. High Z is high impedance state.

FIGURE 3. Truth table.

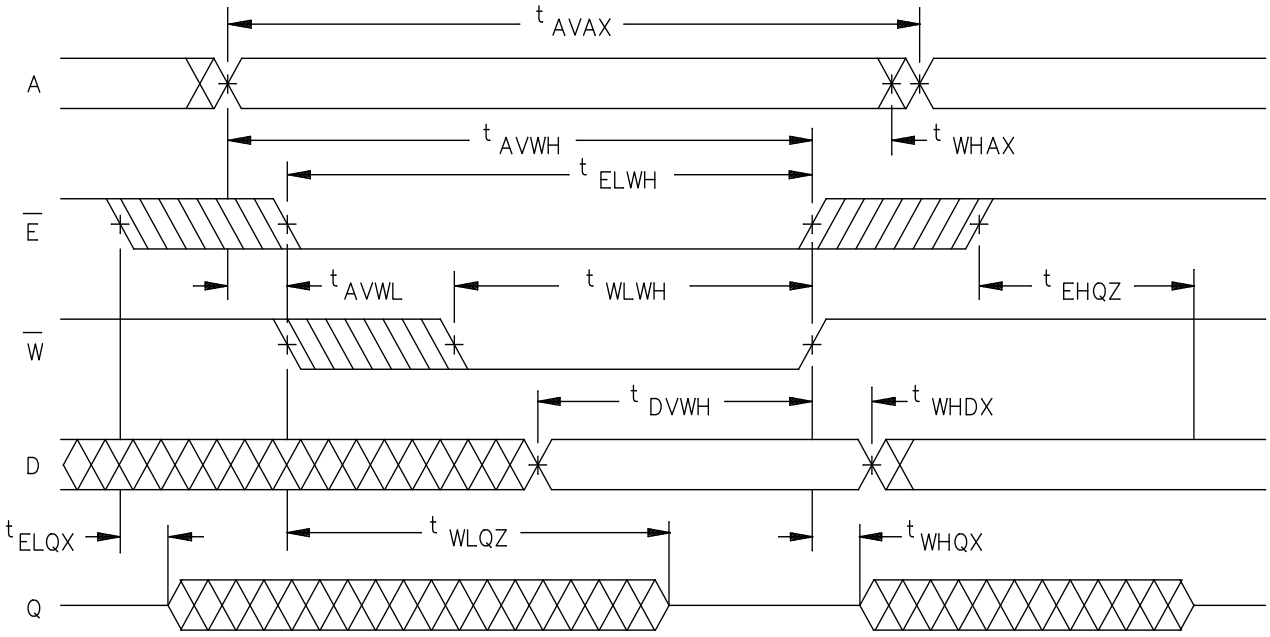
Read cycle (see note)



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

FIGURE 4. Timing waveforms.

Write cycle 1: $\overline{W}$ controlled (see note)



NOTE: In this mode $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

FIGURE 4. Timing waveforms - continued.

Write cycle 2: $\overline{E}$ controlled

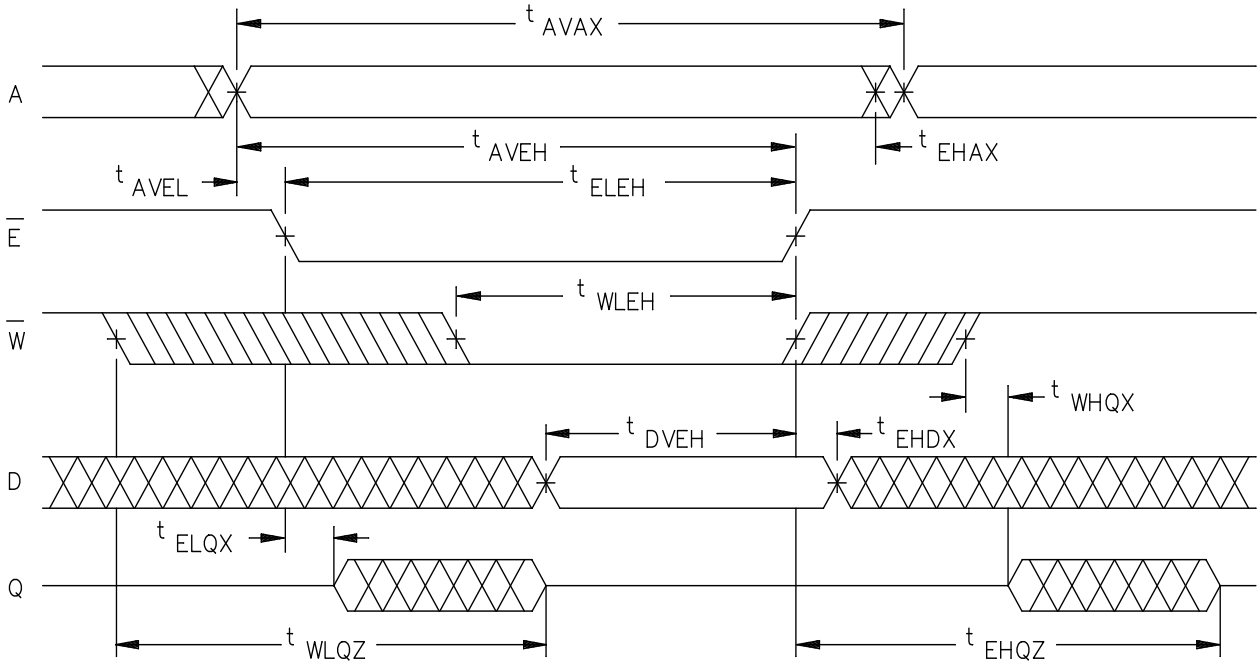


FIGURE 4. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

d. For device classes Q and V subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. Dose rate induced latch-up testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

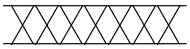
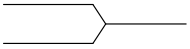
6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

C_{IN} .....Input terminal capacitance.
$C_{I/O}$.....Output terminal capacitance.
GND .....Ground zero voltage potential.
I_{DD}.....Supply current.
I_I.....Input current.
I_O.....Output current.
T_C .....Case temperature.
V_{DD}.....Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-01-29

Approved sources of supply for SMD 5962-95822 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9582201QXC	3/	HS9-65643ARH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406