

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R054-96.	96-02-01	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. – LTG	08-01-23	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-10-21	Muhammad A. Akbar
D	Update boilerplate to current MIL-PRF-38535 requirements. - DRH	25-06-09	Muhammad A. Akbar



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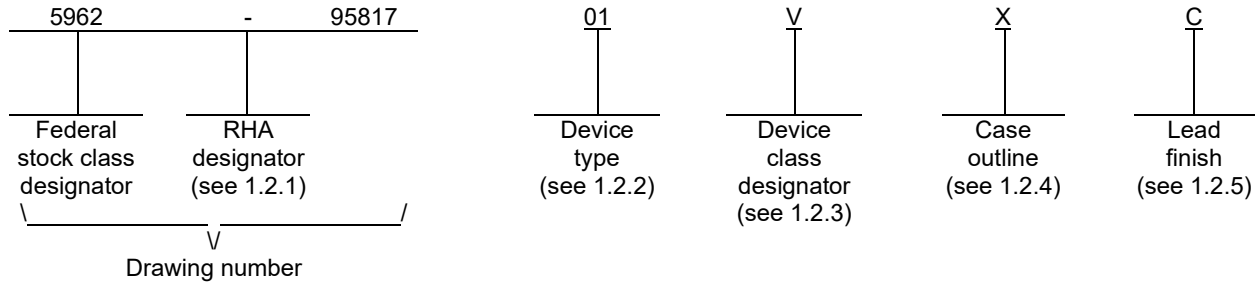
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Thomas M. Hess	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p> <p align="center">MICROCIRCUIT, DIGITAL, SERIAL CONTROLLER INTERFACE, MONOLITHIC SILICON</p>																
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thomas M. Hess																	
	APPROVED BY Monica L. Poelking																	
	DRAWING APPROVAL DATE 95-12-28																	
	REVISION LEVEL D	SIZE A	CAGE CODE 67268	5962-95817														
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	82C52/7	Serial controller interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V

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1.3 Absolute maximum ratings. 1/

Supply voltage (V _{DD})	+8.0 V dc
Input, output or I/O voltage range	GND -0.5 V dc to V _{DD} + 0.5 V dc
Storage temperature range (T _{STG})	-65°C to +150°C
Junction temperature (T _J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC}):	
Case outline X	6°C/W
Thermal resistance, junction-to-ambient (θ _{JA}):	
Case outline X	45°C/W
Maximum package power dissipation +125°C (P _D)	1.11 W 2/

1.4 Recommended operating conditions.

Operating supply voltage range (V _{DD})	4.5 V dc to +5.5 V dc
Ambient operating temperature range (T _A)	-55°C to +125°C
Input low voltage range (V _{IL})	0 V dc to +0.8 V dc
Input high voltage range (V _{IH})	0.7 V _{DD} to V _{DD}
Input low voltage range (V _{ILC}) and (V _{TL})	GND + 0.5 V
Input high voltage range (V _{IHC}) and (V _{TH})	V _{DD} - 0.5 V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the rate of 22.2 mW/°C

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and load circuit. The switching waveforms and load circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical "1" input voltage	V _{IH}	V _{DD} = 5.5 V <u>2/</u>	1, 2, 3	All	0.7V _{DD}		V
Logical "0" input voltage	V _{IL}	V _{DD} = 4.5 V <u>2/</u>	1, 2, 3	All		0.8	V
CLK logical "1" input voltage	V _{IH(CLK)}	External clock, V _{DD} = 5.5 V <u>2/</u>	1, 2, 3	All	V _{DD} -0.5		V
CLK logical "0" input voltage	V _{IL(CLK)}	External clock, V _{DD} = 4.5 V <u>2/</u>	1, 2, 3	All		GND+0.5	V
Schmitt trigger logical one input voltage	V _{TH}	V _{DD} = 5.5 V <u>2/</u> Reset input, pin 13	1, 2, 3	All	V _{DD} -0.5		V
Schmitt trigger logical zero input voltage	V _{TL}	V _{DD} = 4.5 V <u>2/</u> Reset input, pin 13	1, 2, 3	All	V _{DD} -0.5	GND+0.5	V
High level output voltage	V _{OH}	V _{DD} = 4.5 V, I _{OH} = -2.5 mA Except 0X <u>3/</u>	1, 2, 3	All	3.0		V
		V _{DD} = 4.5 V, I _{OH} = -100 μA For 0X, I _{OH} = -1.0 mA <u>3/</u>			V _{DD} -0.4		
Low level output voltage	V _{OL}	V _{DD} = 4.5 V, I _{OL} = +2.5 mA For 0X, I _{OL} = +1.0 mA <u>3/</u>	1, 2, 3	All		0.4	V
Input leakage current	I _{IL} , I _{IH}	V _{DD} = 5.5 V, V _{IN} = GND or V _{DD} All inputs except IX <u>3/</u>	1, 2, 3	All	-1.0	+1.0	μA
Output leakage current	I _{OZL} , I _{OZH}	V _{DD} = 5.5 V V _{IN} = GND or V _{DD}	1, 2, 3	All	-10	+10	μA
Standby power supply current	I _{CCSB}	V _{DD} = 5.5 V, V _{IN} = V _{DD} or GND Outputs open	1, 2, 3	All		100	μA
Operating power supply current	I _{CCOP}	V _{DD} = 5.5 V, V _{IN} = V _{DD} or GND Outputs open, f = 2.5 MHz External clock	1, 2, 3	All		3.0	mA
Input capacitance	C _{IN}	V _{DD} = open, f = 1 MHz All measurements are referenced device GND See 4.4.1c	4	All		12	pF
Output capacitance	C _{OUT}		4	All		15	pF
I/O capacitance	C _{I/O}		4	All		15	pF
Functional tests		V _{DD} = 4.5 V and 5.5 V <u>4/</u> See 4.4.1b	7, 8	All			
Read disable	t _{RHDZ}	V _{DD} = 4.5 V and 5.5 V <u>5/ 6/</u>	9, 10, 11	All	0	60	ns
IX input rise/fall time	t _R /t _F	V _{DD} = 4.5 V and 5.5 V <u>5/ 7/</u>	9, 10, 11	All		tx	ns
Select setup to control leading edge	t _{SVCTL}	<u>8/</u>	9, 10, 11	All	30		ns
Select hold from control trailing edge	t _{CTHSX}	<u>8/</u>	9, 10, 11	All	50		ns
Control pulse width	t _{CTLCTH}	Control consists of \overline{RD} or \overline{WR} <u>8/</u>	9, 10, 11	All	150		ns
Control disable to control enable	t _{CTHCTL}	<u>8/</u>	9, 10, 11	All	190		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read low to data valid	t _{RLDV}	Test condition 1 <u>8/</u>	9, 10, 11	All		120	ns
Data setup time	t _{DVWH}	<u>8/</u>	9, 10, 11	All	50		ns
Data hold time	t _{WHDX}	<u>8/</u>	9, 10, 11	All	20		ns
Clock high time	t _{CHCL}	<u>8/</u>	9, 10, 11	All	25		ns
Clock low time	t _{CLCH}	<u>8/</u>	9, 10, 11	All	25		ns
Clock output fall time	t _{FCO}	From 0.7 V _{DD} to 0.8 V <u>8/</u>	9, 10, 11	All		15	ns
Clock output rise time	t _{RCO}	From 0.7 V _{DD} to 0.8 V <u>8/</u>	9, 10, 11	All		15	ns

1/ All test to be performed using worst case test conditions unless otherwise specified.

2/ Verified as a Go/No go test.

3/ Interchanging of force and sense conditions is permitted.

4/ Tested as follows: V_{IH} = 0.7V_{DD}, V_{IL} = 0.8 V, C_L = 50 pF, V_{OH} ≥ 1.5 V, V_{OL} ≤ 1.5 V, V_{IHC} = V_{DD} - 0.5 V, V_{ILC} = GND +0.5 V, V_{TL} = GND +0.5 V.

5/ The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

6/ Reference test condition 2 of test condition definition table with ac test circuit (See figure 3).

7/ t_x ≥ 1/6 FC or 50 ns, whichever is less.

8/ Unless otherwise specified V_{DD} = 4.5 V. V_{IH} = 0.7V_{DD}, V_{IL} = 0.8 V, C_L = 50 pF unless a test condition is specified. V_{OH} ≥ 1.5 V and V_{OL} ≤ 1.5 V, V_{IHC} = V_{DD} -0.5 V, V_{ILC} = GND +0.5 V, V_{TH} = V_{DD} -0.5 V, V_{TL} = GND +0.5 V.

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Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	\overline{RD}	15	SD0
2	\overline{WR}	16	GND
3	D0	17	\overline{CTS}
4	D1	18	\overline{DSR}
5	D2	19	\overline{DTR}
6	D3	20	\overline{RTS}
7	D4	21	CO
8	D5	22	TBRE
9	D6	23	RST
10	D7	24	INTR
11	A0	25	SDI
12	A1	26	DR
13	IX	27	V _{DD}
14	OX	28	$\overline{CS0}$

FIGURE 1. Terminal connections.

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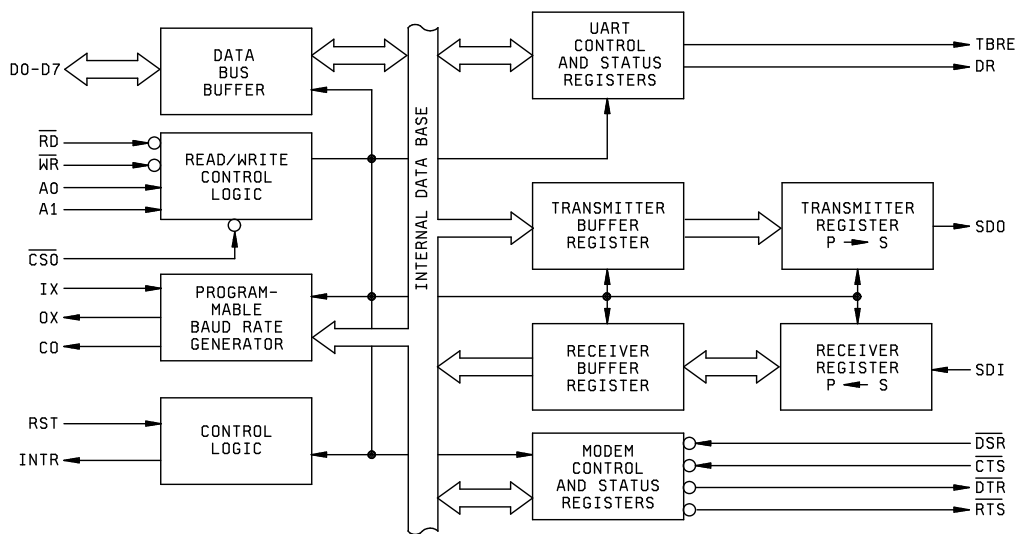


FIGURE 2. Block diagram.

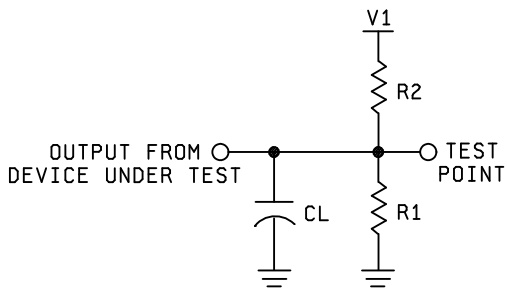
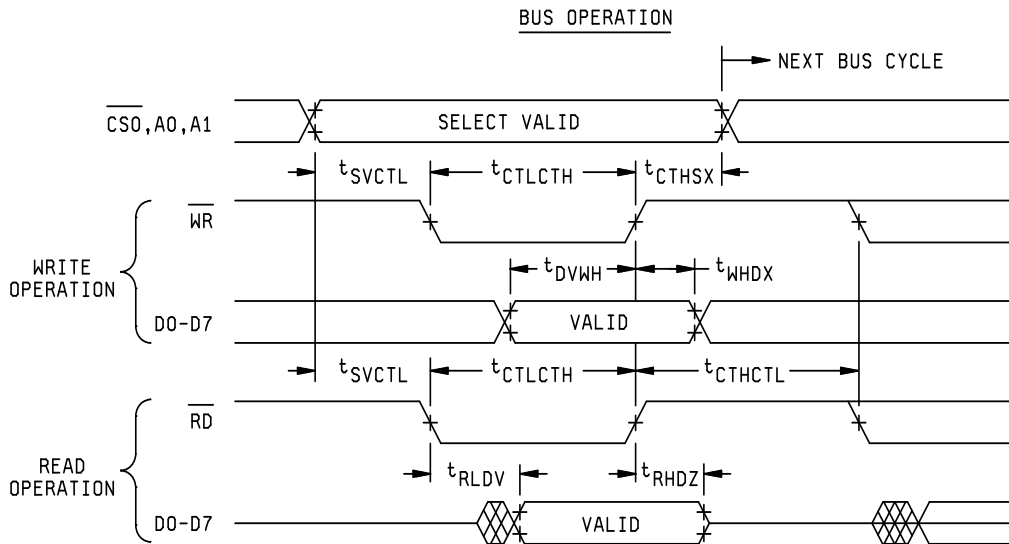
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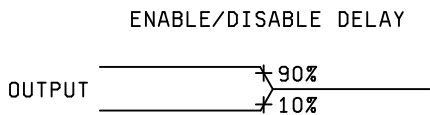
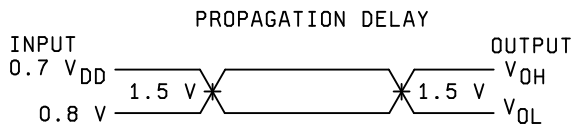
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	Test condition	V_1	$R_1(\Omega)$	$R_2(\Omega)$	$C_L(\text{pF})$
1	Propagation delay	1.7V	520	8	100
2	Disable delay	V_{DD}	5k	5k	50



NOTE: All input signals (except IX and RST) must switch between 0.8 V and $0.7 V_{DD}$. Input rise and fall times are driven at 1 ns/V .

FIGURE 3. Switching waveform and load circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C_{IN}, C_{OUT} and C_{I/O} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/ 3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.

2/ PDA applies to subgroups 1, 7 and delta's.

3/ Delta limits as specified in table IIB herein shall be required where specified and delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°).

Parameter <u>1/</u>	Symbol	Delta limits
Standby power supply current	I _{CCSB}	±15 μA
Output leakage current	I _{OZL} , I _{OZH}	±2.0 μA
Input leakage current	I _{IH} , I _{IL}	±200 nA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
\overline{RD}	I	READ: The \overline{RD} input causes the device to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0-A1), $\overline{CS0}$ enables the \overline{RD} input.
\overline{WR}	I	WRITE: \overline{WR} input causes data from the data bus (D0-D7) to be input to the device. Addressing and chip select action is the same as for read operations.

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
D0-D7	I/O	DATA BITS 0-7: The data bus provides eight, three-state input/output lines for the transfer of data, control and status information between the device and the CPU. For character formats of less than 8-bits, the corresponding D7, D6, and D5 are considered "don't cares" for data WRITE operations and are 0 for data READ operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0,A1	I	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX,OX	I/O	CRYSTAL/CLOCK: Crystal connections for the internal baud rate generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	O	SERIAL DATA OUTPUT: Serial data output from the device transmitter circuitry. A mark (1) is a logic one (high) and space (0) is logic zero (low). SDO is held in the mark condition when \overline{CTS} is false, when RST is true, when the transmitter register is empty, or when in the loop mode.
GND		GROUND: Power supply ground connection.
\overline{CTS}	I	CLEAR TO SEND: The logical state of the \overline{CTS} line is reflected in the \overline{CTS} bit of the modem status register. Any change of state in \overline{CTS} causes INTR to be set true when INTEN and MIEN are true. A false level on \overline{CTS} will inhibit transmission of data on the SDO output and will hold SDO in the mark (high) state. If \overline{CTS} goes false during transmission, the current character being transmitted will be completed, \overline{CTS} does not affect loop mode operation.
\overline{DSR}	I	DATA SET READY: The logical state of the \overline{DSR} line is reflected in the modem status register. Any change of state of \overline{DSR} will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the device.
\overline{DTR}	O	DATA TERMINAL READY: The \overline{DTR} signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 in the \overline{DTR} bit in the MCR or whenever a reset (RST = high) is applied to the device.
\overline{RTS}	O	REQUEST TO SEND: The \overline{RTS} signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the \overline{RTS} bit in the MCR or whenever a reset (RST = high) is applied to the device.
CO	O	CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered baud rate generator (16X) clock output. The buffered IX (crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal baud rate generator clock which operates at sixteen times the programmed baud rate. On reset D7 (CO select) is reset to 0.
TBRE	O	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the transmit register. Application of a reset (RST) to the device will also set the TBRE output, TBRE is cleared (low) whenever data is written to the TBR.

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
RST	I	RESET: The RST input forces the device into an "idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART State Register (USR) is cleared except for the TBRE and TC bits, which are set. The device remains in an "idle" state until programmed to resume serial data activities. The RST inputs is a Schmitt triggered input.
INTR	O	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic.
SDI	I	SERIAL DATA INPUT: Serial data input to the device receiver circuits. A mark (1) is high, and a space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
DR	O	DATA READY: A true level indicates that a character has been received, transferred to the RBR, and is ready for transfer to the CPU, DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
V _{DD}		V _{DD} : +5 V positive power supply pin. A 0.1 μF decoupling capacitor from v _{DD} (pin 27) to GND (pin 16) is recommended.
$\overline{\text{CS0}}$	I	CHIP SELECT: The chip select input acts as an enable signal the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ input signals.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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DATE: 25-06-09

Approved sources of supply for SMD 5962-95817 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number <u>3/</u>	Vendor similar PIN <u>2/</u>
5962-9581701VXC	<u>3/</u>	MD85C52/7

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE
number

34371

Vendor name
and address

Renesas Electronics America, Inc.
1650 Robert J. Conlan Blvd NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.