REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R187-97	97-02-24	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 and updated appendix A. Editorial changes throughout. - tmh	00-10-16	Thomas M. Hess
C	Correct title to more accurately describe the function. Update the radiation features in section 1.5 and paragraphs 4.4.41, 4.4.4.4, and 4.4.4.3. Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. Change footer address. - jak	09-07-27	Thomas M. Hess
D	Update radiation features in section 1.5 and add SEP table IB. Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - MAA	17-02-13	Thomas M. Hess
E	Remove Class M requirement. Updated source of supply (Cage 34371) Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jwc	23-11-27	Muhammad Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	E	E	E																			
SHEET	23	24	25																			
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

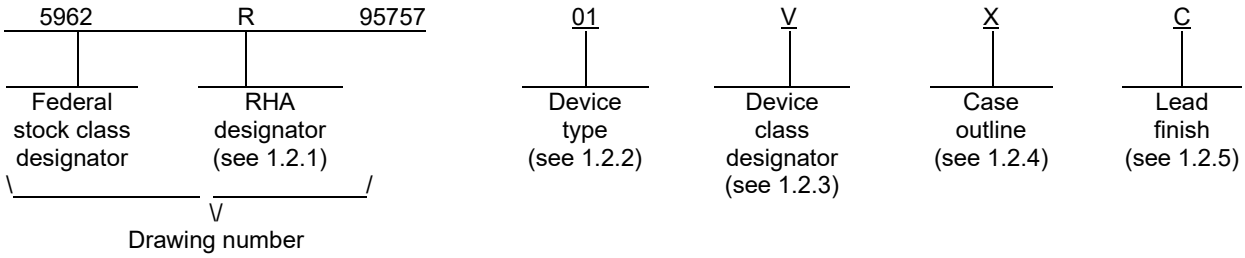
STANDARD MICROCIRCUIT DRAWING	PREPARED BY Joseph A. Kerby CHECKED BY Thanh V. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 95-10-20	MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, RADIATION HARDENED, SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL E	SIZE A	CAGE CODE **67268**	**5962 - 95757**
		SHEET 1 OF 25		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HCTS193	Radiation hardened, SOS, high speed CMOS, synchronous 4-bit binary up/down counter, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line package
X	CDFP4-F16	16	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input current, any one input (I_{IN})	±10 mA
DC output current, any one output (I_{OUT})	±25 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline E	24°C/W
Case outline X	29°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case outline E	73°C/W
Case outline X	114°C/W
Junction temperature (T_J)	+175°C
Maximum package power dissipation at T_A = +125°C (P_D): 4/	
Case outline E	0.68 W
Case outline X	0.44 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	V_{CC}/2
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise and fall time at V_{CC} = 4.5 V (t_r, t_f)	500 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 Rad (Si)/s)	200K Rad(Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.2)	≤ 100 MeV/(mg/cm^2) 5/
No SEU occurs at effective LET (see 4.4.4.2)	≤ 100 MeV/(mg/cm^2) 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:

Case E	13.7 mW/°C
Case X	8.8 mW/°C

5/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveform and test circuit. The switching waveforms and test circuits shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test V_{IH} = 2.25 V or V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 µA	All	4.5 V	1, 2, 3	4.40		V
		For all inputs affecting output under test V_{IH} = 2.25 V or V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 µA	All	5.5 V	1, 2, 3	5.40		
Low level output voltage	V_{OL}	For all inputs affecting output under test V_{IH} = 2.25 V or V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	All	4.5 V	1, 2, 3		0.1	V
		For all inputs affecting output under test V_{IH} = 2.25 V or V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	All	5.5 V	1, 2, 3		0.1	
Input current high	I_{IH}	For input under test, V_{IN} = 5.5 V For all other inputs V_{IN} = V_{CC} or GND	All	5.5 V	1		+0.5	µA
					2, 3		+5.0	
		M, D, P, L, R 2/	All		1		+5.0	
Input current low	I_{IL}	For input under test, V_{IN} = GND For all other inputs V_{IN} = V_{CC} or GND	All	5.5 V	1		-0.5	µA
					2, 3		-5.0	
		M, D, P, L, R 2/	All		1		-5.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Output current high (Source)	I_{OH}	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs V_{IN} = V_{CC} or GND V_{OUT} = 4.1 V	All	4.5 V	1	-4.8		mA
					2, 3	-4.0		
		M, D, P, L, R 2/	All		1	-4.0		
Output current low (Sink)	I_{OL}	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs V_{IN} = V_{CC} or GND V_{OUT} = 0.4 V	All	4.5 V	1	4.8		mA
					2, 3	4.0		
		M, D, P, L, R 2/	All		1	4.0		
Quiescent supply current delta, TTL input levels	ΔI_{CC} 4/	For inputs under test V_{IN} = V_{CC} - 2.1 V For all other inputs V_{IN} = V_{CC} or GND	All	5.5 V	1, 2, 3		1.6	mA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND	All	5.5 V	1		40	µA
					2, 3		750	
		M, D, P, L, R 2/	All		1		750	
Input capacitance	C_{IN}	V_{IH} = 5.0 V, V_{IL} = 0.0 V f = 1 MHz, see 4.4.1c	All	5.0 V	4		10	pF
Power dissipation capacitance	C_{PD} 5/		All	5.0 V	4		53	pF
					5, 6		75	
Functional test	6/	V_{IH} = 2.25 V, V_{IL} = 0.8 V See 4.4.1b	All	4.5 V	7, 8	L	H	
		M, D, P, L, R 2/	All		7	L	H	
Propagation delay time, CPU to Qn	t_{PHL1} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	35.0	ns
					10, 11	2.0	41.0	
		M, D, P, L, R 2/	All		9	2.0	41.0	
	t_{PLH1} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	29.0	ns
					10, 11	2.0	34.0	
		M, D, P, L, R 2/	All		9	2.0	34.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Propagation delay time, CPD to Qn	t_{PHL2} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	36.0	
					10, 11	2.0	42.0	
		M, D, P, L, R 2/			9	2.0	42.0	
	t_{PLH2} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	31.0	
					10, 11	2.0	36.0	
		M, D, P, L, R 2/			9	2.0	36.0	
Propagation delay time, CPU to TCU	t_{PHL3} 8/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	27.0	ns
					10, 11	2.0	35.0	
		M, D, P, L, R 2/ 8/			9	2.0	35.0	
	t_{PLH3} 8/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	27.0	ns
					10, 11	2.0	35.0	
		M, D, P, L, R 2/ 8/			9	2.0	35.0	
Propagation delay time, CPD to TCD	t_{PHL4} 8/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	27.0	ns
					10, 11	2.0	35.0	
		M, D, P, L, R 2/ 8/			9	2.0	35.0	
	t_{PLH4} 8/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	27.0	ns
					10, 11	2.0	35.0	
		M, D, P, L, R 2/ 8/			9	2.0	35.0	
Propagation delay time, PL to Qn	t_{PHL5} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	45.0	ns
					10, 11	2.0	53.0	
		M, D, P, L, R 2/ 8/			9	2.0	53.0	
	t_{PLH5} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	32.0	ns
					10, 11	2.0	36.0	
		M, D, P, L, R 2/ 8/			9	2.0	36.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, MR to Qn	t_{PHL6} 7/	C_L = 50 pF R_L = 500Ω See figure 4 M, D, P, L, R 2/ 8/	All	4.5 V	9	2.0	37.0	ns
					10, 11	2.0	44.0	
					9	2.0	44.0	
Output transition time	t_{THL}, t_{TLH} 9/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	2.0	15.0	ns
					10, 11	2.0	22.0	
Maximum clock frequency, CPU, CPD	f_{MAX} 9/		All	4.5 V	9	22.0		MHz
					10, 11	15.0		
Setup time, high or low, Pn to PL	t_s 9/		All	4.5 V	9	15.0		ns
					10, 11	22.0		
Hold time, high or low, Pn to PL	t_{h1} 9/		All	4.5 V	9	0.0		ns
					10, 11	0.0		
Hold time, high or low, CPD to CPU or CPU to CPD	t_{h2} 9/		All	4.5 V	9	16.0		ns
					10, 11	24.0		
CPU or CPD pulse width, high or low	t_{w1} 9/		All	4.5 V	9	23.0		ns
					10, 11	35.0		
PL pulse width, low	t_{w2} 9/		All	4.5 V	9	16.0		ns
					10, 11	24.0		
MR pulse width, high	t_{w3} 9/		All	4.5 V	9	20.0		ns
					10, 11	30.0		
Recovery time, PL to CPU or CPD	t_{REC1} 9/		All	4.5 V	9	15.0		ns
					10, 11	22.0		
Recovery time, MR to CPU or CPD	t_{REC2} 9/		All	4.5 V	9	5.0		ns
					10, 11	5.0		

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} and ΔI_{CC} tests, the output terminals shall be open. When performing the I_{CC} and ΔI_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

TABLE IA. Electrical performance characteristics - Continued.

2/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, this device is only tested at the R level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I herein.

5/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$

f is the frequency of the input signal; n is the number of device inputs at TTL levels; and d is the duty cycle of the input signal.

6/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V.

7/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V. For propagation delay tests, all paths must be tested.

8/ This parameter is guaranteed but not tested. This parameter will be changed at a later date to be listed as a 100 percent tested parameter.

9/ This parameter is guaranteed but not tested. This parameter is characterized upon initial design or process changes which affect this characteristic.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	V_{CC} = 4.5 V	Bias V_{CC} = 5.0 V
	Effective LET no upsets	Effective LET no SEL occurs
All	LET ≤ 100 MeV/(mg/cm^2)	LET ≤ 100 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at worst case temperature, T_A = +25°C ±10°C and for SEL worst case temperature, T_A = +125°C ±10°C.

Device type	01
Case outlines	E and X
Terminal number	Terminal symbol
1	P1
2	Q1
3	Q0
4	CPD
5	CPU
6	Q2
7	Q3
8	GND
9	P3
10	P2
11	PL
12	TCU
13	TCD
14	MR
15	P0
16	V_{CC}

FIGURE 1. Terminal connections.

Inputs				Function
MR	CPU	CPD	PL	
L	↑	H	H	Count up
L	H	↑	H	Count down
H	X	X	X	Reset
L	X	X	L	Load preset inputs

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-high clock transition

FIGURE 2. Truth table.

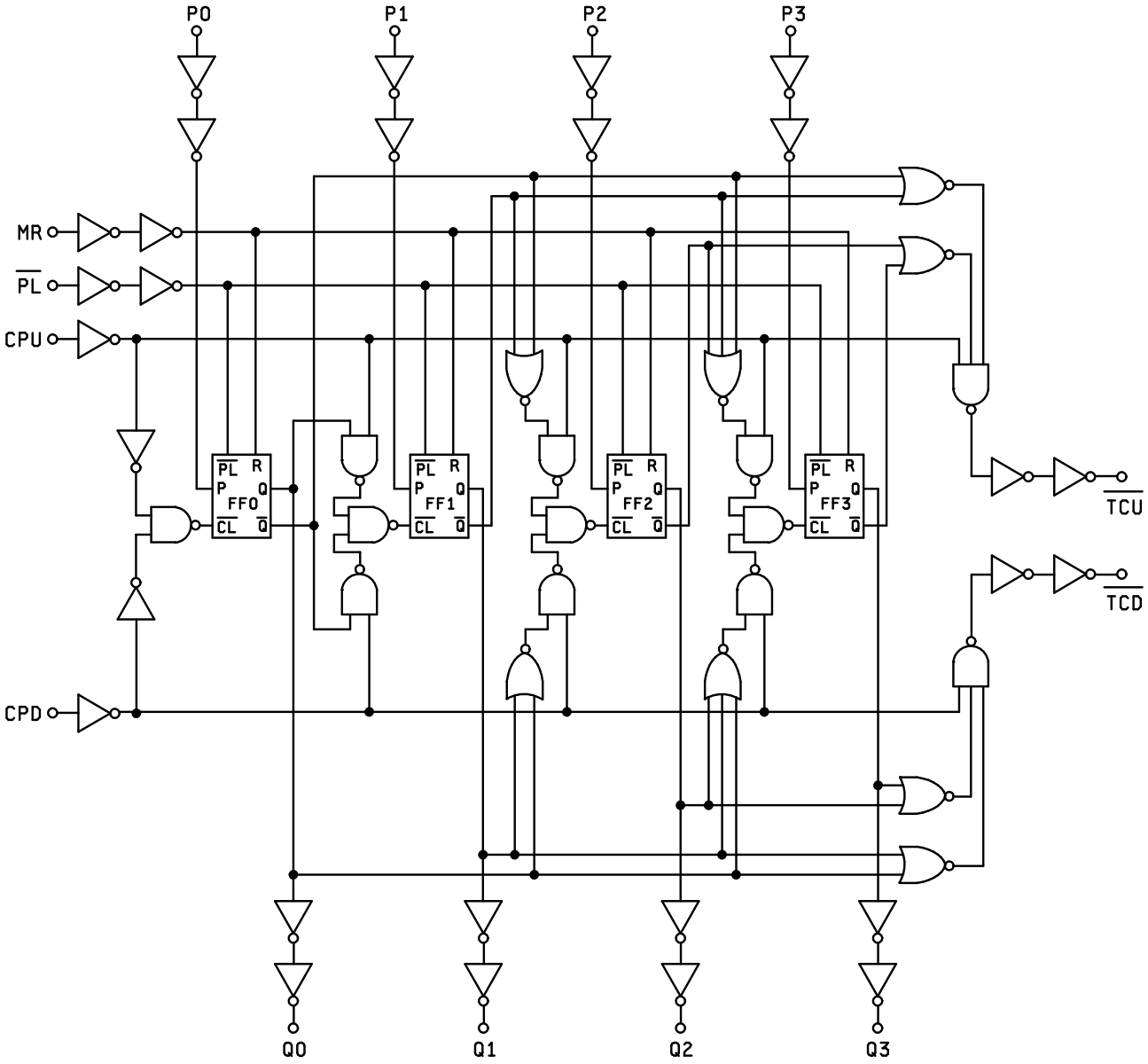


FIGURE 3. Logic diagram.

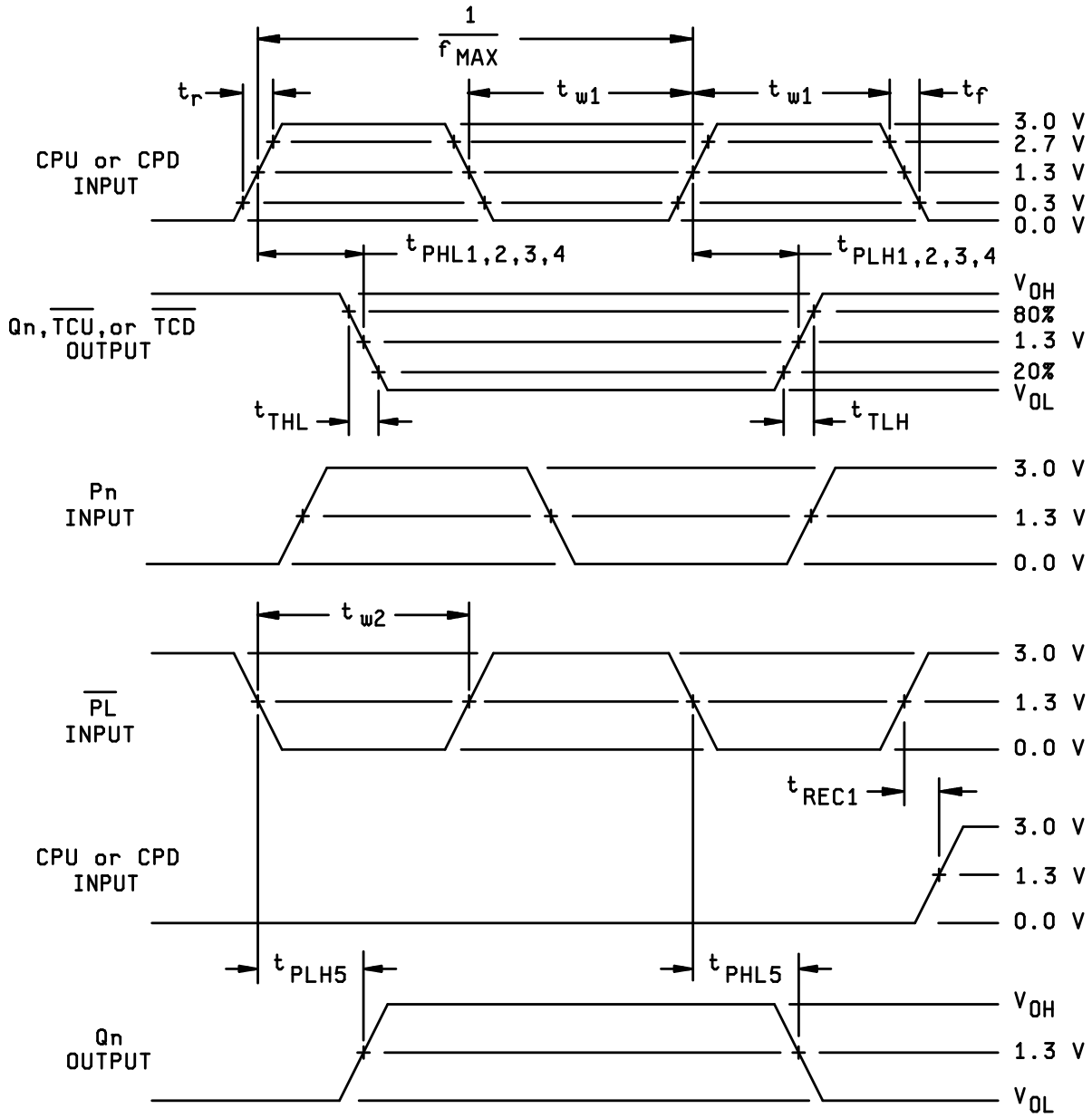
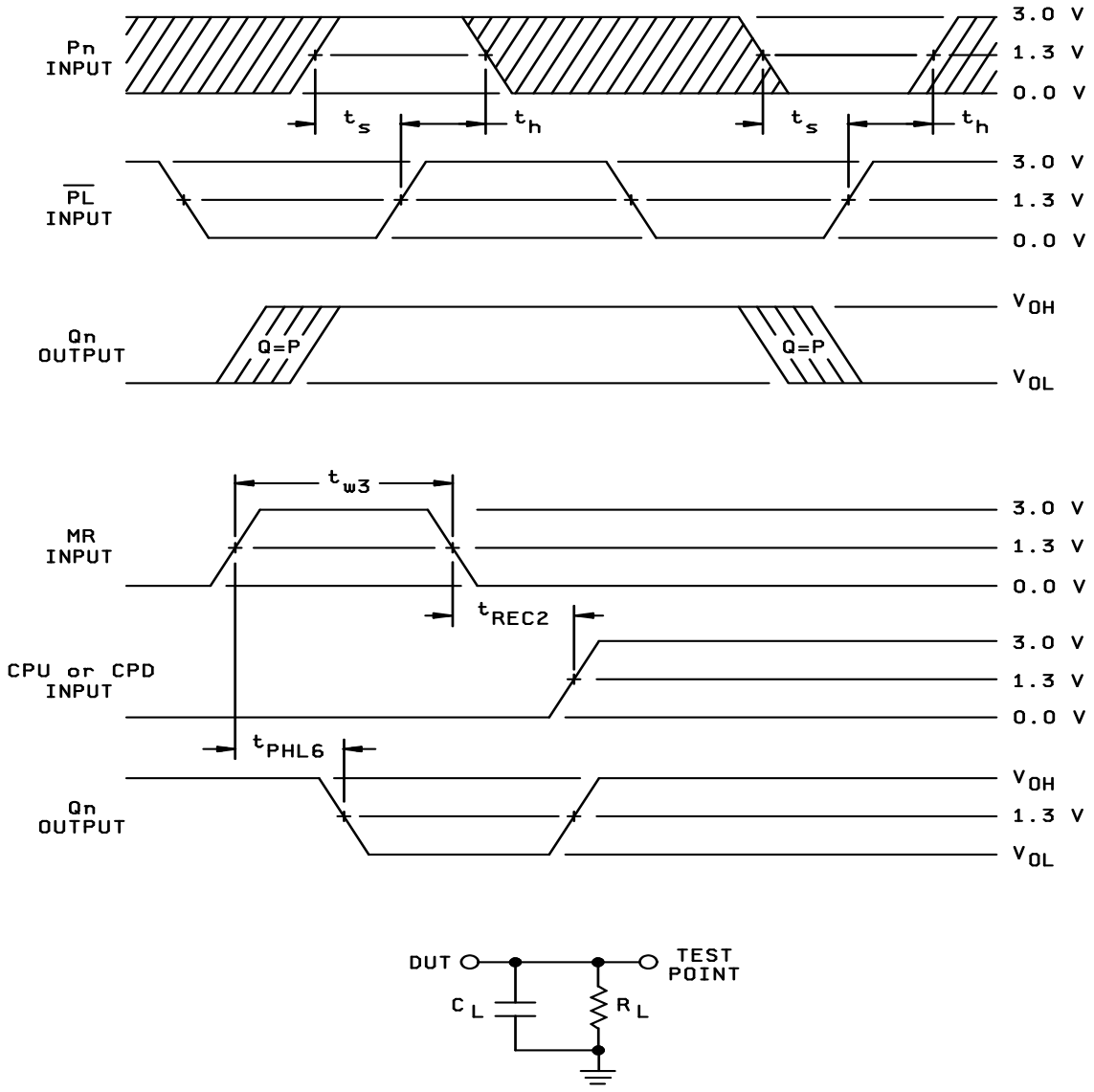


FIGURE 4. Switching waveforms and test circuit.



NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).

c. Subgroup 4, 5 and 6 (C_{IN} and C_{PD} measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD} the tests shall be sufficient to validate the limits defined in table I herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with | MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7, 9 and deltas.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see Table I)

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameters 1/	Delta limits
I_{CC}	+12.0 μA
I_{OL}/I_{OH}	-15%

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019,condition A and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class T and V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.
c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
d. The particle range shall be ≥ 20 microns in silicon.
e. The upset test temperature shall be +25°C. The latchup test temperature shall be at the maximum rated operating temperature ±10°C for the latchup measurements.
f. Bias conditions shall be defined by the manufacturer for latchup measurements.
g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be as specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

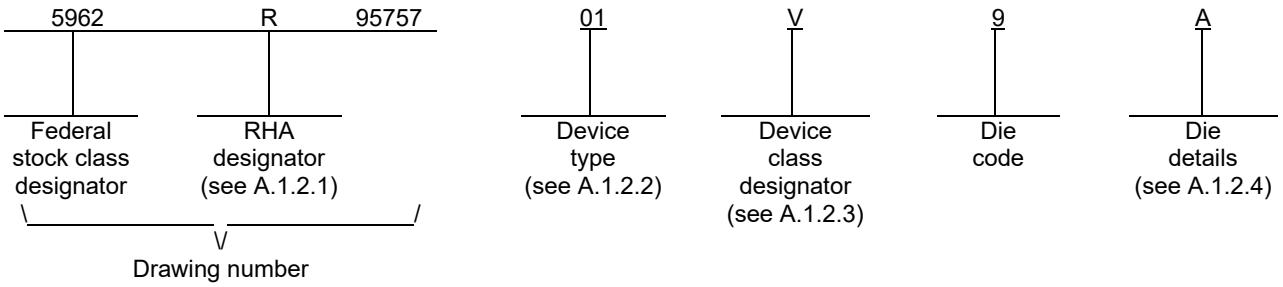
a. RHA test conditions of SEP.
b. Number of upsets (SEU).
c. Number of transients (SET).
d. Occurrence of latch-up (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95757

A.1. SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN shall be as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HCTS193	Radiation hardened, SOS, high speed CMOS, synchronous 4-bit binary up/down counter, TTL compatible inputs.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die Physical dimensions.

Die Types	Figure number
01	A-1

A.1.2.4.2 Die Bonding pad locations and Electrical functions.

Die Types	Figure number
01	A-1

A.1.2.4.3 Interface Materials.

Die Types	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die Types	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

A.2 APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined within paragraph 3.2.3 of the body of this document.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

A.3.3 Electrical performance characteristics and post- irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 TM 5007.

b) 100% wafer probe (see paragraph A.3.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 TM2010 or the alternate procedures allowed within MIL-STD-883 TM5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

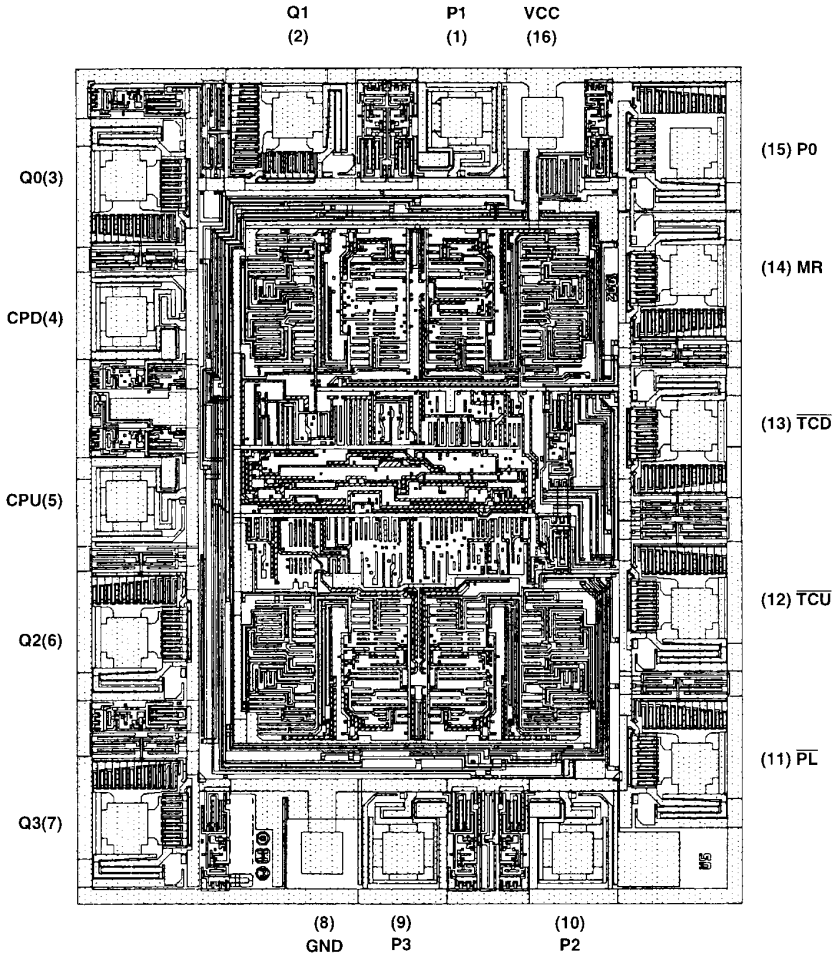
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95757

The following metallization diagram supplies the locations and electrical functions of the bonding pads. The internal metallization layout and alphanumeric information contained within this diagram may or may not represent the actual circuit defined by this SMD.



NOTE: Pad numbers reflect terminal numbers when placed in Case Outlines E, X (see Figure 1).

FIGURE A-1 Die bonding pad locations and electrical functions

o DIE PHYSICAL DIMENSIONS

Die Size:	2190 x 2650 microns.
Die Thickness:	21 +/- 2 mils.

o INTERFACE MATERIALS

Top Metallization:	Si Al
Thickness	11.0kÅ ± 1kÅ
Backside Metallization	None
Glassivation	
Type:	SiO2
Thickness	13.0kÅ ± 2.6kÅ
Substrate:	Silicon on Sapphire (SOS)

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Insulator
Special assembly	
instructions:	Bond pad #16 (V_{CC}) first.

FIGURE A-1 Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-11-27

Approved sources of supply for SMD 5962-95757 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9575701VXC	34371	HCTS193KMSR
5962R9575701VEC	3/	HCTS193DMSR
5962R9575701V9A	3/	HCTS193HMSR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406