REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R001-99	98-10-8	R. Monnin
B	Change conditions for input leakage current an overvoltage leakage current in table I. Editorial changes throughout. - lgt	99-02-24	R. Monnin
C	Make change to descriptive designator as specified in 1.2.4. - ro	99-04-28	R. Monnin
D	Make changes to access time and enable delay waveforms as specified under figure 3. - ro	00-07-19	R. Monnin
E	Redraw. Update drawing to current requirements. - drw	10-11-09	Charles F. Saffle
F	Update paragraphs to MIL-PRF-38535 requirements. - drw	19-07-18	Charles F. Saffle

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
96-02-27

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, RADIATION HARDENED CMOS, MULTIPLEXER/DEMULTIPLEXER WITH ACTIVE OVERVOLTAGE PROTECTION, MONOLITHIC SILICON

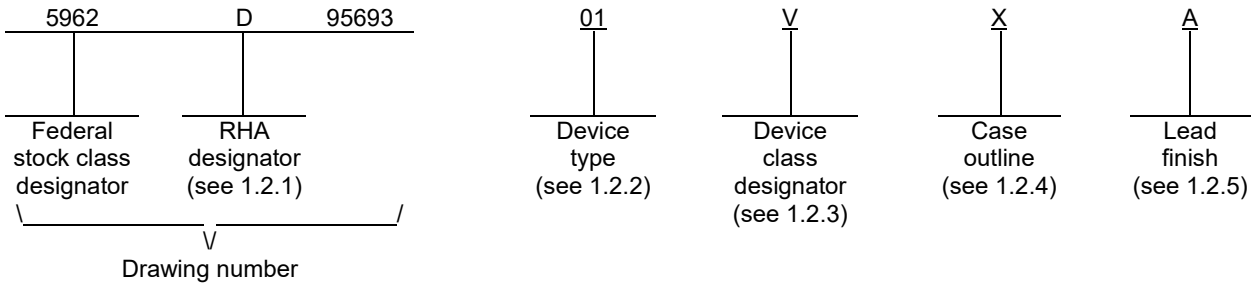
SIZE	CAGE CODE	
A	**67268**	**5962-95693**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS546RH	Radiation hardened DI single 16-channel MUX/DEMUX with active overvoltage protection
02	HS547RH	Radiation hardened DI differential 8-channel MUX/DEMUX with active overvoltage protection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage between +V and -V	+44 V
Supply voltage between +V and ground	+22 V
Supply voltage between -V and ground	-25 V
Digital input overvoltage	
$+V_{EN}$, $+V_A$	$+V_{SUPPLY}$ + 4 V
$-V_{EN}$, $-V_A$	$-V_{SUPPLY}$ – 4 V
Analog input overvoltage	
$+V_S$	$+V_{SUPPLY}$ + 20 V
$-V_S$	$-V_{SUPPLY}$ – 20 V
Continuous current, S or D	
(pulsed at 1 ms, 10 percent duty cycle max)	40 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation at T_A = 125°C (P_D)	1 W 2/
Thermal resistance, junction-to-case (θ_{JC})	18°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	50°C/W
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Operating supply voltage ($\pm V_{SUPPLY}$)	±15 V
Analog input voltage (V_S)	$\pm V_{SUPPLY}$
Logic low level (V_{AL})	0 V to +0.8 V
Logic high level (V_{AH})	+4 V to $+V_{SUPPLY}$
Max RMS current, S or D	8 mA
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	10 Krads (Si)
Dose rate upset (20 ns pulse)	3/
Dose rate burnout	3/
Dose rate latch-up	4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the rate of 20 mW/°C for case outline X.
3/ Values to be specified when testing is completed.
4/ Devices use dielectrically isolated (DI) technology and latch-up is not physically possible.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $-V = -15$ V, $+V = +15$ V V_{REF} = OPEN, V_{EN} = 4.0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3	01, 02	-1.0	1.0	µA
	I_{IL}				-1.0	1.0	
	I_{IH}, I_{IL}	M, D 2/	1		-1.0	1.0	
Leakage current into the source terminal of an “OFF” switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V, All unused inputs = -10V, V_D = -10 V	1	01, 02	-10	+10	nA
			2, 3		-50	+50	
		V_{EN} = 0.5 V, M, D 2/	1		-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V, All unused inputs = +10V, V_D = +10 V	1	01, 02	-10	+10	
			2, 3		-50	+50	
		V_{EN} = 0.5 V, M, D 2/	1		-50	+50	
Leakage current into the drain terminal of an “OFF” switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V, All unused inputs = -10 V	1	01, 02	-10	+10	nA
			2, 3	01	-300	+300	
				02	-200	+200	
		V_{EN} = 0.5 V M, D 2/	1	01	-300	+300	
				02	-200	+200	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V, All unused inputs = +10 V	1	01, 02	-10	+10	nA
			2, 3	01	-300	+300	
				02	-200	+200	
		V_{EN} = 0.5 V M, D 2/	1	01	-300	+300	
				02	-200	+200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ -V = -15 V, +V = +15 V V_{REF} = OPEN, V_{EN} = 4.0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V, All unused inputs = -10 V	1	01, 02	-10	+10	nA
			2, 3	01	-300	+300	
				02	-200	+200	
		V_{EN} = 4.5 V M, D 2/	1	01	-300	+300	
				02	-200	+200	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V, All unused inputs = +10 V	1	01, 02	-10	+10	nA
			2, 3	01	-300	+300	
				02	-200	+200	
		V_{EN} = 4.5 V M, D 2/	1	01	-300	+300	
				02	-200	+200	
Overvoltage protected leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$ OVER VOLTAGE	V_S = 33 V, V_D = 0 V, V_{EN} = 0.8 V	1, 2, 3	01, 02	-2	+2	µA
		V_{EN} = 0.5 V M, D 2/	1		-5	+5	
	$-I_{D(OFF)}$ OVER VOLTAGE	V_S = -33 V, V_D = 0 V, V_{EN} = 0.8 V	1, 2, 3		-2	+2	
		V_{EN} = 0.5 V M, D 2/	1		-5	+5	
Positive supply current	+I	V_A = 0 V	1, 2, 3	01, 02		2.0	mA
		V_{EN} = 4.5 V M, D 2/	1			2.0	
Negative supply current	-I	V_A = 0 V	1, 2, 3	01, 02		-1.0	mA
		V_{EN} = 4.5 V M, D 2/	1			-1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $-V = -15$ V, $+V = +15$ V V_{REF} = OPEN, $V_{EN} = 4.0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Standby positive supply current	$+I_{SBY}$	$V_A = 0$ V, $V_{EN} = 0$ V	1, 2, 3	01, 02		2.0	mA
		M, D 2/	1			2.0	
Standby negative supply current	$-I_{SBY}$	$V_A = 0$ V, $V_{EN} = 0$ V	1, 2, 3	01, 02		-1.0	mA
		M, D 2/	1			-1.0	
Switch "ON" resistance	$+R_{DS1}$	$V_S = 10$ V, $I_D = -100$ µA	1	01, 02		1500	Ω
			2, 3			1800	
		$V_{EN} = 4.5$ V M, D 2/	1			1800	
	$-R_{DS1}$	$V_S = -10$ V, $I_D = +100$ µA	1	01, 02		1500	Ω
			2, 3			1800	
		$V_{EN} = 4.5$ V M, D 2/	1			1800	
Difference in switch "ON" resistance between channels	$+\Delta R_{DS1}$	$\frac{((+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100)}{+R_{DS1}AVE}$	1	01, 02		7	%
		$V_{EN} = 4.5$ V M, D 2/	1			7	
	$-\Delta R_{DS1}$	$\frac{((-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100)}{-R_{DS1}AVE}$	1	01, 02		7	%
		$V_{EN} = 4.5$ V M, D 2/	1			7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ -V = -15 V, +V = +15 V V_{REF} = OPEN, V_{EN} = 4.0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic level voltage	V_{AL1}	3/, 4/	1, 2, 3	01, 02		0.8	V
		V_{EN} = 4.5 V M, D 2/	1			0.5	
	V_{AH1}		1, 2, 3		4.0		
		V_{EN} = 4.5 V M, D 2/	1		4.5		
	V_{AL2}	5/	1, 2, 3	01, 02		0.8	V
		V_{EN} = 4.5 V M, D 2/	1			0.5	
	V_{AH2}		1, 2, 3		6.0		
		V_{EN} = 4.5 V M, D 2/	1		6.5		
Capacitance : Address	C_A	V+ = V- = 0 V, F = 1 MHz, T_A = +25°C, See 4.4.1d 6/	4	01, 02		12	pF
Capacitance : Output switch	Cos	V+ = V- = 0 V, F = 1 MHz, T_A = +25°C, See 4.4.1d 6/	4	01		85	pF
				02		50	
Capacitance : Input switch	C_{IS}	V+ = V- = 0 V, F = 1 MHz, T_A = +25°C, See 4.4.1d 6/	4	01, 02		15	pF
Charge transfer error	V_{CTE}	V_S = GND, T_A = +25°C, V_{EN} = 0 V to 5 V 6/	4	01, 02		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, CL = 15 pF, V_S = 7 V_{rms}, F = 100 kHz, T_A = +25°C 6/, 7/	4	01, 02	-50		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ -V = -15 V, +V = +15 V V_{REF} = OPEN, V_{EN} = 4.0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test	FT	T_A = +25°C, See 4.4.1b	7, 8	01, 02			
Break-before-make time delay	t_D	R_L = 1 kΩ, See figure 3	9	01, 02	25		ns
			10, 11		5		
		M, D 2/	9		5		
Propagation delay times : Address inputs to I/O channels times :	t_A	R_L = 10 kΩ, See figure 3	9	01, 02		500	ns
			10, 11			1000	
		M, D 2/	9			1000	
Enable to I/O	$T_{ON(EN)}$	R_L = 1 kΩ, See figure 3	9	01, 02		500	ns
			10, 11			1000	
		M, D 2/	9			1000	
	$T_{OFF(EN)}$	R_L = 1 kΩ, See figure 3	9	01, 02		500	ns
			10, 11			1000	
		M, D 2/	9			1000	

1/ Input current of one input mode.
2/ Devices supplied to this drawing meet levels M and D of irradiation. However, these devices are only tested at the D level. Pre and post irradiation values are identical unless otherwise specified in Table I.
3/ Used for forcing conditions for all DC tests, unless otherwise specified.
4/ To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0 V supply recommended.
5/ V_{REF} = +10 V.
6/ Guaranteed, if not tested, to the limits as specified.
7/ Worst case isolation occurs on channel 8B due to proximity of the output pins.

Case outline	X	
Device type	01	02
Terminal number	Terminal symbol	
1	V+	V+
2	NC	OUT B
3	NC	NC
4	IN 16	IN 8B
5	IN 15	IN 7B
6	IN 14	IN 6B
7	IN 13	IN 5B
8	IN 12	IN 4B
9	IN 11	IN3B
10	IN 10	IN 2B
11	IN 9	IN 1B
12	GND	GND
13	V_{REF}	V_{REF}
14	A3	NC
15	A2	A2
16	A1	A1
17	A0	A0
18	ENABLE	ENABLE
19	IN 1	IN 1A
20	IN 2	IN 2A
21	IN 3	IN 3A
22	IN 4	IN 4A
23	IN 5	IN 5A
24	IN 6	IN 6A
25	IN 7	IN 7A
26	IN 8	IN 8A
27	V-	V-
28	OUT	OUT A

FIGURE 1. Terminal connections.

Device type 01

A3	A2	A1	A0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

Device type 02

A2	A1	A0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

FIGURE 2. Truth tables.

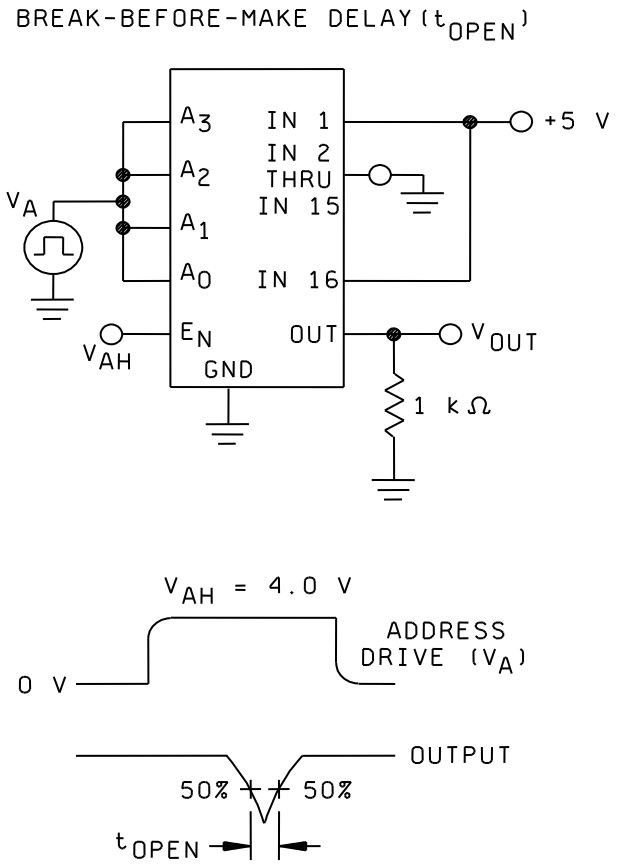


FIGURE 3. Timing diagrams.

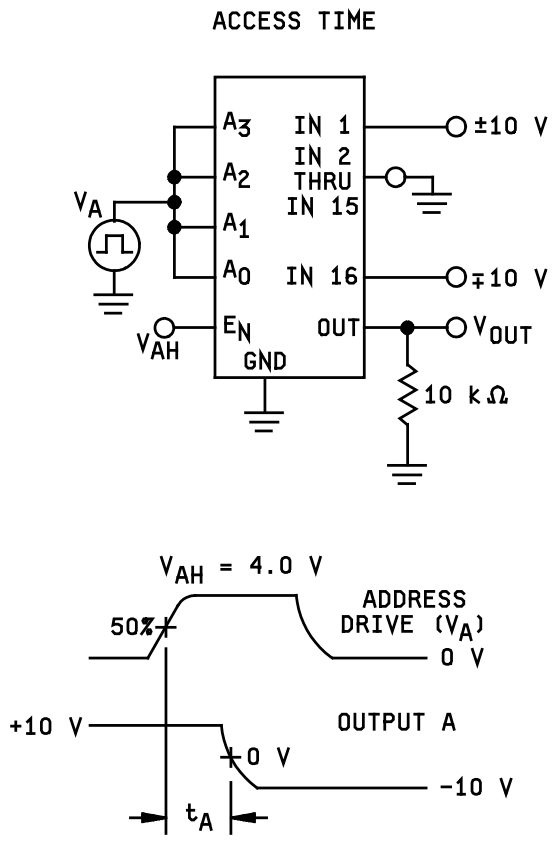


FIGURE 3. Timing diagrams - continued.

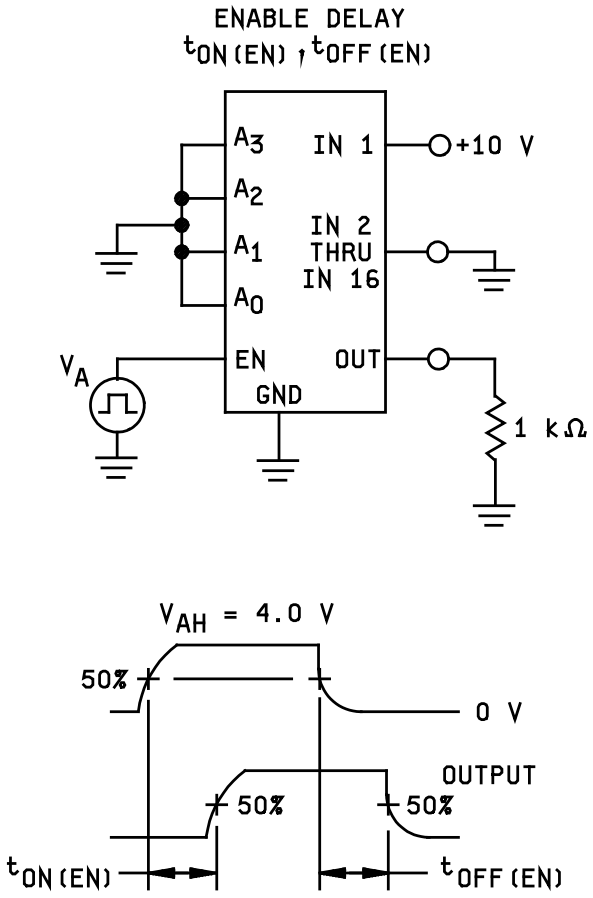


FIGURE 3. Timing diagrams - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Subgroup 4 (C_A, C_{IS}, and C_{OS}, measurements) should be measured only for initial qualification and after any process or design changes which may affect input or output capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/, 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11 3/	1, 2, 3, 4, 7, 8, 9, 10, 11 3/
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1. For class V to subgroups 1 and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed With reference to the zero hour electrical parameters (see table I).
3/ Subgroup 4, if not tested, shall be guaranteed to the limits specified in table I.

TABLE IIB. Burn-in delta parameters (+25°C) and group C delta parameters.

Parameters	Symbol	Delta limits
Leakage current into the source terminal of an "OFF" switch	$I_{S(OFF)}$	±10 nA
Leakage current into the drain terminal of an "OFF" switch	$I_{D(OFF)}$	±10 nA
Leakage current from an "ON" driver into the switch (drain and source)	$I_{D(ON)}$	±10 nA
Switch on resistance	10 V R_{DS}	±150Ω
Positive supply current	I+	±200 μA
Negative supply current	I-	±100 μA
Positive standby supply current	$+I_{SBY}$	±200 μA
Negative standby supply current	$-I_{SBY}$	±100 μA
Input leakage current Address or Enable pins	I_{AL}, I_{AH}	±100 nA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1023 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Dose rate burnout. When required by the customer, test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

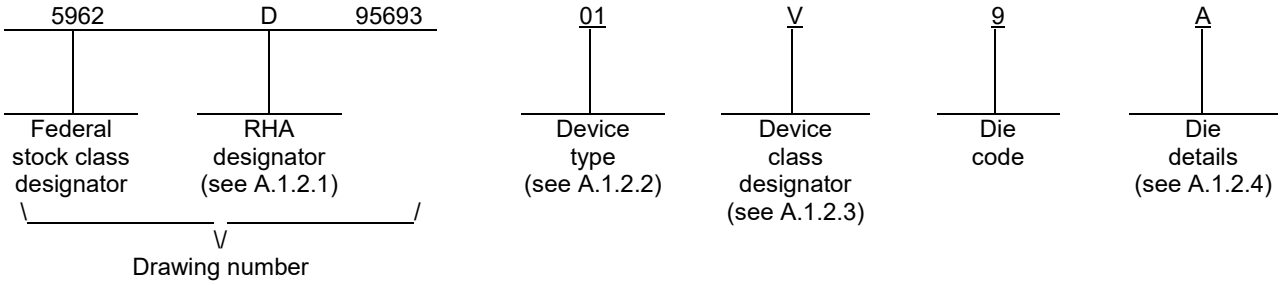
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95693

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS546RH	Radiation hardened DI single 16-channel MUX/DEMUX with overvoltage protection.
02	HS547RH	Radiation hardened, DI differential 8-channel MUX/DEMUX with active overvoltage protection.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1 and A2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1 and A2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1 and A2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1 and A2.

A.3.2.5 Truth tables. The truth tables shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3 and 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

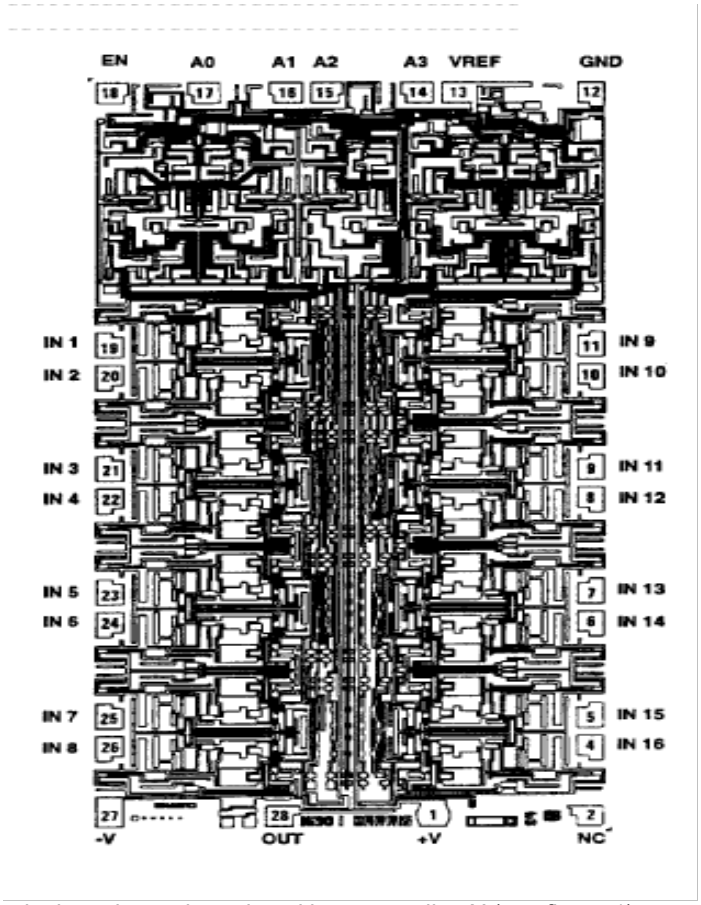
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

Die bonding pad locations and electrical functions



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
Die size: 2130 X 4030 microns.
Die thickness: 20 +/-1 mils.

Interface materials.
Top metallization: CuAl 15.0 kÅ - 17.0 kÅ
Backside metallization: None or Gold backed.

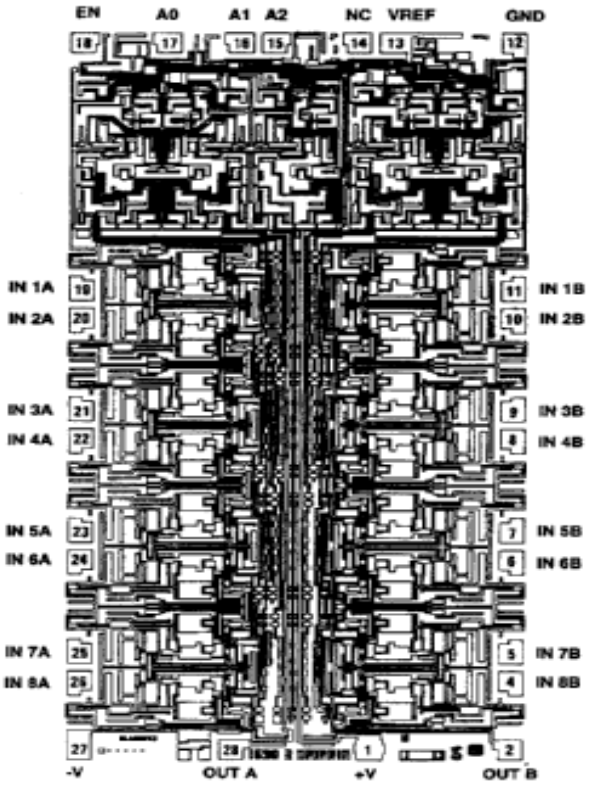
Glassivation.
Type: Nitride.
Thickness: 7.0 kÅ +/- 0.7 kÅ.

Substrate: Dielectrically Isolated (DI).

Assembly related information.
Substrate potential: Insulator.
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
Die size: 2130 X 4030 microns.
Die thickness: 20 +/-1 mils.

Interface materials.
Top metallization: CuAl 15.0 kÅ - 17.0 kÅ
Backside metallization: None or Gold backed.

Glassivation.
Type: Nitride.
Thickness: 7.0 kÅ +/- 0.7 kÅ.

Substrate: Dielectrically Isolated (DI).

Assembly related information.
Substrate potential: Insulator.
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-18

Approved sources of supply for SMD 5962-95693 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962D9569301VXA	3/	HS1-0546RH-Q
5962D9569301VXC	34371	HS1B-0546RH-Q
5962D9569301V9A	34371	HS0-0546RH-Q
5962D9569302VXA	3/	HS1-0547RH-Q
5962D9569302VXC	34371	HS1B-0547RH-Q
5962D9569302V9A	34371	HS0-0547RH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406