REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R044-96.	96-01-24	M.A. Frye
B	Changes in accordance with NOR 5962-R460-97.	97-09-22	Raymond Monnin
C	Update boilerplate for class “T” changes. - glg	98-12-02	Raymond Monnin
D	Correction of paragraph 1.5 Table I changes. - glg	99-06-24	Raymond Monnin
E	Correction of test condition voltage value for $\overline{E}$ in Table I for Operating supply current; V_{DD} was changed to GND. Removed neutron irradiation line from section 1.5. Update boilerplate. - ksr	04-02-12	Raymond Monnin
F	Update boilerplate paragraphs. - glg	10-03-04	Charles Saffle
G	Update to meet current MIL-PRF-38535 requirements. - glg	17-06-22	Charles Saffle
H	Update radiation features in section 1.5 and SEP table IB. Suppliers cage code information updated. Update boilerplate paragraphs throughout. - MAA	18-02-14	Charles Saffle

REV																				
SHEET																				
REV	H	H	H																	
SHEET	15	16	17																	

REV STATUS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
95-10-05

REVISION LEVEL
H

SIZE
A

CAGE CODE
67268

5962-95626

SHEET 1 OF 17

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
FOR USE BY ALL DEPARTMENTS
AND AGENCIES OF THE
DEPARTMENT OF DEFENSE

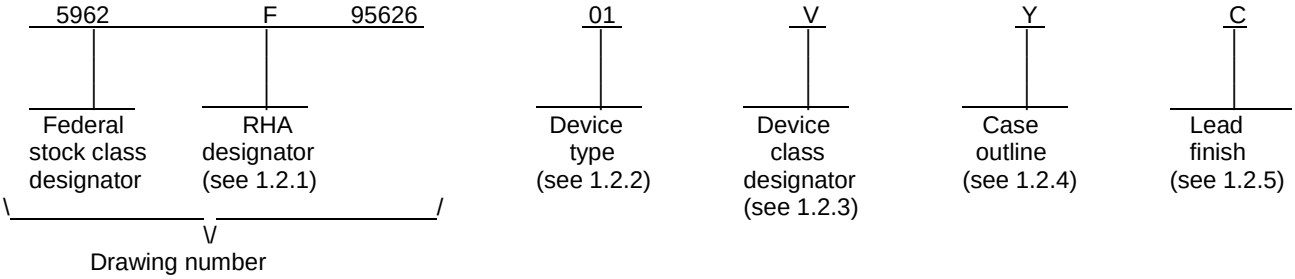
AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION HARDENED, CMOS, 8K X 8-BIT PROM, MONOLITHIC SILICON

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V), and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturers Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type 1/	Generic number 2/	Circuit function	Access time
01	HS-6664RH	8K X 8-bit Radiation hardened PROM	65 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line package
Y	CDFP3-F28	28	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q, T and V.

1/ Device is available in an unprogrammed state only.
2/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 3/

Supply voltage range	-0.3 V dc to +7.0 V dc
Voltage on any pin with respect to ground	-0.3 V dc to V_{DD} +0.3 V dc
Maximum power dissipation (P_D)	1.75 W
Lead temperature (soldering, 10 seconds maximum)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0.0 V dc
Input high voltage (V_{IH})	+2.4 V dc minimum to V_{CC}
Input Low voltage (V_{IL})	0.0 V dc to +0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features

Maximum total dose available (dose rate = 50 - 300 Rad(Si)/s):

Class Q, and V	300K Rad(Si)
Class T	100K Rad(Si)

Single event phenomenon (SEP):

No SEU at effective LET (see 4.4.4)	$\leq$ 100 MeV-cm^2/mg 4/
Dose rate induced upset	5 x 10^8 Rad(Si)/sec 4/
Dose rate survivability	5 x 10^{11} Rad(Si)/sec 4/

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Limits are guaranteed by process or design but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ASTM INTERNARTIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

(Copies of this document are available online at https://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 247, Arlington, VA 22201).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535, and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Unprogrammed device delivered to the user. All testing shall be verified through final electrical testing as defined in 3.2.3.1 and table I. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -2.0 mA		1,2,3	All	3.5		V
			M,D, P,L, R,F	1 2/		3/		V
Output high voltage	V_{OH2}	V_{DD} = 4.5 V, I_{OH} = -100 µA		1,2,3	All	V_{DD} - 0.3		V
			M,D, P,L, R,F	1 2/		3/		V
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 4.8 mA		1,2,3	All		0.4	V
			M,D, P,L, R,F	1 2/			3/	V
Input leakage current	I_I	V_{DD} = 5.5 V, $\overline{P}$ not tested V_{IN} = GND or V_{DD}		1,2,3	All	-1.0	1.0	µA
			M,D, P,L, R,F	1 2/		3/	3/	µA
High impedance output leakage current	I_{OZ}	V_{DD} = 5.5 V, $\overline{E}$ = 5.5 V $V_{I/O}$ = GND or V_{DD}		1,2,3	All	-10	10	µA
			M,D, P,L, R,F	1 2/		3/	3/	µA
Operating supply current	I_{DDOP}	V_{DD} = 5.5 V, $\overline{E}$ = GND I_{OUT} = 0 mA, f = 1 MHz V_{IN} = GND or V_{DD} 4/		1,2,3	All		15	mA
			M,D, P,L, R,F	1 2/			3/	mA
Standby supply current	I_{DDSB}	V_{DD} = 5.5 V, I_{OUT} = 0 mA V_{IN} = GND or V_{DD}		1,2,3	All		500	µA
			M,D, P,L, R,F	1 2/			3/	µA
Input capacitance 5/	C_{IN}	V_{DD} = open, T_A = +25ºC, f = 1.0 MHz, see 4.4.1c		4	All		15	pF
Output capacitance 5/	C_{OUT}	V_{DD} = open, T_A = +25ºC, f = 1.0 MHz, see 4.4.1c		4	All		12	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Functional tests		See 4.4.1d, V_{DD} = 4.5 V f = 1 MHz, V_{IH} = 2.4 V V_{IL} = 0.45 V, I_{OH} = -1.0 mA I_{OL} = 1.0 mA, $V_{OH} \ge$ 1.5 V $V_{OL} \le$ 1.5 V		7,8A,8B	All			
			M,D, P,L, R,F	7 2/		3/		
Address access time 7/	t_{AVQV}	See figure 4 6/ V_{DD} = 4.5V and 5.5V		9,10,11	All		65	ns
Address setup time	t_{AVEL}			9,10,11	All	5		ns
			M,D, P,L, R,F	9 2/		3/		ns
Address hold time	t_{ELAX}			9,10,11	All	12		ns
			M,D, P,L, R,F	9 2/		3/		ns
Chip enable access time	t_{ELQV}			9,10,11	All		60	ns
			M,D, P,L, R,F	9 2/			3/	ns
Output enable access time	t_{GLQV}			9,10,11	All		20	ns
			M,D, P,L, R,F	9 2/			3/	ns
Chip enable to output active 7/	t_{ELQX}			9,10,11	All	5		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Chip disable to output in high Z 7/	t_{EHQZ}	See figure 4 6/ V_{DD} = 4.5V and 5.5V		9,10,11	All		15	ns
Output enable to output active 7/	t_{GLQX}			9,10,11	All	5		ns
Output enable to output disable 7/	t_{GHQZ}			9,10,11	All		15	ns
Chip enable low width	t_{ELEH}			9,10,11	All	60		ns
			M,D, P,L, R,F	9 2/		3/		ns
Chip enable high width	t_{EHEL}			9,10,11	All	20		ns
			M,D, P,L, R,F	9 2/		3/		ns
Read cycle time	t_{ELEL}			9,10,11	All	80		ns
			M,D, P,L, R,F	9 2/		3/		ns

1/ All tests performed with $\overline{P}$ hardwired to V_{DD}.
2/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C. The M, D, P, L, R, and F in the test condition column are the postirradiation limits for the device types specified in the device types column. For classes Q, and V, devices are tested only at level "F"; for class T, devices are tested only at level "R" (see paragraph 1.5).
3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
4/ Typical derating = 15mA/MHz increase in operating supply current.
5/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
6/ AC measurements assume rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load = 1 TTL equivalent load and $C_L \ge 50$ pF (see figure 3).
7/ If not specifically tested, shall be guaranteed to the limits specified in table I.

TABLE IB. SEP test limits. 1/ 2/

Device type	Test	Bias V_{DD} = 4.5 V for SEU test 3/ No SEU observed at effective LET
All	No SEU	LET ≤ 100 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for worst case operating temperature T_A = +25°C ± 10°C for single event upset(SEU).

Device types	All
Case outlines	X,Y
Terminal number	Terminal symbol
1	NC
2	A_{12}
3	A_7
4	A_6
5	A_5
6	A_4
7	A_3
8	A_2
9	A_1
10	A_0
11	DQ_0
12	DQ_1
13	DQ_2
14	GND
15	DQ_3
16	DQ_4
17	DQ_5
18	DQ_6
19	DQ_7
20	$\overline{E}$
21	A_{10}
22	$\overline{G}$
23	A_{11}
24	A_9
25	A_8
26	NC
27	$\overline{P}$
28	V_{DD}

NOTES: NC = no connection; $\overline{P}$ must be hardwired at all times to V_{DD}, except during programming.

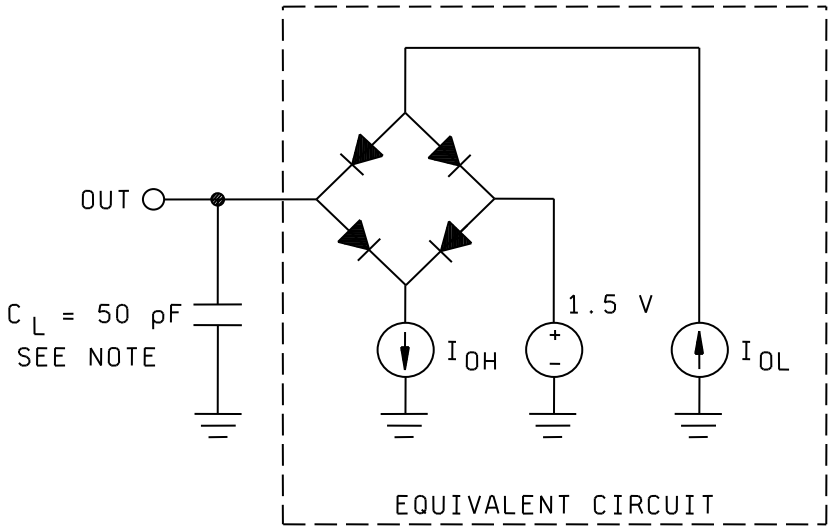
FIGURE 1. Terminal connections.

Read modes

Mode	$\overline{E}$	$\overline{G}$	Outputs
Read	L	L	Enabled
Output Disable	L	H	High Z
Standby	H	X	High Z

NOTES:
1. L = logic low voltage level; H = logic high voltage level; X can be H or L.
2. High Z is high impedance state.

FIGURE 2. Truth table.



NOTE: C_L = load capacitance and includes scope and jig capacitance.

FIGURE 3. Output load circuit or equivalent.

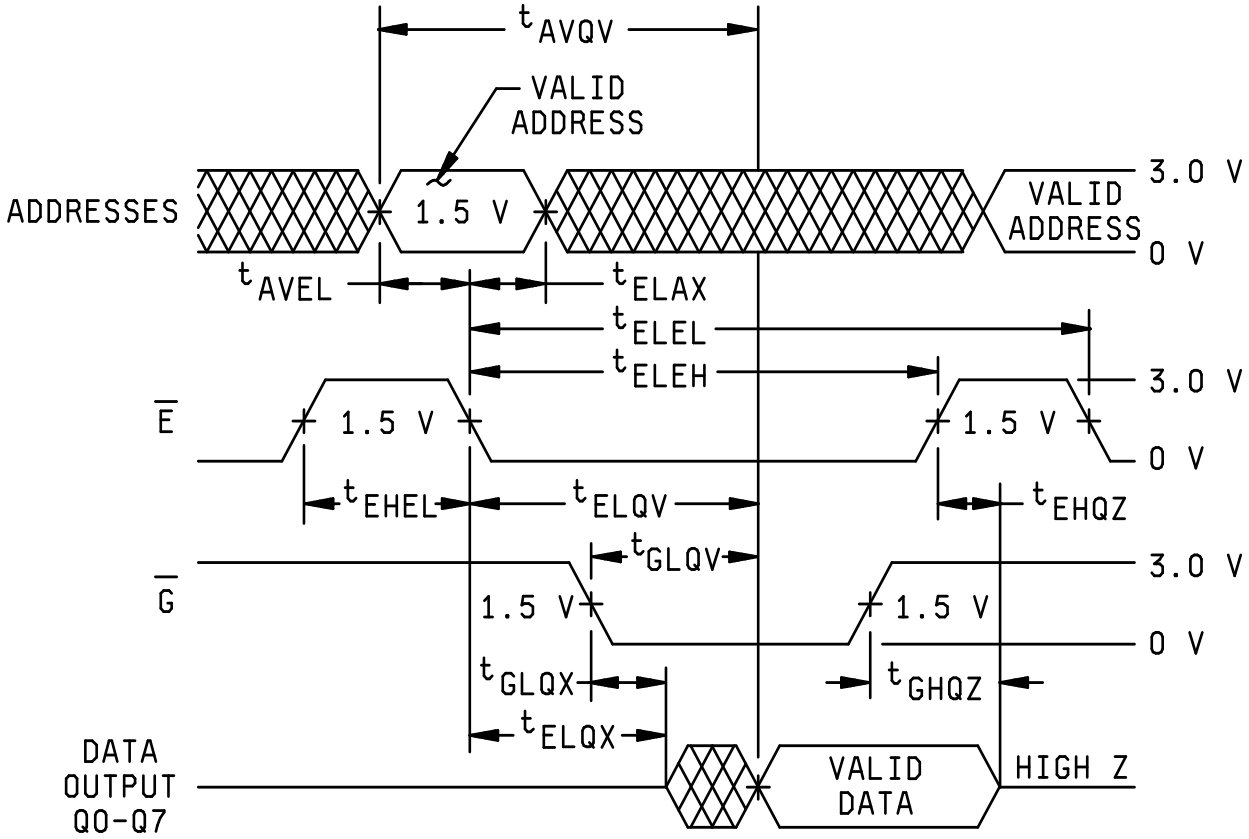


FIGURE 4. Read cycle waveform.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device Class Q	Device Class V	Device Class T
1	Interim electrical parameters (see 4.2)	1,7,9	1,7,9	As specified in QM plan
2	Static burn-in I method 1015	Not required	Required	
3	Same as line 1		1*,7*,9* Δ	
4	Dynamic burn-in (method 1015)	Required	Required	
5	Same as line 1		1*,7*,9* Δ	
6	Final electrical Parameters (see 4.2)	1*,2,3,7*, 8A,8B,9*,10,11	1*,2,3,7*, 8A,8B,9*,10,11	
7	Group A test requirements (see 4.4)	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10,11	
8	Group C end-point electrical parameters (see 4.4)	1,2,3,7, 8A,8B,9	1,2,3,7, 8A,8B,9,10,11 Δ	
9	Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	
10	Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1, 7, and 9.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IIA).
7/ See 4.6.

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I_I	±100 nA
I_{OZ}	±1 μA
I_{DDSB}	±50 μA
V_{OL}	±60 mV
V_{OH2}	±400 mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan, including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturers QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T, and V, interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535, including groups A, B, C, D, and E inspections and as specified herein. Technology conformance inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz.

d. For device classes Q and V, subgroups 7, 8A and 8B shall include verifying the functionality of the device.

e. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry, which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A= +25°C +5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K Rad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Dose rate induced latch-up testing. When specified in the purchase order or contract, the testing will be done in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When dose rate upset testing is performed, the testing will be done in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V and T devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. ASTM standard F1192 or JESD57 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥10^6 ions/cm2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in Table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in Table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

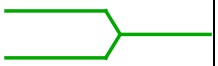
6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test conditions of SEP.
b. Number of upsets (SEU).
c. Number of transients (SET).
d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 18-02-14

Approved sources of supply for SMD 5962-95626 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9562601QXC	34371	HS1-6664RH-8
5962F9562601QYC	34371	HS9-6664RH-8
5962F9562601VXC	34371	HS1-6664RH-Q
5962F9562601VYC	34371	HS9-6664RH-Q
5962R9562601TXC	34371	HS1-6664RH-T
5962R9562601TYC	34371	HS9-6664RH-T

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert Conlan Blvd. Palm Bay, FL 32905