REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Make changes to 1.2.2, 1.3, 1.4, TABLE I, and figure 1.	94-03-03	M. A. FRYE
B	Drawing updated to reflect current requirements. - ro	01-10-16	R. MONNIN
C	Update drawing as part of 5 year review. –rrp	07-04-11	Robert M. Heber

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
CHARLES E. BESORE

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
93-01-26

MICROCIRCUIT, LINEAR, HIGH SPEED, PRECISION SAMPLE AND HOLD AMPLIFIER, MONOLITHIC SILICON

REVISION LEVEL
C

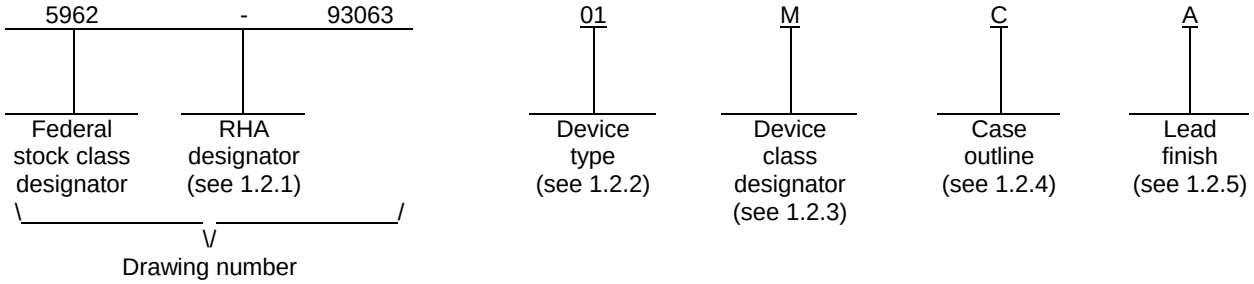
SIZE	CAGE CODE	
A	**67268**	**5962-93063**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HA-5340	Sample and hold amplifier
02	HA-5320	Sample and hold amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Voltage between $+V_S$ and $-V_S$ terminals:
- Device type 01 ..... 36 V dc
- Device type 02 ..... 40 V dc

Differential input voltage ..... 24 V dc

Digital input voltage ($\overline{S}$ /H pin):
- Device type 01 ..... +8.0 V dc / -6.0 V dc
- Device type 02 ..... +8.0 V dc / -15.0 V dc

Continuous output current ..... ±20 mA

Power dissipation, above +75°C (P_D):
- Case C ..... 1.4 W 2/
- Case 2 ..... 1.2 W 3/

Junction temperature (T_J) ..... +175°C

Lead temperature (soldering, 10 seconds) ..... +275°C

Storage temperature range ..... -65°C to +150°C

Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

Thermal resistance, junction-to-ambient (θ_{JA})
- Case C ..... +70°C/W
- Case 2 ..... +82°C/W

1.4 Recommended operating conditions.

Operating supply voltage ($\pm V_S$) ..... ±15 V dc

Analog input voltage (V_A) ..... ±10 V dc

Logic low input voltage range (V_{IL}) ..... 0 V dc to 0.8 V dc

Logic high input voltage range (V_{IH}) ..... 2.0 V dc to 5.0 V dc

Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate above +75°C at 14 mW/°C.
3/ Derate above +75°C at 12 mW/°C.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 60 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Input offset voltage	V_{IO}		1	01	-1.5	1.5	mV
			2,3		-3.0	3.0	
			1	02	-1.0	1.0	
			2,3		-2.0	2.0	
Input bias current	$+I_{IB}$		1,2,3	01	-350	350	nA
				02	-200	200	
	$-I_{IB}$			01	-350	350	
				02	-200	200	
Input offset current	I_{IO}		1,2,3	01	-350	350	nA
				02	-100	100	
Open loop voltage gain	$+A_{VS}$	V_{OUT} = +10 V,	1	01	110		dB
		R_L = 2.0 kΩ, C_L = 60 pF	2,3		100		
		V_{OUT} = +10 V,	1	02	120		
		R_L = 1.0 kΩ	2,3		110		
	$-A_{VS}$	V_{OUT} = -10 V,	1	01	110		
		R_L = 2.0 kΩ, C_L = 60 pF	2,3		100		
		V_{OUT} = -10 V,	1	02	120		
		R_L = 1.0 kΩ	2,3		110		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Common mode rejection ratio	+CMRR	$+V_S$ = 5 V, $-V_S$ = -25 V, V_{OUT} = -10 V, $V_{\overline{S}/H}$ = -9.2 V	1,2,3	01	72		dB
		$+V_S$ = 10 V, $-V_S$ = -20 V, V_{OUT} = -5 V, $V_{\overline{S}/H}$ = -4.2 V		02	80		
	-CMRR	$+V_S$ = 25 V, $-V_S$ = -5 V, V_{OUT} = +10 V, $V_{\overline{S}/H}$ = 10.8 V		01	72		
		$+V_S$ = 20 V, $-V_S$ = -10 V, V_{OUT} = +5 V, $V_{\overline{S}/H}$ = 5.8 V		02	80		
Output current	$+I_O$	V_{OUT} = +10 V	1,2,3	All	10		mA
	$-I_O$	V_{OUT} = -10 V				-10	
Output voltage swing	$+V_{OP}$	R_L = 2.0 kΩ, C_L = 60 pF	1,2,3	01	10		V
		R_L = 1.0 kΩ		02	10		
	$-V_{OP}$	R_L = 2.0 kΩ, C_L = 60 pF		01		-10	
		R_L = 1.0 kΩ		02		-10	
Power supply current	$+I_{CC}$	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	01		25	mA
				02		13	
	$-I_{CC}$			01	-25		
				02	-13		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Power supply rejection ratio	+PSRR	$+V_S$ = +13.5 V and +16.5 V, $-V_S$ = -15 V	1,2,3	01	75		dB
		$+V_S$ = +14.5 V and +15.5 V, $-V_S$ = -15 V		02	80		
	-PSRR	$-V_S$ = -13.5 V and -16.5 V, $+V_S$ = +15 V		01	75		
		$-V_S$ = -14.5 V and -15.5 V, $+V_S$ = +15 V		02	65		
Digital input high current	I_{INH}	V_{IN} = 5.0 V	1,2,3	01		40	µA
				02		0.1	
Digital input low current	I_{INL}	V_{IN} = 0 V	1,2,3	01		40	µA
			1	02		4	
			2,3			10	
Digital input low voltage	V_{IL}		1,2,3	All		0.8	V
Digital input high voltage	V_{IH}		1,2,3	All	2.0		V
Output voltage droop rate	V_D	V_{OUT} = 0 V, T_A = +125°C	2	01		95	µV/µs
				02		100	
Hold step error 3/	V_{ERR}	V_{IL} = 0 V, V_{IH} = 4.0 V, $t_R(V_{S/H})$ = 15 ns, T_A = +25°C	4	01	-50	50	mV
		V_{IL} = 0 V, V_{IH} = 3.5 V, 4/ $t_R(V_{IL}$ to $V_{IH})$ = 10 ns, T_A = +25°C		02	-6	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Rise time 3/	t_R	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +200 mV step, measured at 10 % and 90 % points	9,10,11	01		50	ns
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +200 mV step, measured at 10 % and 90 % points	9	02		150	
Fall time 3/	t_F	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to -200 mV step, measured at 10 % and 90 % points	9,10,11	01		50	ns
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +200 mV step, measured at 10 % and 90 % points	9	02		150	
Overshoot 3/	+OS	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +200 mV step	4,5,6	01		60	%
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +200 mV step	4	02		25	
	-OS	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to -200 mV step	4,5,6	01		60	
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to -200 mV step	4	02		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Slew rate 3/	+SR	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to +10 V step, measured at 25 % and 75 % points	4,5,6	01	40		V/µs
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = -5 V to +5 V step, measured at 10 % and 90 % points	4	02	30		
	-SR	A_V = +1.0, C_L = 60 pF, R_L = 2.0 kΩ, V_{OUT} = 0 mV to –10 V step, measured at 75 % and 25 % points	4,5,6	01	40		
		A_V = +1.0, T_A = +25°C, 4/ C_L = 50 pF, R_L = 2.0 kΩ, V_{OUT} = +5 V to –5 V step, measured at 90 % and 10 % points	4	02	30		
Hold mode feedthrough 4/	V_{HMF}	V_{IN} = 20 V_{PP}, f = 200 kHz, T_A = +25°C	4	01		-70	dB
		V_{IN} = 10 V_{PP}, f = 100 kHz, T_A = +25°C		02		-70	
Sample mode noise voltage 4/	$E_{n(S)}$	f = DC to 10 MHz, $V_{S/H}$ = 0 V, R_L = 2.0 kΩ, T_A = +25°C	4	01		335	µV rms
				02		200	
Hold mode noise voltage 4/	$E_{n(H)}$	f = DC to 10 MHz, $V_{S/H}$ = 5 V, R_L = 2.0 kΩ, T_A = +25°C	4	01		100	µV rms
				02		200	
Input capacitance 4/	C_{IN}	$V_{S/H}$ = 0 V, T_A = +25°C	4	All		5.0	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Input resistance 4/	R_{IN}	$V_{S/H}$ = 0 V, ΔV_{IN} = 20 V, T_A = +25°C	4	All	1.0		MΩ
Acquistion time, 0.1 percent 4/	t_{ACQ}	V_{OUT} = 0 V to 10 V step, R_L = 2.0 kΩ, C_L = 60 pF, T_A = +25°C	4	01		600	ns
		V_{OUT} = 0 V to 10 V step, R_L = 2.0 kΩ, C_L = 50 pF, T_A = +25°C		02		1.2	µs
Total harmonic distortion, hold mode 4/	$THD_{(H)1}$	f_S = 450 kHz, R_L = 2.0 kΩ, V_{IN} = 20 V_{PP}, 200 kHz, C_L = 60 pF, T_A = +25°C	4	01		-50	dBc
	$THD_{(H)2}$	f_S = 450 kHz, R_L = 2.0 kΩ, V_{IN} = 5.0 V_{PP}, 500 kHz, C_L = 60 pF, T_A = +25°C				-47	
Total harmonic distortion, sample mode 4/	$THD_{(S)1}$	V_{IN} = 20 V_{PP}, 200 kHz, R_L = 2.0 kΩ, C_L = 60 pF, T_A = +25°C	4	01		-60	dBc
	$THD_{(S)2}$	V_{IN} = 5.0 V_{PP}, 500 kHz, R_L = 2.0 kΩ, C_L = 60 pF, T_A = +25°C				-49	

1/ Unless otherwise specified, $+V_S$ = 15 V, $-V_S$ = -15, V_{IL} = 0.8 V (sample), V_{IH} = 2.0 V (hold), C_H = internal = 135 pF for device type 01, C_H = internal = 100 pF for device type 02, and signal ground = supply ground.

2/ The algebraic convention, where by the most negative value is a minimum and the most positive value is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

3/ Measured with -INPUT tied to OUTPUT.

4/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device types	01		02	
Case outlines	C	2	C	2
Terminal number	Terminal symbol			
1	-INPUT	NC	-INPUT	NC
2	+INPUT	-INPUT	+INPUT	-INPUT
3	OFFSET ADJUST	+INPUT	OFFSET ADJUST	+INPUT
4	OFFSET ADJUST	OFFSET ADJUST	OFFSET ADJUST	OFFSET ADJUST
5	$-V_S$	NC	$-V_S$	NC
6	SIGNAL GROUND	OFFSET ADJUST	SIGNAL GROUND	OFFSET ADJUST
7	OUTPUT	NC	OUTPUT	NC
8	NC	$-V_S$	INTEGRATOR BANDWIDTH	$-V_S$
9	$+V_S$	SIGNAL GROUND	$+V_S$	SIGNAL GROUND
10	NC	OUTPUT	NC	OUTPUT
11	EXTERNAL HOLD CAPACITOR	NC	EXTERNAL HOLD CAPACITOR	NC
12	NC	NC	NC	INTEGRATOR BANDWIDTH
13	SUPPLY GROUND	$+V_S$	SUPPLY GROUND	$+V_S$
14	$\overline{S}$ /H CONTROL	NC	$\overline{S}$ /H CONTROL	NC
15	---	NC	---	NC
16	---	EXTERNAL HOLD CAPACITOR	---	EXTERNAL HOLD CAPACITOR
17	---	NC	---	NC
18	---	NC	---	NC
19	---	SUPPLY GROUND	---	SUPPLY GROUND
20	---	$\overline{S}$ /H CONTROL	---	$\overline{S}$ /H CONTROL

NC = No connection

FIGURE 1. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5,6, 1/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6,9, 10,11	1,2,3,4,5,6,9, 10,11	1,2,3,4,5,6,9, 10,11
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3
Group D end-point electrical parameters (see 4.4)	1	1	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-04-11

Approved sources of supply for SMD 5962-93063 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9306301MCA	3/	HA1-5340/883
5962-9306301M2A	34371	HA4-5340/883
5962-9306302MCA	3/	HA1-5320/883
5962-9306302M2A	3/	HA4-5320/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803 Point of contact: 1650 Robert J. Conlan Blvd. Palm Bay, FL 32905

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.