REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to table I. Editorial changes throughout.	91-12-23	M. L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. - CFS	03-08-04	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	08-07-16	Thomas M. Hess
D	Update devices supplier information. Update boilerplate paragraphs to MIL-PRF-38535 requirements. - MAA	16-06-27	Thomas M. Hess
E	Update devices supplier CAGE 34371 information to bulletin page. Update boilerplate paragraphs to MIL-PRF-38535 requirements. - TTM	23-04-14	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
91-02-05

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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MICROCIRCUIT, DIGITAL, CMOS, UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER MONOLITHIC SILICON

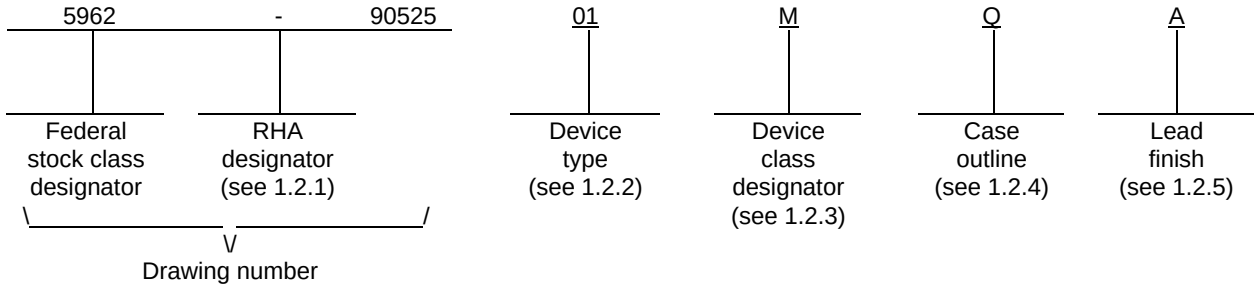
AMSC N/A	REVISION LEVEL E	SIZE A	CAGE CODE **67268**	**5962-90525**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example.



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Clock frequency (f_{clk})
01	HD-6402R	Universal asynchronous receiver transmitter (UART)	2.0 MHz
02	HD-6402B	Universal asynchronous receiver transmitter (UART)	8.0 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage	+8.0 V
Input, output, or I/O voltage applied	GND – 0.5 V dc to V_{CC} +0.5 V dc
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	1.03 W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	48.3°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Control definition. The control definition shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	V_{CC} = 5.5 V	1, 2, 3	All	2.3		V
Input low voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All		0.8	V
Input leakage current	I_I	V_O = 0 V or 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-1.0	1.0	µA
Output high voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5 V 2/	1, 2, 3	All	3.0		V
		I_{OH} = -100 µA, V_{CC} = 4.5 V 2/			V_{CC} – 0.4		
Output low voltage	V_{OL}	I_{OL} = +2.5 mA, V_{CC} = 4.5 V 2/	1, 2, 3	All		0.4	V
Output leakage current	I_O	V_O = 0 V or 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-1.0	1.0	µA
Operating supply current	I_{CC} 3/	V_O = 0 V or 5.5 V, V_{CC} = 5.5 V, f_{clk} = 2.0 MHz, Outputs open	1, 2, 3	All		2.0	mA
Standby supply current	I_{SB}	V_O = 0 V or 5.5 V, V_{CC} = 5.5 V, Outputs open	1, 2, 3	All		100	µA
Input capacitance	C_{IN}	All measurements are referenced to device GND, f = 1.0 MHz, T_A = +125°C,	4	All		25	pF
Output capacitance	C_{OUT}	See 4.4.1c	4	All		25	pF
Functional tests		See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock frequency	f_{CLK}	See figure 4. CL = 50 pF, V_{CC} = 4.5 V $t_r = t_f$ = 1.0 ns/V	9, 10, 11	01		2.0	MHz
				02		8.0	
CRL, DRR, and TBRL pulse width	t_{PW}		9, 10, 11	01	150		ns
				02	75		
Pulse width MR	t_{MR}		9, 10, 11	All	150		ns
Input data setup time	t_{SET}		9, 10, 11	01	50		ns
				02	20		
Input data hold time	t_{HOLD}		9, 10, 11	01	60		ns
				02	20		
Output enable time	t_{EN}		9, 10, 11	01		160	ns
				02		35	

1/ All tests shall be performed using the worst case conditions, unless otherwise specified.

2/ Interchanging of force and sense conditions is permitted. Relaxed input levels for V_{OL} and V_{OH} may be used if separate V_{IL} and V_{IH} tests that guarantee threshold voltage transition are performed.

3/ If not tested, shall be guaranteed to the limits specified in table I.

Device types: 01 and 02			
Case outline Q			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	21	MR
2	NC	22	TBRE
3	GND	23	$\overline{\text{TBRL}}$
4	RRD	24	TRE
5	RBR8	25	TRO
6	RBR7	26	TBR1
7	RBR6	27	TBR2
8	RBR5	28	TBR3
9	RBR4	29	TBR4
10	RBR3	30	TBR5
11	RBR2	31	TBR6
12	RBR1	32	TBR7
13	PE	33	TBR8
14	FE	34	CRL
15	OE	35	PI
16	SFD	36	SBS
17	RRC	37	CLS2
18	$\overline{\text{DRR}}$	38	CLS1
19	DR	39	EPE
20	RRI	40	TRC

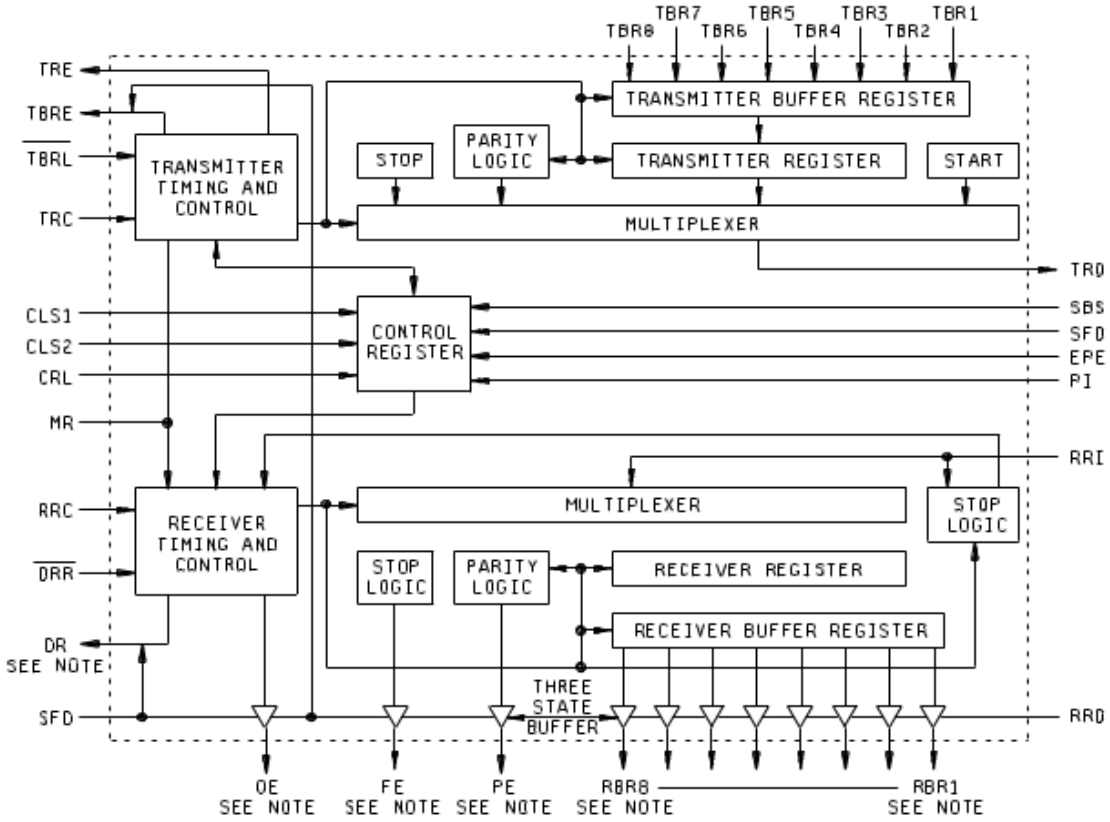
NC = No connection

FIGURE 1. Terminal connections.

Control word				Character format				
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

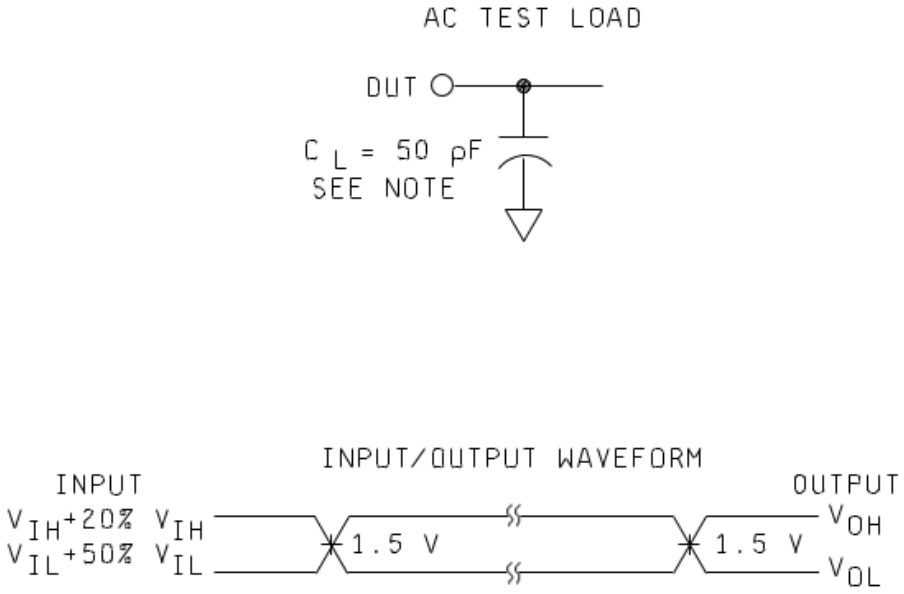
X = Irrelevant
0 = Low level voltage
1 = High level voltage

FIGURE 2. Control definition.



Note: These outputs are three-state.

FIGURE 3. Block diagram.



Note: C_L includes stray and jig capacitance.

FIGURE 4. Switching waveforms and test circuit.

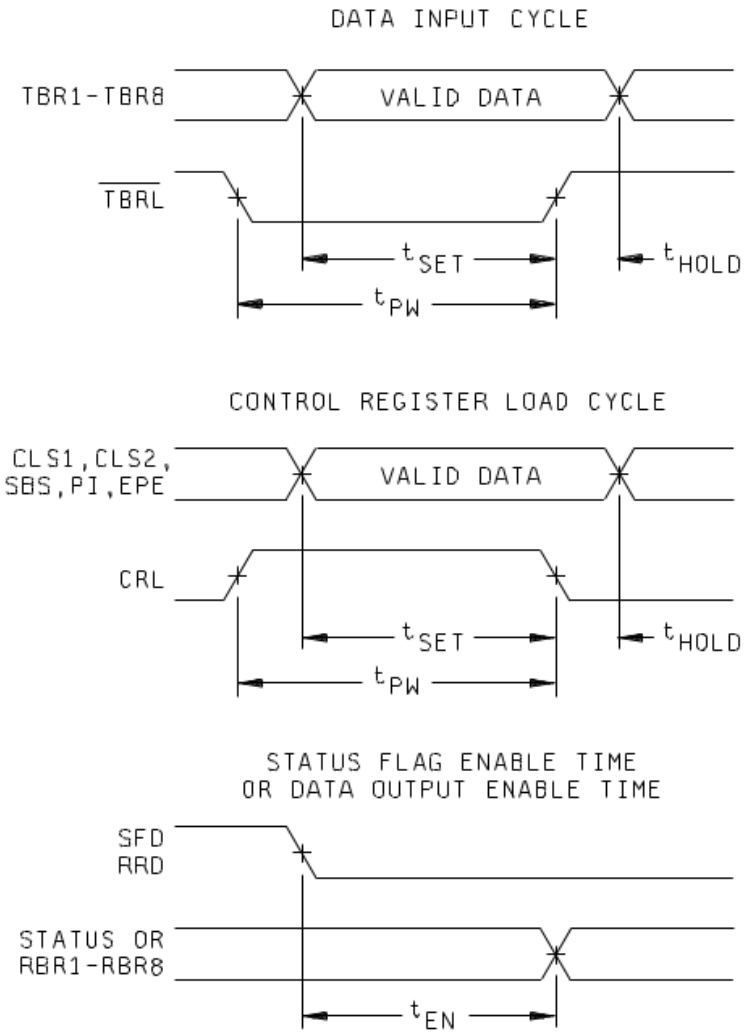


FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

Symbol	Definition	Functional description
V_{CC}		Positive supply current. A .01μF decoupling capacitor from the V_{CC} pin to the GND pin is recommended.
NC		No connection.
GND		Ground.
RRD	Receiver register disable	A high level on receiver register disable forces the receiver holding outputs RBR1 – RBR8 to high impedance state.
RBR1 through RBR8	Receiver buffer register	The contents of the receiver buffer register appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
PE	Parity error	A high level on parity error indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
FE	Framing error	A high level on framing error indicates the first stop bit was invalid.

Symbol	Definition	Functional description
OE	Overrun error	A high level on overrun error indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
SFD	Status flags disable	A high level on status flags disable forces the outputs PE, FE, OE, DR, and TBRE to a high impedance state.
RRC	Receiver register clock	The receiver register clock is 16X the receiver data rate.
$\overline{DRR}$	Data received reset	A low level on data received reset clears the data received output DR to a low level.
DR	Data received	A high level on data received indicates a character has been received and transferred to the receiver buffer register.
RRI	Receiver register input	Serial data on receiver register input is clocked into the receiver register.
MR	Master reset	A high level on master reset clears PE, FE, OE, and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power-up. The reset pulse should meet V_{IH} and t_{MR}. Wait 18 clock cycles after the falling edge of MR before beginning operation.
TBRE	Transmitter buffer register empty	A high level on transmitter buffer register empty indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
$\overline{TBRL}$	Transmitter buffer register load	A low level on transmitter buffer register load transfers data from inputs TBR1 – TBR8 into the transmitter buffer register. A low-to-high transition on $\overline{TBRL}$ initiates data transfer to the transmitter register. If busy, transfer is automatically delayed so that the two characters are transmitted end-to-end.
TRE	Transmitter register empty	A high level on transmitter register empty indicates completed transmission of a character including stop bits.
TRO	Transmitter register output	Character data, start data and stop bits appear serially at the transmitter register output.
TBR1 through TBR8	Transmitter buffer register	Character data is loaded into the transmitter buffer register via inputs TBR1 – TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to their programmed word length.
CRL	Control register load	A high level on control register load loads the control register with the control word. The control word is latched on the falling edge of CRL.
PI	Parity inhibit	A high level on parity inhibit inhibits parity generation, parity checking, and forces PE output low.
SBS	Stop bit select	A high level on stop bit select selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
CLS1, CLS2	Character length selected	These inputs program the character length selected (CLS1 low, CLS2 low, 5 bits) (CLS1 high, CLS2 low, 6 bits) (CLS1 low, CLS2 high, 7 bits) (CLS1 high, CLS2 high, 8 bits).
EPE	Even parity enable	When PI is low, a high level on even parity enable generates and checks even parity. A low level selects odd parity.
TRC	Transmitter register clock	The transmitter register clock is 16X the transmit data rate.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-04-14

Approved sources of supply for SMD 5962-90525 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9052501MQA	34371	HD-6402R
5962-9052502MQA	34371	HD-6402B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406