REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redraw. Update drawing to current requirements. - drw	08-10-24	Robert M. Heber

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A	PREPARED BY Rick Officer	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin APPROVED BY Michael A. Frye DRAWING APPROVAL DATE 88-12-20 REVISION LEVEL A	MICROCIRCUIT, LINEAR, 16-CHANNEL/ DIFFERENTIAL 8- CHANNEL CMOS MULTIPLEXER SIZE A | CAGE CODE **67268** | **5962-88699** SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88699	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	HI-516	16-channel/differential 8-channel CMOS analog multiplexer

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage between $+V_{CC}$ and $-V_{CC}$	33 V dc
Voltage between $+V_{CC}$ and ground	16.5 V dc
Voltage between $-V_{CC}$ and ground	16.5 V dc
Analog input voltage:	
$+V_S$	$+V_{CC}$ + 2.0 V dc
$-V_S$	$-V_{CC}$ - 2.0 V dc
Digital input voltage, TTL (V_{DD}/LLS = GND or open):	
$+V_A$	+6.0 V dc
$-V_A$	-6.0 V dc
$+A_3$/SDS	$+V_{CC}$ + 2.0 V dc
$-A_3$/SDS	$-V_{CC}$ - 2.0 V dc
Digital input voltage, CMOS (V_{DD}/LLS = +15 V):	
$+V_A$	$+V_{CC}$ + 2.0 V dc
$-V_A$	-2.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D):	
Case X	2.0 W 1/
Case 3	1.23 W 2/
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case X	50°C/W
Case 3	81°C/W
Junction temperature (T_J)	+175°C

1/ Derate linearly above T_A = +75°C at 20.0 mW/°C.
2/ Derate linearly above T_A = +75°C at 12.3 mW/°C.

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{CC}$)	±15 V dc
Analog input voltage (V_S)	$\pm V_{CC}$
Input logic low voltage range (V_{AL})	0 V dc to 0.8 V dc
Input logic high voltage range (V_{AH})	2.4 V dc to $+V_{CC}$
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Functional diagram. The functional diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{IH}	Measure inputs sequentially, All unused inputs = GND	1, 2, 3	All	-1.0	1.0	µA
	I_{IL}	Measure inputs sequentially, All unused inputs = +5.0 V	1, 2, 3		-25	25	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_D = -10 V, V_{EN} = 0.8 V, All unused inputs = -10 V	1, 2, 3	All	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10 V, V_D = +10 V, V_{EN} = 0.8 V, All unused inputs = +10 V	1, 2, 3		-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_S = -10 V, V_D = +10 V, V_{EN} = 0.8 V, All unused inputs = -10 V	1, 2, 3	All	-100	+100	nA
	$-I_{D(OFF)}$	V_S = +10 V, V_D = -10 V, V_{EN} = 0.8 V, All unused inputs = +10 V	1, 2, 3		-100	+100	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	$V_S = V_D$ = +10 V, All unused inputs = -10 V	1, 2, 3	All	-100	+100	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -10 V, All unused inputs = +10 V	1, 2, 3		-100	+100	
Positive supply current	$+I_{CC}$	V_S = 0 V, V_D = open, V_{EN} = 2.4 V, sequence all address combinations, record highest $+I_{CC}$	1, 2, 3	All		+25	mA
Negative supply current	$-I_{CC}$	V_S = 0 V, V_D = open, V_{EN} = 2.4 V, sequence all address combinations, record highest $-I_{CC}$	1, 2, 3	All	-25		mA
Standby positive supply current	$+I_{SBY}$	V_A = 0.8 V, V_{EN} = 0.8 V, V_S = 0 V, V_D = open	1, 2, 3	All		+25	mA
Standby Negative supply current	$-I_{SBY}$		1, 2, 3		-25		mA
Switch "ON" resistance	$+R_{DS1}$	V_S = +10 V, I_D = -100 µA	1	All		750	Ω
			2, 3			1000	
	$-R_{DS1}$	V_S = -10 V, I_D = +100 µA	1			750	
			2, 3			1000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic level voltage	V_{AL} (TTL)	V_{DD}/LLS = GND	1, 2, 3	All		0.8	V
	V_{AH} (TTL)				2.4		
	V_{AL} (CMOS)	V_{DD}/LLS = +15 V	1, 2, 3	All		4.5	V
	V_{AH} (CMOS)				10.5		
Address input capacitance	C_A	$+V_{CC} = -V_{CC} = 0$ V, f = 1.0 MHz, $T_A = +25°C$, See 4.3.1c	4	All		10	pF
Output switch capacitance	C_{OS}		4	All		25	pF
Input switch capacitance	C_{IS}		4	All		10	pF
Charge transfer error 2/	V_{CTE}	V_S = GND, V_{EN} = 0 to 5.0 V, C_L = 100 pF, f = 500 kHz, $T_A = +25°C$	4	All		20	mV
Off channel isolation 2/	V_{ISO}	V_{EN} = 0.8 V, R_L = 1.0 kΩ, C_L = 40 pF, V_S = 3.0 V rms, f = 500 kHz, $T_A = +25°C$	4	All	-55		dB
Break-before-make time delay	t_d	R_L = 800Ω, C_L = 12.5 pF See figure 4	9	All	10		ns
			10		2.0		
			11 2/		2.0		
Propagation delay time, enable to I/O	$t_{ON(EN)}$		9	All		175	ns
			10, 11			225	
	$t_{OFF(EN)}$		9			175	ns
			10, 11			225	
Propagation delay time, address inputs to I/O channel	t_A	R_L = 10 MΩ, C_L = 12.5 pF See figure 4	9	All		175	ns
			10, 11			225	
Functional test		See 4.3.1d	7, 8	All			

1/ $+V_{CC}$ = +15 V, $-V_{CC}$ = -15V, V_{EN} = 2.4 V, V_{DD}/LLS = GND, V_{AH} = 2.4 V and V_{AL} = 0.8 V, unless otherwise specified.
2/ Guaranteed, but not tested to the limits specified in table I.

Device type	01
Case outlines	X and 3
Terminal number	Terminal symbol
1	$+V_{CC}$
2	OUT B
3	No connection
4	IN 16/8B
5	IN 15/7B
6	IN 14/6B
7	IN 13/5B
8	IN 12/4B
9	IN 11/3B
10	IN 10/2B
11	IN 9/1B
12	GND
13	V_{DD}/LLS
14	A_3/SDS
15	A_2
16	A_1
17	A_0
18	Enable
19	IN 1/1A
20	IN 2/2A
21	IN 3/3A
22	IN 4/4A
23	IN 5/5A
24	IN 6/6A
25	IN 7/7A
26	IN 8/8A
27	$-V_{CC}$
28	OUT A

FIGURE 1. Terminal connections.

16-channel multiplexer operation. 1/ 2/

Use A_3 as digital address input					On channel to	
Enable	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

See footnotes at end of table.

FIGURE 2. Truth table.

Differential 8-channel multiplexer operation. 2/ 3/

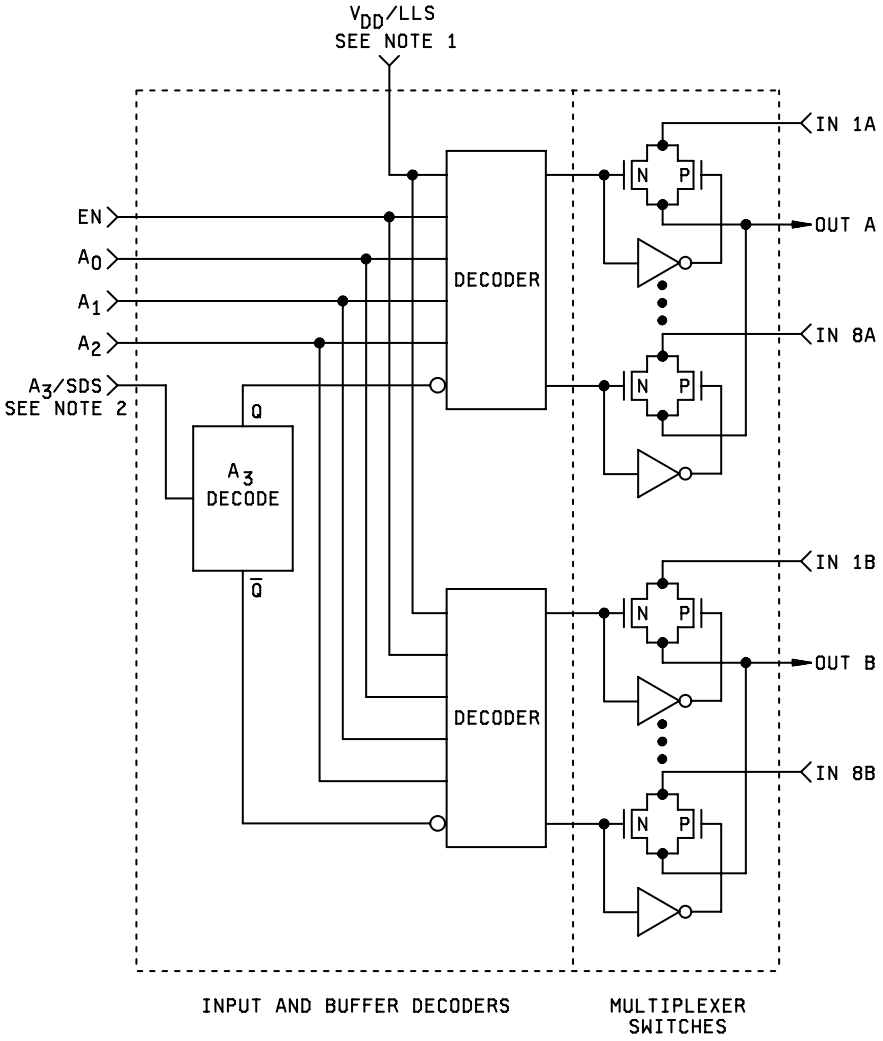
A_3 connected to $-V_{CC}$				On channel to	
Enable	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

1/ For 16-channel operation, connect OUT A to OUT B.

2/ H = High logic level
L = Low logic level
X = Don't care

3/ For differential 8-channel operation, use the A_3 address pin to select the differential mode where $A_3 = -V_{CC}$ and OUT A is not connected to OUT B.

FIGURE 2. Truth table - continued.



A_3 decode		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
$-V_{CC}$	L	L

NOTES:
1. LLS = logic level select. The circuit is TTL compatible when V_{DD}/LLS = GND or open, and CMOS compatible when V_{DD}/LLS = +15 V.
2. SDS = single ended/differential select. Multiplexer is in differential mode when A_3/SDS = $-V_{CC}$.

FIGURE 3. Functional diagram.

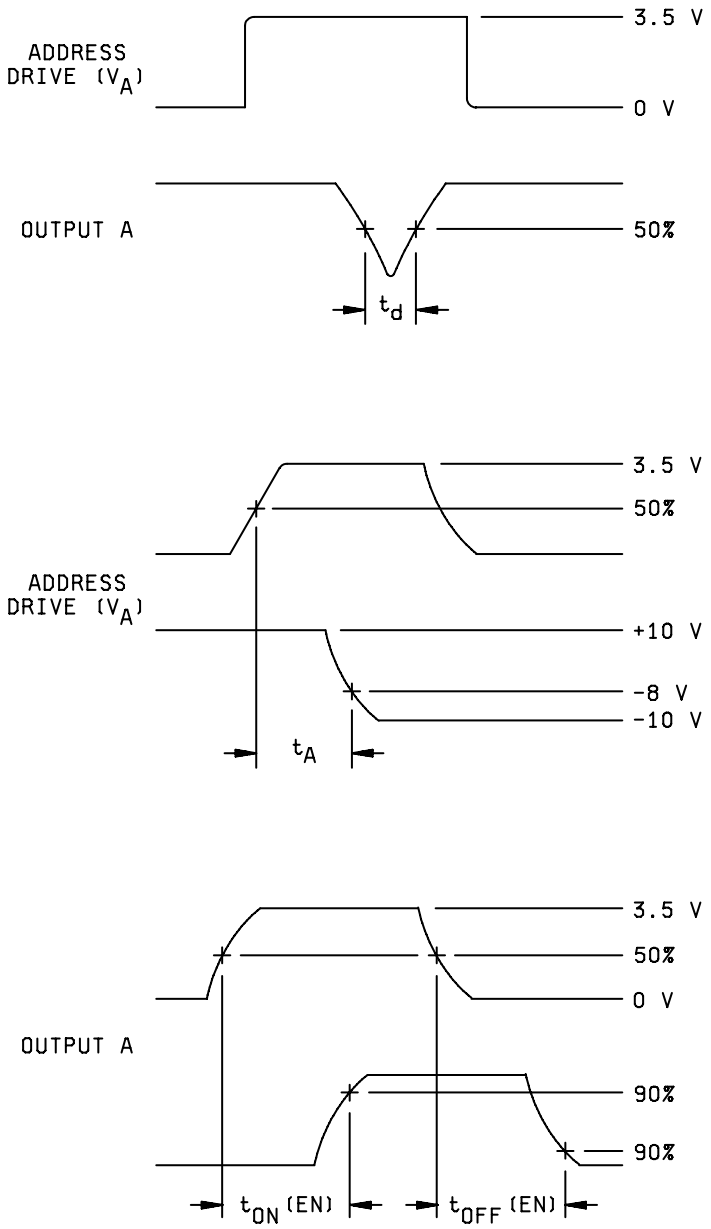


FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** See 4.3.1c.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (capacitance measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is fifteen devices, all input and output terminals tested, and no failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-10-24

Approved sources of supply for SMD 5962-88699 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8869901XA	3/	HI1-516/883
5962-88699013A	3/	HI4-516/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901