

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate and made editorial changes throughout. - LTG	00-05-19	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-07-25	Thomas M. Hess
C	Update boilerplate paragraphs to MIL-PRF-38535 requirements. - jwc	15-05-22	Thomas M. Hess
D	Update vendor CAGE 34371 information. Update boilerplate to MIL-PRF-38535 requirements. - DRH	22-03-14	Muhammad A. Akbar



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

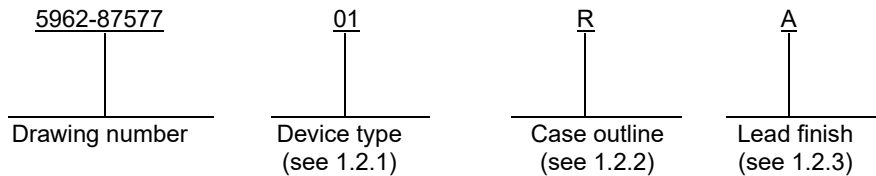
REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12								

PMIC N/A																			
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>		PREPARED BY Ray Monnin						<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>											
		CHECKED BY D. A. DiCenzo																	
		APPROVED BY N. A. Hauck						<p align="center">MICROCIRCUIT, CMOS, OCTAL BUS TRANSCEIVER, MONOLITHIC SILICON</p>											
		DRAWING APPROVAL DATE 87-04-21																	
AMSC N/A		REVISION LEVEL D						SIZE A		CAGE CODE 67268				5962-87577					
												SHEET		1 OF 12					

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	82C86	CMOS octal bus transceiver
02	82C87	CMOS octal inverting bus transceiver

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (referenced to ground)	+8.0 V dc maximum
Input, output or I/O voltage applied	GND -0.5 V dc to V _{CC} +0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P _D).....	1.0 W <u>1/</u>
Lead temperature (soldering, 10 seconds).....	+275°C
Maximum junction temperature (T _J)	+150°C
Thermal resistance, junction to case (θ _{JC}):	
Case R.....	(See MIL-STD-1835)
Case 2	23°C/W <u>2/</u>

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
2/ When a thermal resistance value for this case is included in MIL-STD-1835 that value shall supersede the value indicated herein.

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1.4 Recommended operating conditions.

Supply voltage (V _{CC}).....	+4.5 V dc minimum to +5.5 V dc maximum
Input to output delay, inverting or noninverting (t _{IOV}).....	5 ns minimum <u>1/</u> <u>2/</u> <u>3/</u> (reference no. 1)
Transmit/receive hold time (t _{EHTV}).....	5 ns minimum <u>1/</u> <u>2/</u> (reference no. 2)
Transmit/receive setup time (t _{VEL}).....	10 ns minimum <u>1/</u> <u>2/</u> (reference no. 3)
Output disable time (t _{HOZ}).....	5 ns minimum to 35 ns maximum <u>1/</u> <u>2/</u> (reference no. 4)
Output enable time (t _{LOV}).....	10 ns minimum <u>1/</u> <u>2/</u> <u>3/</u> (reference no. 5)
Input rise/fall time (t _r /t _f).....	20 ns minimum <u>1/</u> <u>2/</u> (reference no. 6)
Minimum output enable high time (t _{EHEL}).....	35 ns minimum <u>1/</u> <u>2/</u> <u>4/</u> (reference no. 7)
Case operating temperature range (T _c).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Not tested but characterized at initial device design and after major process or design changes affecting this parameter.
2/ See appropriate ac test load and timing reference number see figure 4.
3/ Reference table I for other limit.
4/ A system limitation only when changing directions.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Item requirements. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -8.0 mA B outputs <u>1/</u>	1, 2, 3	All	3.0		V
		V _{CC} = 4.5 V, I _{OH} = -4.0 mA A outputs <u>1/</u>	1, 2, 3	All	3.0		V
		V _{CC} = 4.5 V, I _{OH} = -100 μA A or B outputs <u>1/</u>	1, 2, 3	All	V _{CC} -0.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA B outputs <u>1/</u>	1, 2, 3	All		0.45	V
		V _{CC} = 4.5 V, I _{OL} = 12 mA A outputs <u>1/</u>	1, 2, 3	All		0.45	V
Input high level	V _{IH}	V _{CC} = 5.5 V <u>2/</u>	1, 2, 3	All	2.2		V
Input low level	V _{IL}	V _{CC} = 4.5 V	1, 2, 3	All		0.8	V
Input leakage current	I _{IN}	V _{CC} = 5.5 V, V _{IN} = V _{CC} or GND	1, 2, 3	All	-10.0	10.0	μA
Output leakage current	I _{OUT}	V _{CC} = 5.5 V, V _{OUT} = V _{CC} or GND, OE ≥ V _{CC} -0.5 V	1, 2, 3	All	-10.0	10.0	μA
Standby supply current	I _{CCSB}	V _{CC} = 5.5 V, V _{IN} = V _{CC} or GND, outputs open	1, 2, 3	All		10	μA
Input capacitance, A inputs	C _{IN}	f = 1.0 MHz, T _C = +25°C All measurements referenced to device ground. See 4.3.1c	4	All Case R		13	pF
				All Case 2		10	pF
Input capacitance, B inputs	C _{IN}	f = 1.0 MHz, T _C = +25°C All measurements referenced to device ground. See 4.3.1c	4	All Case R		17	pF
				All Case 2		15	pF
Input capacitance, all other inputs	C _{IN}	f = 1.0 MHz, T _C = +25°C All measurements referenced to device ground. See 4.3.1c	4	All Case R		12	pF
				All Case 2		7	pF
Functional test		V _{CC} = 4.5 V and 5.5 V <u>3/</u> See 4.3.1d	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Input to output delay, inverting or noninverting	t _{I/OV}	V _{CC} = 4.5 V and 5.5 V ^{3/} Reference number 1 and figure 4.	9, 10, 11	All	<u>4/</u>	35	ns
Output enable time	t _{ELOV}	V _{CC} = 4.5 V and 5.5 V ^{3/} Reference number 5 and figure 4	9, 10, 11	All	<u>4/</u>	65	ns

1/ Interchanging of force and sense conditions is permitted.

2/ V_{IH} is measured by applying a pulse magnitude = V_{IH} minimum to one data input at a time and checking the corresponding device output for a valid logical one during valid input high time. Control pins, T (transmit) and OE, are tested separately with all device data input pins at V_{CC} - 0.4 V.

3/ Tested as follows: f = 1 MHz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, C_L = 50 pF (unless otherwise specified), V_{OH} ≥ 1.5 V, V_{OL} ≤ 1.5 V, and V_{IH} for T (transmit control pin) ≥ V_{CC} - 0.5 V. Input rise and fall times are driven at 1 ns/V.

4/ Reference 1.4 for this limit.

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Device type 01			
Case outlines R and 2			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A ₀	11	T
2	A ₁	12	B ₇
3	A ₂	13	B ₆
4	A ₃	14	B ₅
5	A ₄	15	B ₄
6	A ₅	16	B ₃
7	A ₆	17	B ₂
8	A ₇	18	B ₁
9	\overline{OE}	19	B ₀
10	GND	20	V _{CC}

Device type 02			
Case outlines R and 2			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A ₀	11	T
2	A ₁	12	$\overline{B_7}$
3	A ₂	13	$\overline{B_6}$
4	A ₃	14	$\overline{B_5}$
5	A ₄	15	$\overline{B_4}$
6	A ₅	16	$\overline{B_3}$
7	A ₆	17	$\overline{B_2}$
8	A ₇	18	$\overline{B_1}$
9	\overline{OE}	19	$\overline{B_0}$
10	GND	20	V _{CC}

FIGURE 1. Terminal connections.

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T	\overline{OE}	A	B
X	H	Z	Z
H	L	I	O
L	L	O	I

H = Logic one
L = Logic zero
I = Input mode
O = Output mode
X = Irrelevant
Z = High impedance

FIGURE 2. Truth table.

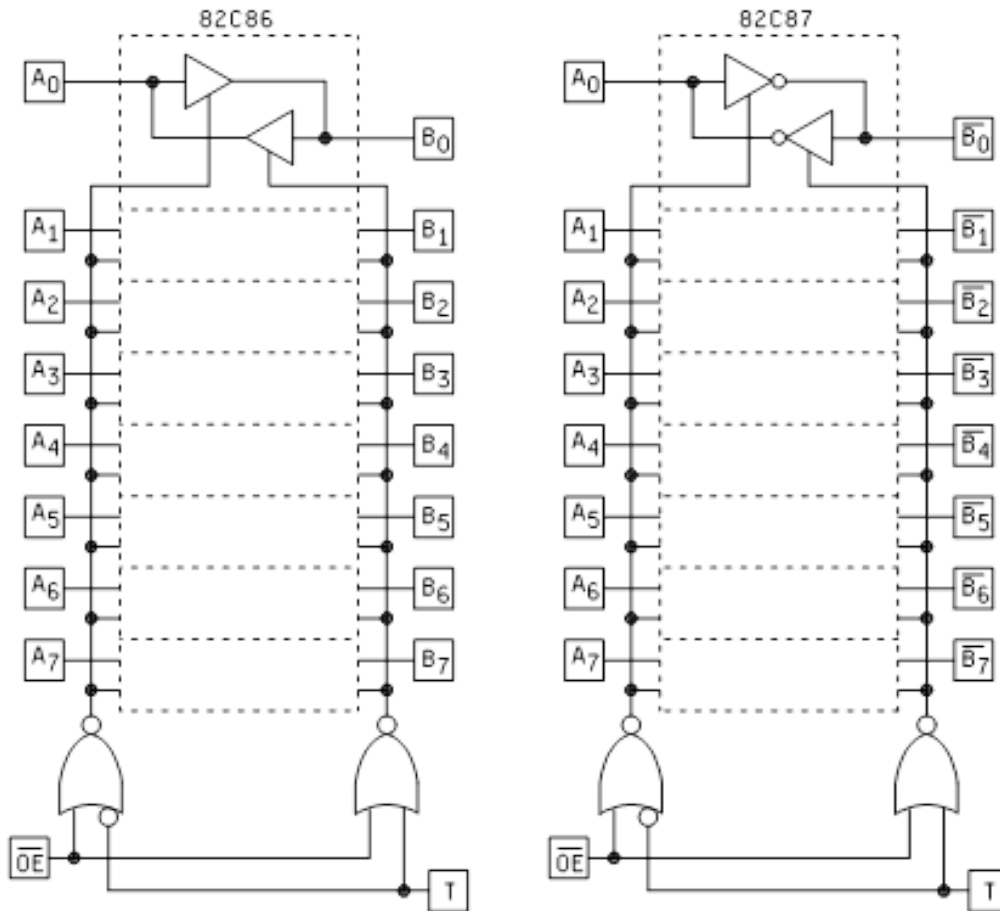


FIGURE 3. Block diagram.

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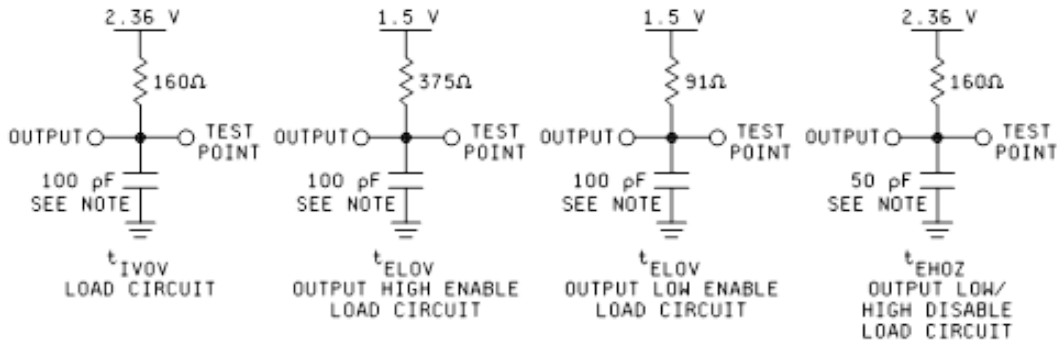
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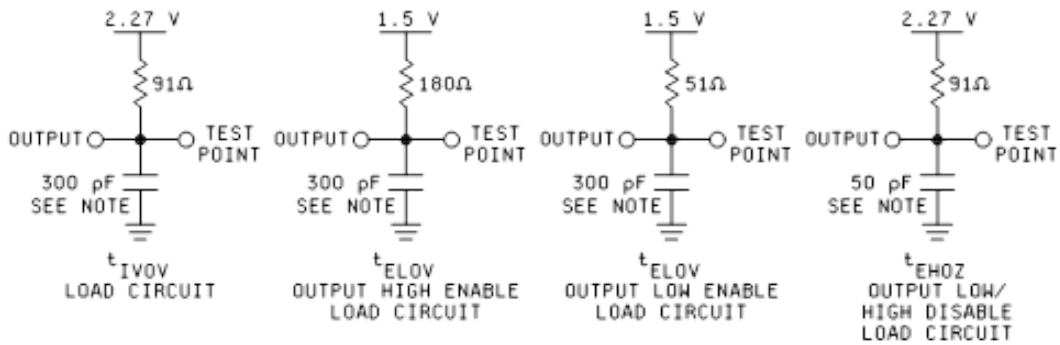
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AC TEST CIRCUIT SPECIFICATIONS

A SIDE OUTPUT



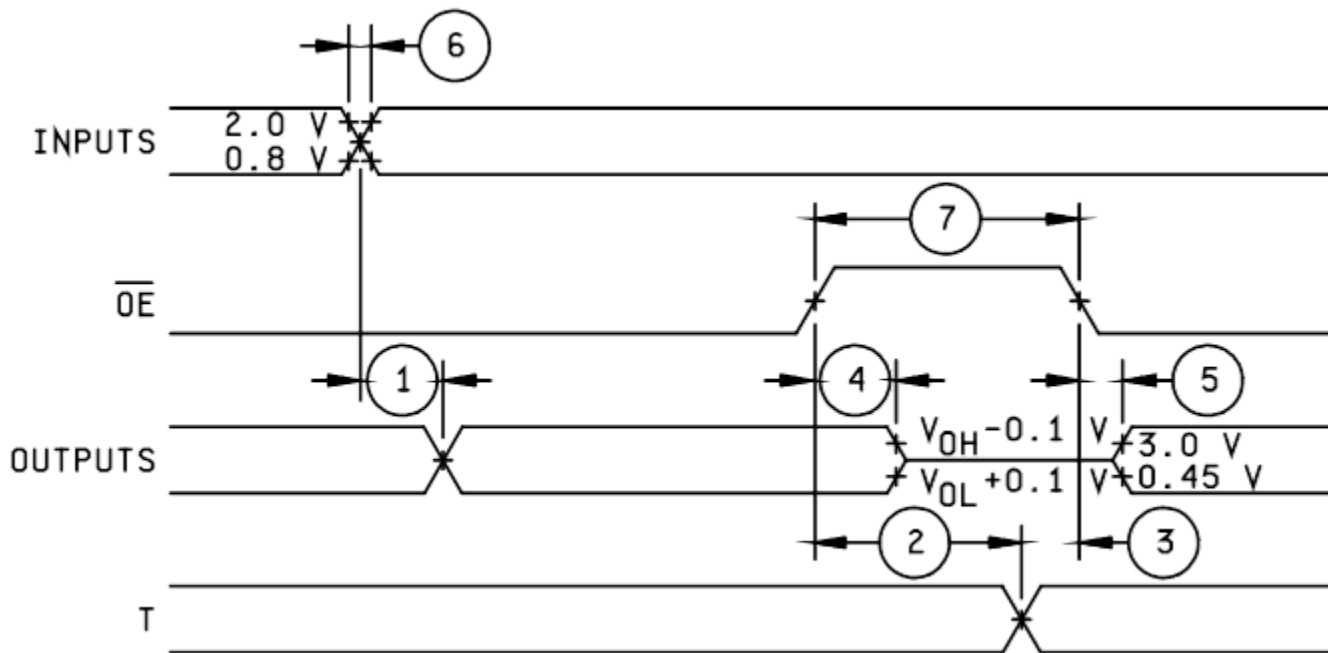
B SIDE OUTPUT



NOTE: Includes jig and stray capacitance. Resistances have a tolerance of $\pm 1\%$. Capacitances have a tolerance of $\pm 10\%$.

FIGURE 4. Test circuit and timing waveforms.

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All timing measurements are made at 1.5 V unless otherwise noted.
 Inputs must switch between $V_{IL} - 0.4 V$ and $V_{IH} + 0.4 V$.

FIGURE 4. Test circuit and timing waveforms – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (125°C only), 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- d. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 Group C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime VA, Columbus, Ohio 43218-3990, or telephone (614) 692 0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-03-14

Approved sources of supply for SMD 5962-87577 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8757701RA	34371	MD82C86H-5/883
5962-87577012A	<u>3/</u>	MR82C86H-5/883
5962-8757702RA	34371	MD82C87H-5/883
5962-87577022A	<u>3/</u>	MR82C87H-5/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
number

34371

Vendor name
and address

Renesas Electronics America, Inc.
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.