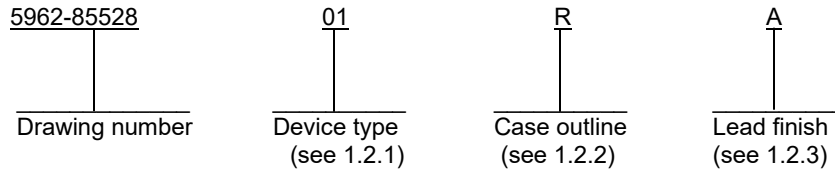


1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Frequency</u>	<u>Circuit</u>
01	82C89	8 MHz	CMOS Bus Arbiter

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
R	D-8 (20-lead, 1/4" x 1-1/16"), dual-in-line package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+8.0 V <u>1/</u>
Input, output or I/O voltage applied	GND-0.5 V to $V_{CC}+0.5$ V <u>1/</u>
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C
Temperature under bias	-55 °C to +125 °C
Storage temperature range	-65 °C to +150 °C
Maximum package power dissipation, (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260 °C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55 °C to +125 °C
Maximum frequency of operation (f_{MAX})	0 to 8.0 MHz
Setup time, status active (t_{SVCH})	t_{CLCL} - 10 ns maximum <u>3/</u>
Setup time, status inactive (t_{SHCL})	t_{CLCL} - 10 ns maximum <u>3/</u>
\overline{BCLK} high time (t_{BHCL})	0.65 t_{BLBL} maximum <u>3/</u>
Delay time, \overline{BCLK} to \overline{CBRQ} float (t_{BLCBH})	35 ns maximum
Delay time, \overline{BCLK} to \overline{BUSY} float (t_{BLBYH})	35 ns maximum
Input rise time (t_r)	20 ns maximum
Input fall time (t_f)	20 ns maximum

1/ All voltages referenced to V_{SS} .
2/ $V_{CC} = 4.5$ V and 5.5 V.
3/ See table I for minimum limits.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A	5962-85528
	REVISION LEVEL A	SHEET 2

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 3

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Weapons Support-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

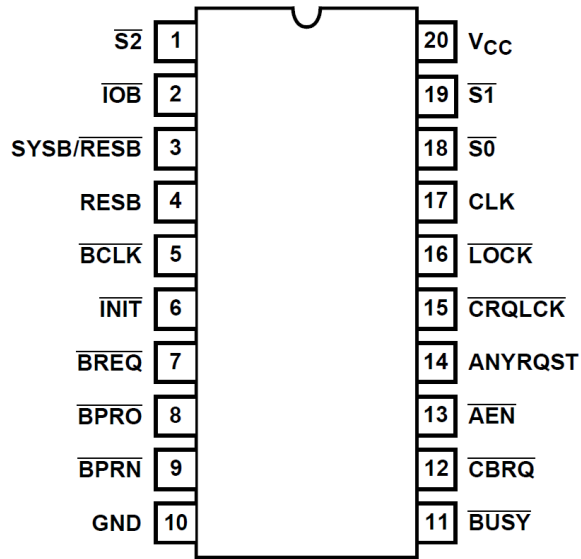
3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Weapons Support-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Weapons Support, DLA Weapons Support's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 4

Case R



Case 2

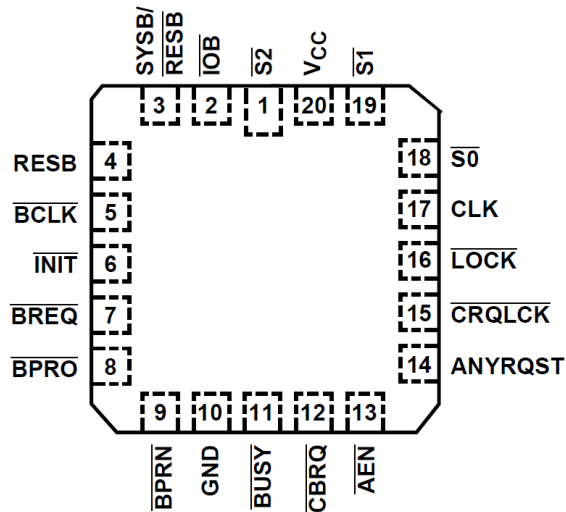


FIGURE 1. Terminal connections (top view).

**STANDARD
MICROCIRCUIT DRAWING**

DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
A

5962-85528

SHEET **5**

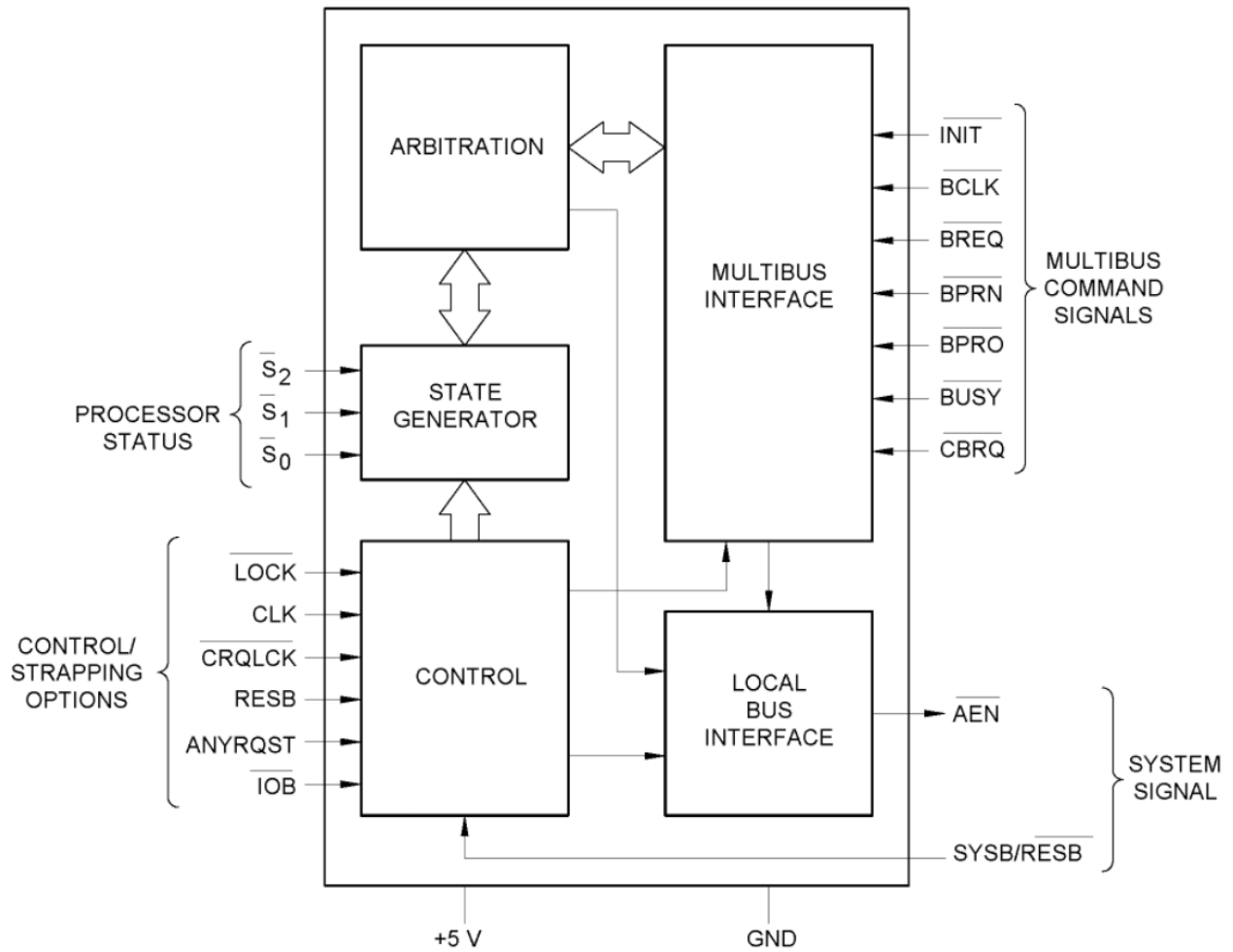


FIGURE 2. Functional block diagram.

**STANDARD
MICROCIRCUIT DRAWING**
DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-85528

REVISION LEVEL
A

SHEET **6**

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V _{IH}	V _{CC} = 5.5V	1, 2, 3	All	2.2		V
Input low voltage	V _{IL}	V _{CC} = 4.5V	1, 2, 3			0.8	V
Input high clock voltage	V _{IHC}	V _{CC} = 5.5V	1, 2, 3		70% V _{CC}		V
Input low clock voltage	V _{ILC}	V _{CC} = 4.5V	1, 2, 3			20% V _{CC}	V
Output low voltage (<u>BUSY</u> , <u>CBRQ</u>)	V _{OL1}	V _{CC} = 4.5V, I _{OL} = 20mA, Test pins 11 and 12	1, 2, 3			0.45	V
Output low voltage (<u>AEN</u>)	V _{OL2}	V _{CC} = 4.5V, I _{OL} = 16mA, Test pin 13	1, 2, 3			0.45	V
Output low voltage (<u>BPRO</u> , <u>BREQ</u>)	V _{OL3}	V _{CC} = 4.5V, I _{OL} = 10mA, Test pins 7 and 8	1, 2, 3			0.45	V
Output high voltage (<u>BUSY</u> , <u>CBRQ</u>)	V _{OH1}	V _{CC} = 4.5V, Open drain, Test pins 11 and 12	1, 2, 3		<u>9/</u>		V
Output high voltage (All others)	V _{OH2}	V _{CC} = 4.5V, I _{OH} = -2.5mA, Test pins 7-8 and 13	1, 2, 3		3.0		V
Output high voltage (All others)	V _{OH3}	V _{CC} = 4.5V, I _{OH} = -100μA, Test pins 7-8 and 13	1, 2, 3		V _{CC} -0.4		V
Input leakage current	I _I	V _{CC} = 5.5V, V _{IN} = GND or V _{CC} , Test pins 1-6, 9 and 14-19	1, 2, 3		-1.0	1.0	μA
I/O leakage current (<u>BUSY</u> , <u>CBRQ</u>)	I _O	V _{CC} = 5.5V, V _{IN} = GND or V _{CC} , Test pins 11-12	1, 2, 3		-10	10	μA
Standby supply current	I _{CCSB}	V _{CC} = 5.5V, V _{IN} = GND or V _{CC} , Outputs open	1, 2, 3			10	μA
Operating supply current	I _{CCOP}	V _{CC} = 5.5V, f = 1MHz, Outputs open <u>2/</u>	1, 2, 3		1.0	mA/MHz	
Input capacitance	C _{IN}	T _C = +25°C, f = 1MHz	4		10	pF	
Output capacitance	C _O		4		10	pF	
I/O capacitance	C _{I/O}		4		15	pF	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
A

5962-85528

SHEET **7**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test	FT	V _{CC} = 4.5V and 5.5V <u>3/</u>	7, 8	All			
CLK cycle time	t _{CLCL}	V _{CC} = 4.5V and 5.5V	9, 10, 11		125		ns
CLK low time	t _{CLCH}		9, 10, 11		55		ns
CLK high time	t _{CHCL}		9, 10, 11		35		ns
Status active setup time	t _{SVCH}		9, 10, 11		65	<u>4/</u>	ns
Status inactive setup time	t _{SHCL}		9, 10, 11		50	<u>4/</u>	ns
Status active hold time	t _{HVCL}		9, 10, 11		10		ns
Status inactive hold time	t _{HVCH}		9, 10, 11		10		ns
$\overline{\text{BUSY}}^{**}$ setup to $\overline{\text{BCLK}}$ <u>5/ 8/</u>	t _{BYSBL}		9, 10, 11		20		ns
$\overline{\text{CBRQ}}^{**}$ setup to $\overline{\text{BCLK}}$ <u>5/</u>	t _{CBSBL}		9, 10, 11		20		ns
$\overline{\text{BCLK}}$ cycle time	t _{BLBL}		9, 10, 11		100		ns
$\overline{\text{BCLK}}$ high time	t _{BHCL}		9, 10, 11		30	<u>4/</u>	ns
$\overline{\text{LOCK}}$ inactive hold time	t _{CLLL1}		9, 10, 11		10		ns
$\overline{\text{LOCK}}$ active hold time	t _{CLLL2}		9, 10, 11		40		ns
$\overline{\text{BPRN}}^{**}$ to $\overline{\text{BCLK}}$ setup time <u>5/</u>	t _{PNBL}		9, 10, 11		15		ns
$\overline{\text{SYSB}}/\overline{\text{RESB}}$ setup time	t _{CLSR1}		9, 10, 11	0		ns	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-85528

REVISION LEVEL
A

SHEET **8**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SYSB/ <u>RESB</u> hold time	t _{CLSR2}	V _{CC} = 4.5V and 5.5V	9, 10, 11	All	30		ns
Initialization pulse width	t _{VIH}		9, 10, 11		675		ns
<u>BCLK</u> to <u>BREQ</u> ** delay time ^{5/}	t _{BLBRL}		9, 10, 11			35	ns
<u>BCLK</u> to <u>BPRO</u> ** ^{5/ 6/}	t _{BLPOH}		9, 10, 11			40	ns
<u>BPRN</u> ** to <u>BPRO</u> ** delay time ^{5/ 6/}	t _{PNPO}		9, 10, 11			25	ns
<u>BCLK</u> to <u>BUSY</u> low	t _{BLBYL}		9, 10, 11			60	ns
CLK to <u>AEN</u> high	t _{CLAEH}		9, 10, 11			65	ns
<u>BCLK</u> to <u>AEN</u> low	t _{BLAEL}		9, 10, 11			40	ns
<u>BCLK</u> to <u>CBRQ</u> low	t _{BLCBL}		9, 10, 11			60	ns
Output rise time	t _{OLOH}		V _{CC} = 4.5V and 5.5V, From 0.8V to 2.0V ^{7/}		9, 10, 11		20
Output fall time	t _{OHOL}	V _{CC} = 4.5V and 5.5V, From 2.0V to 0.8V ^{7/}	9, 10, 11		12	ns	

- ^{1/} During AC testing, input waveforms must switch between V_{IH}+0.4 V and V_{IL}-0.4 V. Input rise and fall times are driven at 1ns/V. Loading is per appropriate AC test circuit (see figure 3).
- ^{2/} Maximum current defined by CLK or BCLK, whichever has the highest operating frequency.
- ^{3/} Tested as follows: f = 1MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, Load per appropriate AC test circuit, V_{OH} ≥ 1.5V, and V_{OL} ≤ 1.5V.
- ^{4/} Reference paragraph 1.4 for this limit.
- ^{5/} Both transitions of the signal apply to parameters with asterisks (**).
- ^{6/} BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRN.
- ^{7/} Except BUSY and CBRQ.
- ^{8/} The falling edge of BUSY may be sensitive to the rising or falling edge of BCLK, while the rising edge of BUSY is always sensitive to the falling edge of BCLK.
- ^{9/} No measurement required.

**STANDARD
MICROCIRCUIT DRAWING**
DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-85528

REVISION LEVEL
A

SHEET **9**

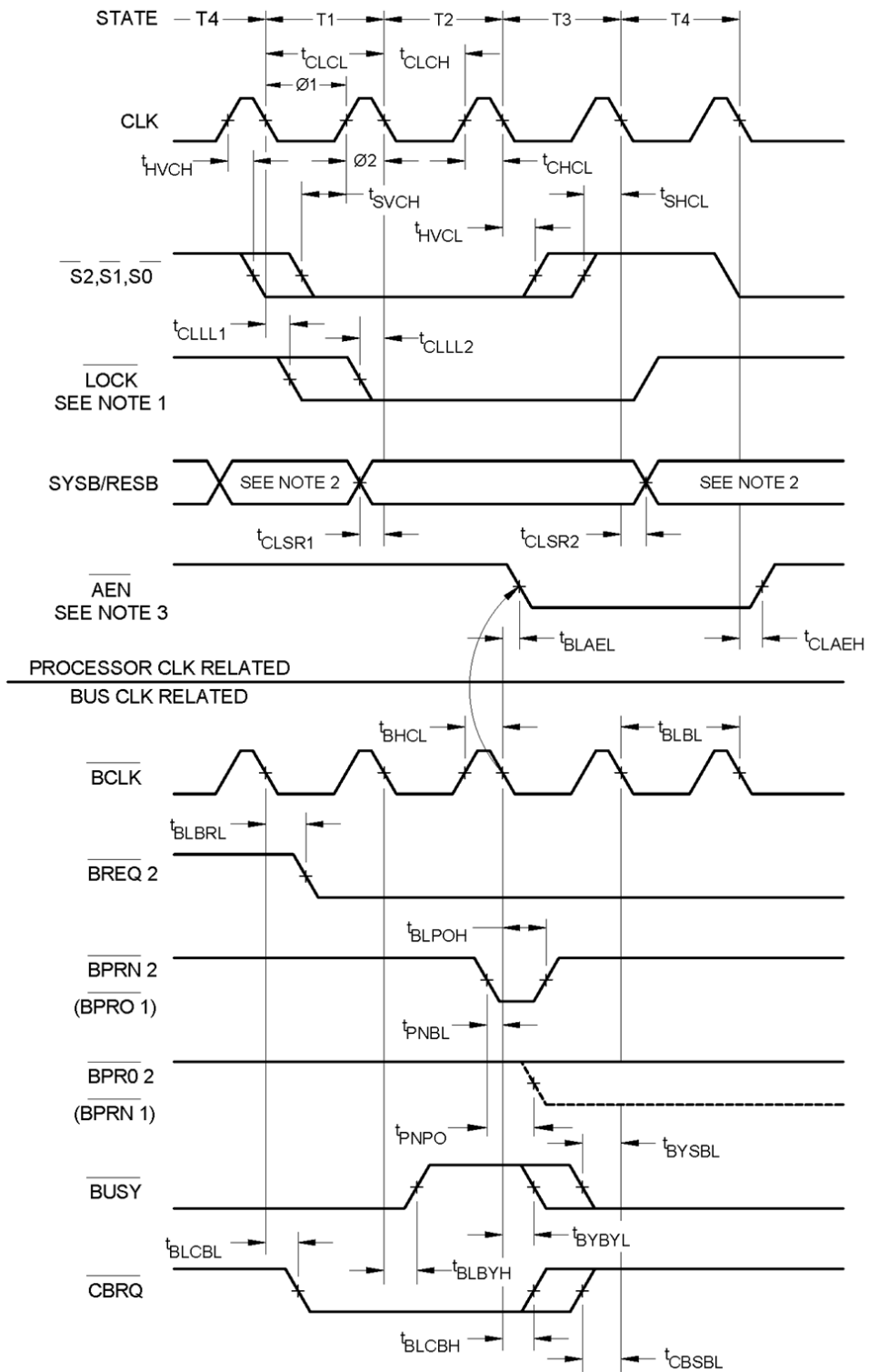


FIGURE 3. Switching waveforms.

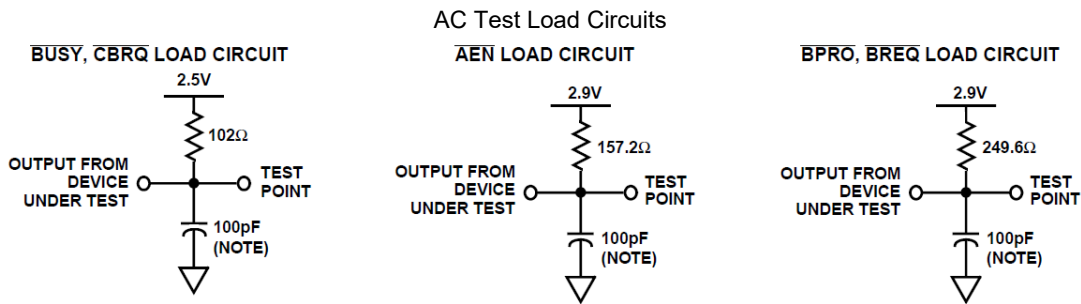
**STANDARD
MICROCIRCUIT DRAWING**
DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990

SIZE
A

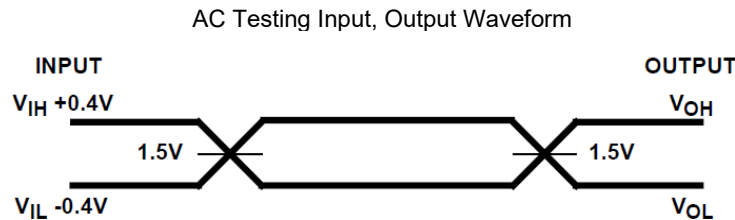
5962-85528

REVISION LEVEL
A

SHEET **10**



NOTE:
Includes stray and jig capacitance.



AC Testing: Inputs are driven at $V_{IH} + 0.4V$ for a logic "1" and $V_{IL} - 0.4V$ for a logic "0". The clock is driven at 4.1V and 0.4V. Timing measurements are made at 1.5V for both a logic "1" and "0".

NOTES:

1. \overline{LOCK} active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. \overline{LOCK} inactive has no critical time and can be asynchronous. \overline{CRQLCK} has no critical timing and is considered an asynchronous input signal.
2. Glitching of $\overline{SYSB}/\overline{RESB}$ is permitted during this time. After θ_2 of T1, and before θ_1 of T4, $\overline{SYSB}/\overline{RESB}$ should be stable to maintain system efficiency.
3. \overline{AEN} leading edge is related to \overline{BCLK} , trailing edge to CLK. The trailing edge of \overline{AEN} occurs after bus priority is lost.

ADDITIONAL NOTES:

The signals related to CLK are typical processor signals and do not relate to the depicted sequence of events of the signals referenced to \overline{BCLK} . The signals shown related to the \overline{BCLK} represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme. Assume arbiter 1 has the bus and is holding \overline{BUSY} low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{BREQ} \#2$. If $\overline{BPRN} \#2$ is high (as shown), arbiter #2 will pull low \overline{CBRQ} line. \overline{CBRQ} signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted \overline{BPRN} when it makes the bus request rather than having to wait for another arbiter to release the bus through \overline{CBRQ}].
*Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see table III), by lowering its $\overline{BPRO} \#1$ (tied to $\overline{BPRN} \#2$) and releasing \overline{BUSY} . Arbiter #2 now sees that it has priority from $\overline{BPRN} \#2$ being low and releases \overline{CBRQ} . As soon as \overline{BUSY} signifies the bus is available (high), arbiter #2 pulls \overline{BUSY} low on the next falling edge of \overline{BCLK} . Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{BPRO} \#2$ [t_{PNPO}].

*Note that even a higher priority arbiter which is acquiring the bus through \overline{BPRN} will momentarily drop \overline{CBRQ} until it has acquired the bus.

FIGURE 3. Switching waveforms – Continued.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A	REVISION LEVEL A	5962-85528 SHEET 11
--	------------------	----------------------------	--

TABLE III. Summary of modes, requesting and relinquishing the multi-master system bus.

SINGLE LINES FROM PROCESSOR				IOB MODE ONLY $\overline{\text{IOB}} = \text{LOW}$ $\text{RESB} = \text{LOW}$	RESB MODE ONLY $\overline{\text{IOB}} = \text{HIGH}, \text{RESB} = \text{HIGH}$		IOB MODE RESB MODE $\overline{\text{IOB}} = \text{LOW}, \text{RESB} = \text{HIGH}$		SINGLE BUS MODE $\overline{\text{IOB}} = \text{HIGH},$ $\text{RESB} = \text{LOW}$
$\overline{\text{S2}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	$\text{SYSB}/\overline{\text{RESB}} = \text{HIGH}$		$\text{SYSB}/\overline{\text{RESB}} = \text{LOW}$	$\text{SYSB}/\overline{\text{RESB}} = \text{HIGH}$	$\text{SYSB}/\overline{\text{RESB}} = \text{LOW}$		
I/O Commands	0	0	0	X	†	X	X	X	†
	0	0	1	X	†	X	X	X	†
	0	1	0	X	†	X	X	X	†
Halt	0	1	1	X	X	X	X	X	X
Memory Commands	1	0	0	†	†	X	†	X	†
	1	0	1	†	†	X	†	X	†
	1	1	0†	†	†	X	†	X	†
Idle	1	1	1	X	X	X	X	X	X

NOTES:

- X = Multi-master system bus is allowed to be Surrendered.
- † = Multi-master system bus is Requested.

TABLE III. Summary of modes, requesting and relinquishing the multi-master system bus – Continued.

MODE	PIN STRAPPING	MULTI-MASTER SYSTEM BUS	
		REQUESTED**	SURRENDERED*
Single Bus Multi-Master Mode	$\overline{\text{IOB}} = \text{High}, \text{RESB} = \text{Low}$	Whenever the processor's status lines go active	$\text{HLT} + \text{TI} \cdot \overline{\text{CBRQ}} + \text{HPBRQ} \ddagger$
RESB Mode Only	$\overline{\text{IOB}} = \text{High}, \text{RESB} = \text{High}$	$\text{SYSB}/\overline{\text{RESB}} + \text{High} \cdot \text{ACTIVE STATUS}$	$(\text{SYSB}/\overline{\text{RESB}} = \text{Low} + \text{TI}) \cdot \overline{\text{CBRQ}} + \text{HLT} + \text{HPBRQ}$
IOB Mode Only	$\overline{\text{IOB}} = \text{Low}, \text{RESB} = \text{Low}$	Memory Commands	$(\text{I/O Status} + \text{TI}) \cdot \overline{\text{CBRQ}} + \text{HLT} + \text{HPBRQ}$
IOB Mode RESB Mode	$\overline{\text{IOB}} = \text{Low}, \text{RESB} = \text{High}$	$(\text{Memory Command}) \cdot (\text{SYSB}/\overline{\text{RESB}} = \text{HIGH})$	$(\text{I/O Status Commands}) + (\text{SYSB}/\overline{\text{RESB}} = \text{Low}) \cdot \overline{\text{CBRQ}} + \text{HPBRQ} + \text{HLT}$

NOTES:

- * $\overline{\text{LOCK}}$ prevents surrender of bus to any other arbiter, $\overline{\text{CRQLCK}}$ prevents surrender of bus to any lower priority arbiter.
- ** Except for HALT and Passive or Idle Status.
- ‡ HPBRQ, High priority bus request or $\overline{\text{BPRN}} = 1$.
- 1. $\overline{\text{IOB}}$ Active Low.
- 2. RESB Active High.
- 3. + is read as "OR" and \cdot as "AND".
- 4. TI = Processor Idle Status $\overline{\text{S2}}, \overline{\text{S1}}, \overline{\text{S0}} = 111$.
- 5. HLT = Processor Halt Status $\overline{\text{S2}}, \overline{\text{S1}}, \overline{\text{S0}} = 011$.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 12

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn in test (method 1015 of MIL-STD-883).
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125\text{ }^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} , C_O , $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design which may affect input capacitance.

4.3.2 Groups C and D inspections.

- a. End point electrical parameters shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125\text{ }^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 13

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*,2,3,7,8,9,10,11
Group A test requirements (method 5005)	1,2,3,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8**,10
Additional electrical subgroups for group C periodic inspections	

* PDA applies to subgroup 1.

** Maximum operating temperature only.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Weapons Support when a system application requires configuration control and the applicable SMD to that system. DLA Weapons Support will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Weapons Support-VA, email VACChief@dla.mil.

6.5 Comments. Comments on this drawing should be directed to DLA Weapons Support-VA, Columbus, Ohio 43218-3990, or email VASChief@dla.mil.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Weapons Support-VA.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 14

6.7 Pin description.

SYMBOL	TYPE	NAME AND FUNCTION
V _{CC}		Power: +5V supply ±10%.
GND		Ground.
$\overline{S0}, \overline{S1}, \overline{S2}$	I	Status Input Pins: The status input pins from a processor. The arbiter decodes these pins to initiate bus request and surrender actions (See table III).
CLK	I	Clock: From the clock chip and serves to establish when bus arbiter actions are initiated.
\overline{LOCK}	I	Lock: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
\overline{CRQLCK}	I	Common Request Lock: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the \overline{CRQLCK} input pin.
RESB	I	Resident Bus: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/ \overline{RESB} input pin. Strapped low, the SYSB/ \overline{RESB} input is ignored.
ANYRQST	I	Any Request: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to table I. If ANYRQST is strapped high and \overline{CBRQ} is activated, the bus is surrendered at the end of the present bus cycle. Strapping \overline{CBRQ} low and ANYRQST high forces the arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs \overline{BREQ} is driven false (high).
\overline{IOB}	I	IO Bus: A strapping option which configures the arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
\overline{AEN}	O	Address Enable: The output of the Arbiter to the processor's address latches, to the Bus Controller and Clock Generator. \overline{AEN} serves to instruct the Bus Controller and address latches when to three-state their output drivers.
\overline{INIT}	I	Initialize: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 15

6.7 Pin description – Continued.

SYMBOL	TYPE	NAME AND FUNCTION
$\overline{\text{SYSB}}/\overline{\text{RESB}}$	I	System Bus/Resident Bus: An input signal when the arbiter is configured in the System/Resident Mode (RESB is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from $\theta 1$ of T4 to $\theta 1$ of T2 of the processor cycle. During the period from $\theta 1$ of T2 to $\theta 1$ of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the $\overline{\text{SYSB}}/\overline{\text{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\text{CBRQ}}$	I/O	Common Bus Request: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\text{CBRQ}}$ pins (open-drain output) of all the Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\text{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\text{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\text{BREQ}}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{\text{CBRQ}}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\text{BCLK}}$	I	Bus Clock: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{\text{BREQ}}$	O	Bus Request: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	I	Bus Priority In: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{\text{BCLK}}$. $\overline{\text{BPRN}}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{\text{BPRO}}$	O	Bus Priority Out: An active low output signal used in the serial priority resolving scheme where $\overline{\text{BPRO}}$ is daisy-chained to $\overline{\text{BPRN}}$ of the next lower priority arbiter.
$\overline{\text{BUSY}}$	I/O	Busy: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{\text{BPRN}}$) seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{\text{BUSY}}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

STANDARD MICROCIRCUIT DRAWING DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990	SIZE A		5962-85528
		REVISION LEVEL A	SHEET 16

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 26-03-19

Approved sources of supply for SMD 5962-85528 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Weapons Support-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Weapons Support maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8552801RX	<u>3/</u>	MD82C89/B
5962-8552801RA	0DKS7	GEM49301QRA
5962-85528012X	<u>3/</u>	MR82C89/B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

0DKS7

Vendor name
and address

SRI International
201 Washington Road
Princeton, NJ 08540-6449

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.