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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY Greg A. Pitz	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY Mick Saunders	
Original date of drawing: 19 November 1986	APPROVED BY Mick Saunders	TITLE: MICROCIRCUIT, DIGITAL, CMOS, BUS ARBITER, MONOLITHIC SILICON
	SIZE A / CODE IDENT. NO. 14933	DWG NO. 5962-85528
AMSC N/A	REV	PAGE 1 OF 15

5962-E853

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85528	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish (3.3)

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	82C89	8 MHz	CMOS Bus Arbiter

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1/4" x 1-1/16"), dual-in-line package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+8.0 V 1/
Input, output or I/O voltage applied	GND-0.5 V to V_{CC}+0.5 V 1/
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C
Temperature under bias	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Maximum package power dissipation, (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum frequency of operation (f_{MAX})	0 to 8.0 MHz
Setup time, status active (t_{SVCH})	t_{CLCL} -10 ns maximum 3/
Setup time, status inactive (t_{SHCL})	t_{CLCL} -10 ns maximum 3/
BCLK high time (t_{BHCL})	.65 t_{BLBL} maximum 3/
Delay time, BCLK to CBRQ float (t_{BLBYH})	35 ns maximum
Delay time, BCLK to BUSY float (t_{BLBYH})	35 ns maximum
Input rise time (t_r)	20 ns maximum
Input fall time (t_f)	20 ns maximum

1/ All voltages referenced to V_{SS}.
2/ V_{CC} = 4.5 V and 5.5 V.
3/ See table I for minimum limits.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

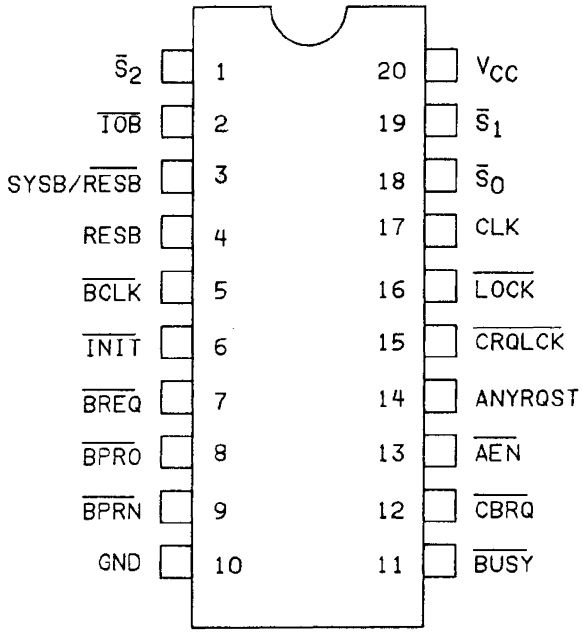
3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

Case R



Case 2

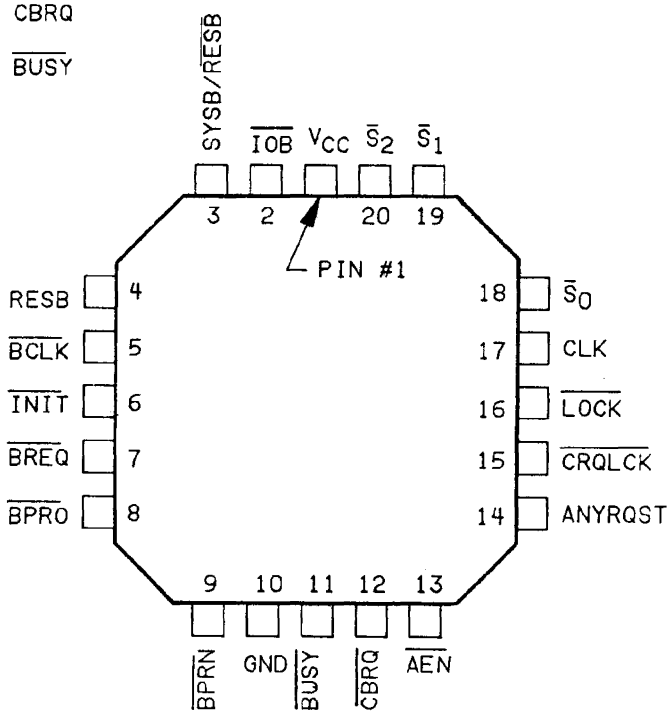


FIGURE 1. Terminal connections (top view).

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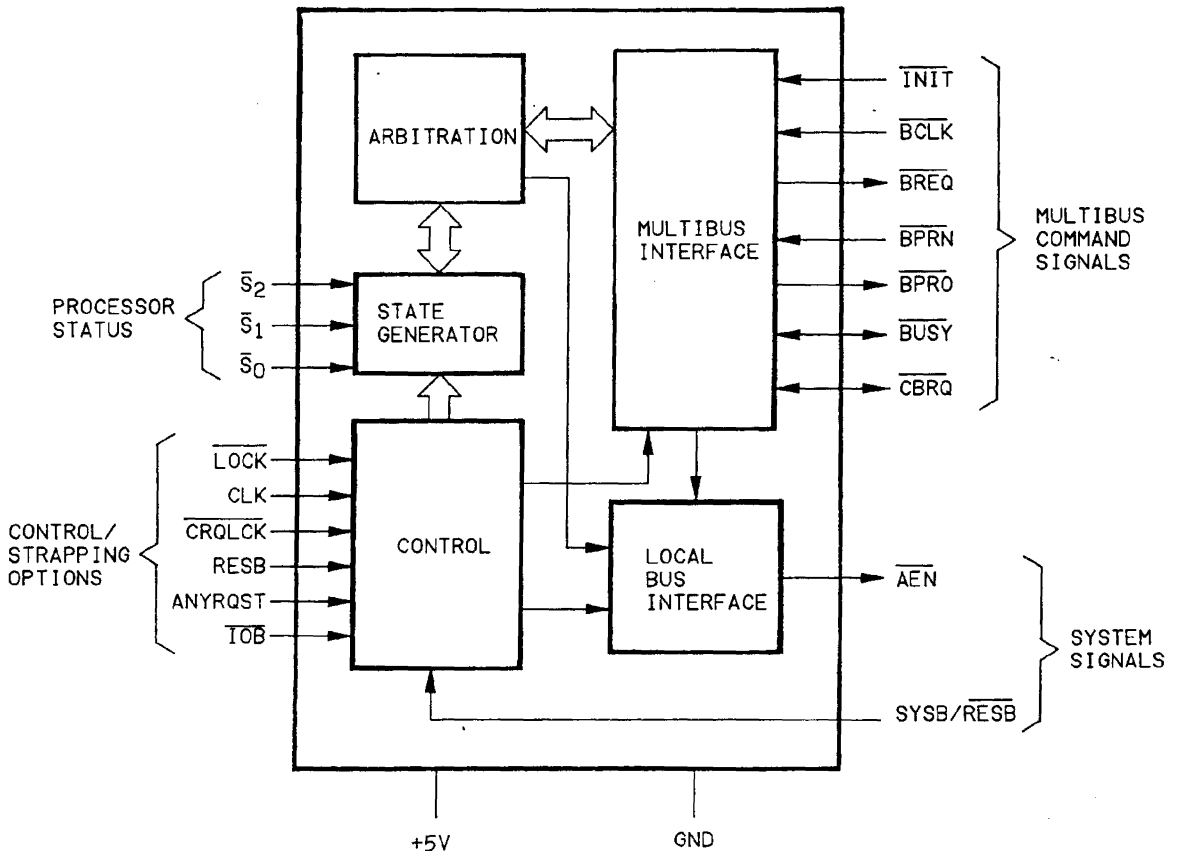

FIGURE 2. Functional block diagram.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}	V_{CC} = 5.5 V	1, 2, 3	2.2		V
Input low voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3		0.8	V
Input high clock voltage	V_{IHC}	V_{CC} = 5.5 V	1, 2, 3	70% V_{CC}		V
Input low clock voltage	V_{ILC}	V_{CC} = 4.5 V	1, 2, 3		20% V_{CC}	V
Output low voltage ($\overline{BUSY}$, $\overline{CBRQ}$)	V_{OL1}	V_{CC} = 4.5 V, I_{OL} = 20 mA, Test pins 11 and 12	1, 2, 3		0.45	V
Output low voltage ($\overline{AEN}$)	V_{OL2}	V_{CC} = 4.5 V, I_{OL} = 16 mA, Test pin 13	1, 2, 3		0.45	V
Output low voltage ($\overline{BPRO}$, $\overline{BREQ}$)	V_{OL3}	V_{CC} = 4.5 V, I_{OL} = 10 mA, Test pins 7 and 8	1, 2, 3		0.45	V
Output high voltage ($\overline{BUSY}$, $\overline{CBRQ}$)	V_{OH1}	V_{CC} = 4.5 V, Open drain, Test pins 11 and 12	1, 2, 3			V
Output high voltage (All others)	V_{OH2}	V_{CC} = 4.5 V, I_{OH} = -2.5 mA, Test pins 7-8 and 13	1, 2, 3	3.0		V
Output high voltage (All others)	V_{OH3}	V_{CC} = 4.5 V, I_{OH} = -100 uA, Test pins 7-8 and 13	1, 2, 3	V_{CC} -0.4		V
Input leakage current	I_I	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}, Test pins 1-6, 9, 14-19	1, 2, 3	-1.0	1.0	uA
I/O leakage current ($\overline{BUSY}$, $\overline{CBRQ}$)	I_O	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}, Test pins 11-12	1, 2, 3	-10	10	uA
Standby supply current	I_{CCSB}	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}, Outputs open	1, 2, 3		10	uA
Operating supply current	I_{CCOP}	V_{CC} = 5.5 V, f = 1 MHz, Outputs open, 2/	1, 2, 3		1.0	mA/MHz
Input capacitance	C_{IN}	T_C = +25°C, f = 1 MHz	4		10	pF
Output capacitance	C_O		4		10	pF
I/O capacitance	$C_{I/O}$		4		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Functional test	FT	V_{CC} = 4.5 V and 5.5 V, 3/	7, 8			
CLK cycle time	t_{CLCL}	V_{CC} = 4.5 V and 5.5 V	9, 10, 11	125		ns
CLK low time	t_{CLCH}		9, 10, 11	55		ns
CLK high time	t_{CHCL}		9, 10, 11	35		ns
Status active setup time	t_{SVCH}		9, 10, 11	65	4/	ns
Status inactive setup time	t_{SHCL}		9, 10, 11	50	4/	ns
Status active hold time	t_{HVCH}		9, 10, 11	10		ns
Status inactive hold time	t_{HVCL}		9, 10, 11	10		ns
$\overline{BUSY}$** setup to $\overline{BCLK}$ 5/	t_{BYSBL}		9, 10, 11	20		ns
$\overline{CBRQ}$** setup to $\overline{BCLK}$ 5/	t_{CBSBL}		9, 10, 11	20		ns
$\overline{BCLK}$ cycle time	t_{BLBL}		9, 10, 11	100		ns
$\overline{BCLK}$ high time	t_{BHCL}		9, 10, 11	30	4/	ns
$\overline{LOCK}$ inactive hold time	t_{CLLL1}		9, 10, 11	10		ns
$\overline{LOCK}$ active setup time	t_{CLLL2}		9, 10, 11	40		ns
$\overline{BPRN}$** to $\overline{BCLK}$ setup time 5/	t_{PNBL}		9, 10, 11	15		ns
SYSB/$\overline{RESB}$ setup time	t_{CLSR1}		9, 10, 11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
SYSB/$\overline{RESB}$ hold time	t_{CLSR2}	V_{CC} = 4.5 V and 5.5 V	9, 10, 11	30		ns
Initialization pulse width	t_{IVIH}		9, 10, 11	575		ns
$\overline{BCLK}$ to $\overline{BREQ}$** delay time 5/	t_{BLBRL}		9, 10, 11		35	ns
$\overline{BCLK}$ to $\overline{BPRO}$** 5/ 6/	t_{BLPOH}		9, 10, 11		40	ns
$\overline{BPRN}$** to $\overline{BPRO}$** 5/ 6/ delay time	t_{PNPO}		9, 10, 11		25	ns
$\overline{BCLK}$ to $\overline{BUSY}$ low	t_{BLBYL}		9, 10, 11		60	ns
CLK to $\overline{AEN}$ high	t_{CLAEH}		9, 10, 11		65	ns
$\overline{BCLK}$ to $\overline{AEN}$ low	t_{BLAEL}		9, 10, 11		40	ns
$\overline{BCLK}$ to $\overline{CBRQ}$ low	t_{BLCBL}		9, 10, 11		60	ns
Output rise time	t_{OLOH}	V_{CC} = 4.5 V and 5.5 V, 7/, From 0.8 V to 2.0 V	9, 10, 11		20	ns
Output fall time	t_{OHOL}	V_{CC} = 4.5 V and 5.5 V, 7/, From 2.0 V to 0.8 V	9, 10, 11		12	ns

1/ During AC testing, input waveforms must switch between V_{IH}+0.4 V and V_{IL}-0.4 V. Input rise and fall times are driven at 1ns/V. Loading is per appropriate AC test circuit (see figure 3).
2/ Maximum current defined by CLK or BCLK, whichever has the highest operating frequency.
3/ Tested as follows: f = 1 MHz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, Load per appropriate AC test circuit, $V_{OH} \ge 1.5$ V, and $V_{OL} \le 1.5$ V.
4/ Reference paragraph 1.4 for this limit.
5/ Both transistions of the signal apply to parameters with asterisks (**).
6/ $\overline{BCLK}$ generates the first $\overline{BPRO}$ wherein subsequent $\overline{BPRO}$ changes lower in the chain are generated through BPRON.
7/ Except $\overline{BUSY}$ and $\overline{CBRQ}$.

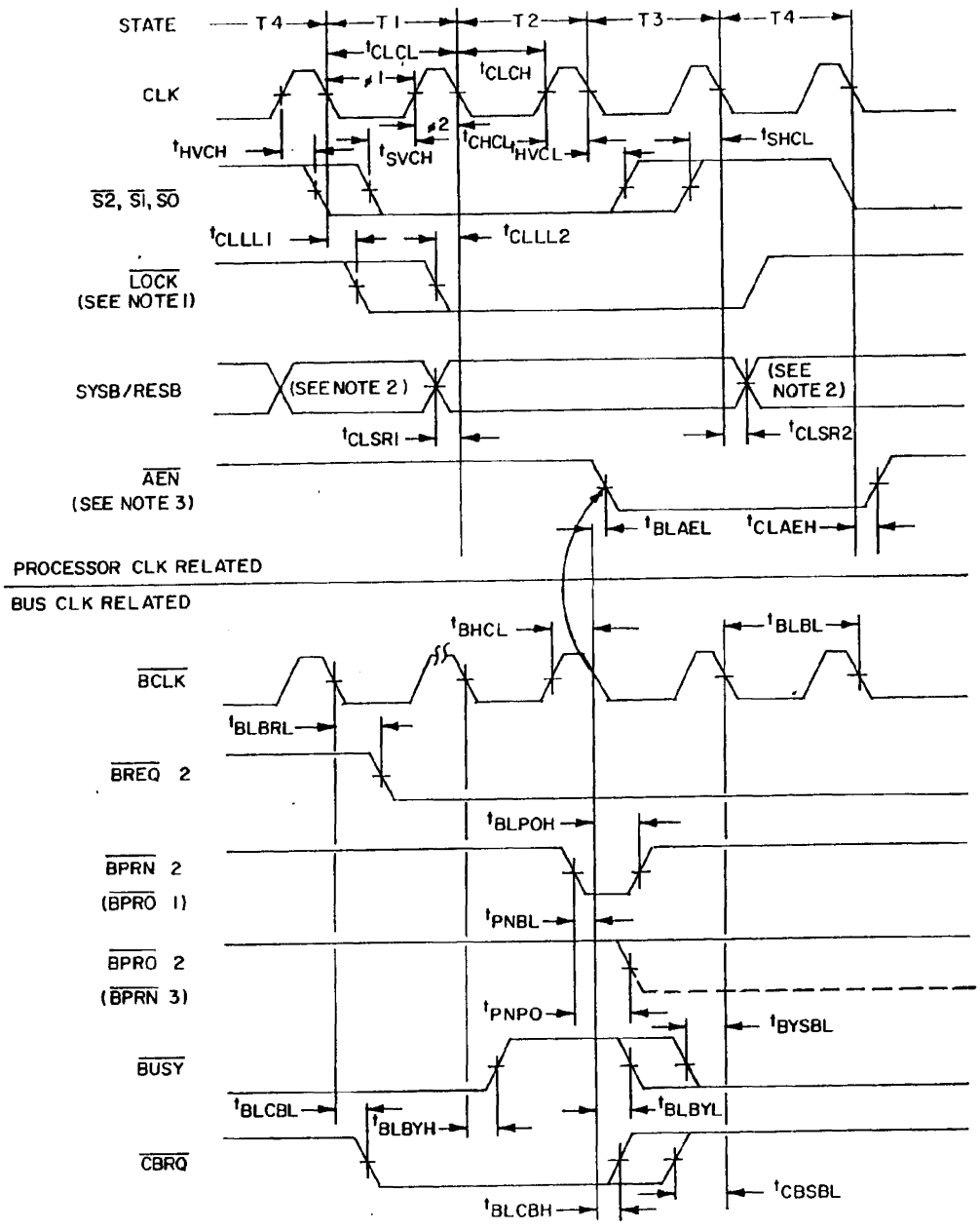

FIGURE 3. Switching waveforms.

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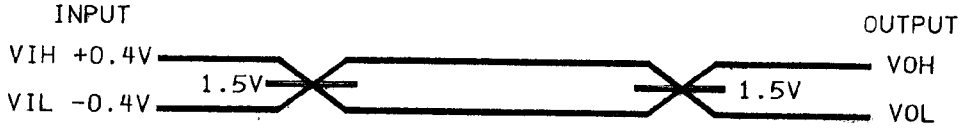
A.C. Testing: Inputs are driven at VIH +0.4V for a logic "1" and VIL -0.4V for a logic "0". The clock is driven at 4.1 V and 0.4 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

AC testing input, output waveform



AC testing: Inputs are driven at VIH +0.4 V

NOTES:

1. Lock active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. LOCK inactive has no critical time and can be asynchronous $\overline{\text{CRQLCK}}$ has no critical timing and is considered an asynchronous input signal.

2. Glitching of SYSB/RESB is permitted during this time. After ø2 of T1, and before ø1 of T4, SYSB/$\overline{\text{RESB}}$ should be stable to maintain system efficiency.

3. $\overline{\text{AEN}}$ leading edge is related to $\overline{\text{BCLK}}$, training edge to CLK. The training edge of $\overline{\text{AEN}}$ occurs after bus priority is lost.

ADDITIONAL NOTES:

The signals related to CLK are typical processor signals and do not relate to the depicted sequence of events of the signals referenced to $\overline{\text{BCLK}}$. The signals shown related to the $\overline{\text{BCLK}}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme (as shown in figure 3). Assume arbiter 1 has the bus and is holding BUSY low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{\text{BREQ}}$ #2. If $\overline{\text{BPRN}}$ #2 is high (as shown) arbiter #2 will pull low $\overline{\text{CPRQ}}$ line $\overline{\text{CBRQ}}$ signals to the higher priority arbiter α1 that a lower priority arbiter wants the bus (A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{\text{CBRQ}}$). Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see table 1), by lowering its $\overline{\text{BPRO}}$ #1 (tied to $\overline{\text{BPRN}}$ #2) and releasing BUSY arbiter #2 now sees that is has priority from BPRN α2 being low and releases $\overline{\text{CBRQ}}$. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{\text{BPRO}}$ #2 (TPNPO).

*Note that even a higher priority arbiter which is acquiring the bus through $\overline{\text{BPRN}}$ will momentarily drop $\overline{\text{CBRQ}}$ until it has acquired the bus.

FIGURE 3. Switching waveforms - Continued.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_O, $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8**,10
Additional electrical subgroups for group C periodic inspections	

* PDA applies to subgroup 1.
**Maximum operating temperature only.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin description.

SYMBOL	TYPE	NAME AND FUNCTION
V_{CC}		Power: +5 V supply ±10%.
GND		Ground.
$\overline{S0}, \overline{S1}, \overline{S2}$	I	Status Input Pins: The status input pins from a processor. The arbiter decodes these pins to initiate bus request and surrender actions.
CLK	I	Clock: From the clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	I	Lock: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	I	Common Request Lock: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	I	Resident Bus: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	I	Any Request: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table I. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	I	IO Bus: A strapping option which configures the arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line. $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	O	Address Enable: The output of the Arbiter to the processor's address latches, to the Bus Controller and Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to three-state their output drivers.
$\overline{INIT}$	I	Initialize: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.

6.4 Pin description - (Continued)

SYMBOL	TYPE	NAME AND FUNCTION
SYSB/ $\overline{\text{RESB}}$	I	System Bus/Resident Bus: An input signal when the arbiter is configured in the System/Resident Mode (RESB is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from o1 of T4 to o1 of T2 of the processor cycle. During the period from o1 of T2 to o1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the SYSB/$\overline{\text{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\text{CBRQ}}$	I/O	Common Bus Request: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\text{CBRQ}}$ pins (open-drain output) of all the Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\text{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\text{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\text{BREQ}}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{\text{CBRQ}}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\text{BCLK}}$	I	Bus Clock: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{\text{BREQ}}$	O	Bus Request: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	I	Bus Priority In: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{\text{BCLK}}$. $\overline{\text{BPRN}}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{\text{BPRO}}$	O	Bus Priority Out: An active low output signal used in the serial priority resolving scheme where $\overline{\text{BPRO}}$ is daisy-chained to $\overline{\text{BPRN}}$ of the next lower priority arbiter.
$\overline{\text{BUSY}}$	I/O	Busy: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{\text{BPRN}}$) seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{\text{BUSY}}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8552801RX	34371	MD82C89/B	
5962-85528012X	34371	MR82C89/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901