REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Revise table I limits. Revise figure 3 waveforms. Make editorial changes.	87-03-16	N. A. Hauck
B	Updated boilerplate and added Intersil as source of supply CAGE code 34371. - LTG	00-08-09	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 requirements. - LTG	01-06-05	Thomas M. Hess
D	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-07-06	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-10-21	Muhammad A. Akbar

REV																				
SHEET																				
REV	E																			
SHEET	15																			

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Greg A. Pitz

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
86-06-18

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, CMOS, PROGRAMMABLE INTERRUPT CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-85016**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-85016	01	Y	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	82C59A-5	5 MHz	CMOS programmable interrupt controller
02	82C59A	8 MHz	CMOS programmable interrupt controller

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground) ..... +8.0 V dc 1/
Input, output, or I/O voltage applied ..... GND -0.5 V dc to V_{CC} +0.5 V dc
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1 W
Lead temperature (soldering, 10 seconds) ..... +275°C
Maximum junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Temperature under bias ..... -55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc 1/
Case operating temperature range (T_C) ..... $-55°C \le T_C \le +125°C$
Frequency of operation:
  Device type 01 ..... 5 MHz
  Device type 02 ..... 8 MHz
Data float after $\overline{RD}/\overline{INTA}$ (t_{RHDZ}) reference number 14: 2/
  Device type 01 ..... 10 ns minimum, 100 ns maximum
  Device type 02 ..... 10 ns minimum, 85 ns maximum

1/ All voltages are referenced to V_{SS}.
2/ The reference number refers to the parameter being measured on figure 3. The parameter being measured uses test condition 2 on figure 4.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.2.5 AC test circuit and waveform. The AC test circuit and waveform shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Ref no. 1/	Group A subgroups	Limits		Unit
							Min	Max	
High level output voltage 2/	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5 V		All		1, 2, 3	3.0		V
	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5 V		All		1, 2, 3	V_{CC} -0.4		V
Low level output voltage 2/	V_{OL}	I_{OL} = +2.5 mA, V_{CC} = 4.5 V		All		1, 2, 3		0.4	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V		All		1, 2, 3	2.2		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		All		1, 2, 3		0.8	V
Input leakage current	I_{IN}	V_{CC} = 5.5 V	V_{IN} = 0.0 V	All		1, 2, 3	-1.0		µA
			V_{IN} = V_{CC}	All		1, 2, 3		1.0	
Input/output leakage current	$I_{I/O}$	V_{CC} = 5.5 V	V_{IN} = 0.0 V	All		1, 2, 3	-10		µA
			V_{IN} = V_{CC}	All		1, 2, 3		10	
Standby power supply current	I_{CCSB}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND 3/ Outputs open		All		1, 2, 3		10	µA
IR input load current	I_{LIR}	V_{IN} = 0.0 V, V_{CC} = 5.5 V		All		1, 2, 3		-500	µA
		V_{IN} = V_{CC}, V_{CC} = 5.5 V		All		1, 2, 3		10	µA
Functional tests		See 4.3.1d 4/ V_{CC} = 4.5 V and 5.5 V		All		7, 8			
Input capacitance	C_{IN}	FREQ = 1 MHz		Case Y		4		15	pF
		T_C = +25°C		Case 3		4		7	pF
Output capacitance	C_{OUT}	See 4.3.1c		Case Y		4		15	pF
		All measurements referenced to device ground		Case 3		4		7	pF
I/O capacitance	$C_{I/O}$			Case Y		4		15	pF
				Case 3		4		7	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Ref no. 1/	Group A subgroups	Limits		Unit
						Min	Max	
A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}$	t_{AHRL}	V_{CC} = 4.5 V and 5.5 V 4/	01, 02	1	9, 10, 11	10		ns
A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}$	t_{RHAX}		01, 02	2	9, 10, 11	5		ns
$\overline{RD}$/$\overline{INTA}$ pulse width	t_{RLRH}		01	3	9, 10, 11	235		ns
			02	3	9, 10, 11	160		ns
A0/$\overline{CS}$ setup to $\overline{WR}$	t_{AHWL}		01, 02	4	9, 10, 11	0		ns
A0/$\overline{CS}$ hold after $\overline{WR}$	t_{WHAX}		01, 02	5	9, 10, 11	5		ns
$\overline{WR}$ pulse width	t_{WLWH}		01	6	9, 10, 11	165		ns
			02	6	9, 10, 11	95		ns
Data setup to $\overline{WR}$	t_{DVWH}		01	7	9, 10, 11	240		ns
			02	7	9, 10, 11	160		ns
Data hold after $\overline{WR}$	t_{WHDX}		01, 02	8	9, 10, 11	5		ns
Interrupt request width (Lo) 5/	t_{JLJH}		01, 02	9	9, 10, 11	100		ns
Cascade setup to second or third $\overline{INTA}$ (slave only)	t_{CVIAL}		01	10	9, 10, 11	55		ns
			02	10	9, 10, 11	40		ns
End of $\overline{RD}$ to next $\overline{RD}$, end of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	t_{RHRL}		01, 02	11	9, 10, 11	160		ns
End of $\overline{WR}$ to next $\overline{WR}$	t_{WHWL}		01, 02	12	9, 10, 11	190		ns
End of command to next command (not same command type), end of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence 6/	t_{CHCL}		01	21	9, 10, 11	500		ns
			02	21	9, 10, 11	400		ns
Data valid from $\overline{RD}$/$\overline{INTA}$ 7/	t_{RLDV}		01	13	9, 10, 11		160	ns
			02	13	9, 10, 11		120	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Ref no. 1/	Group A subgroups	Limits		Unit
						Min	Max	
Interrupt output delay	t_{JHIH}	V_{CC} = 4.5 V and 5.5 V 4/ 7/	01	15	9, 10, 11		350	ns
			02	15	9, 10, 11		300	ns
Cascade valid from first $\overline{INTA}$ (Master only)	t_{IALCV}		01	16	9, 10, 11		565	ns
			02	16	9, 10, 11		360	ns
Enable active from $\overline{RD}$ or $\overline{INTA}$	t_{RLEL}		01	17	9, 10, 11		125	ns
			02	17	9, 10, 11		100	ns
Enable inactive from $\overline{RD}$ or $\overline{INTA}$	t_{RHEH}		01	18	9, 10, 11		60	ns
			02	18	9, 10, 11		50	ns
Data valid from stable address	t_{CVDV}		01	19	9, 10, 11		300	ns
			02	19	9, 10, 11		200	ns
Cascade valid to valid data	t_{AHDV}		01	20	9, 10, 11		210	ns
			02	20	9, 10, 11		200	ns

1/ The reference number refers to the parameter being measured on figure 3.
2 Interchanging of force and sense conditions are permitted.
3/ For IR0-IR7 pins, $V_{IN} = V_{CC}$ or open.
4/ Tested as follows: f = 1 MHz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, $V_{OH} \ge 1.5$ V, $V_{OL} \le 1.5$ V and C_L 50 pF unless otherwise noted. Circuits and waveforms are shown on figure 4.
5/ This is the low time required to clear the input latch in the edge triggered mode.
6/ Worst case timing for reference number 21 (t_{CHCL}) in an actual microprocessor system is typically much greater than the limits shown.
7/ The parameter being measured uses test condition 1 on figure 4.

Device types	01 and 02
Case outlines	Y and 3
Terminal number	Terminal symbol
1	$\overline{CS}$
2	$\overline{WR}$
3	$\overline{RD}$
4	D_7
5	D_6
6	D_5
7	D_4
8	D_3
9	D_2
10	D_1
11	D_0
12	CAS 0
13	CAS 1
14	GND
15	CAS 2
16	$\overline{SP}/\overline{EN}$
17	INT
18	IR0
19	IR1
20	IR2
21	IR3
22	IR4
23	IR5
24	IR6
25	IR7
26	$\overline{INTA}$
27	A_0
28	V_{CC}

FIGURE 1. Terminal connections.

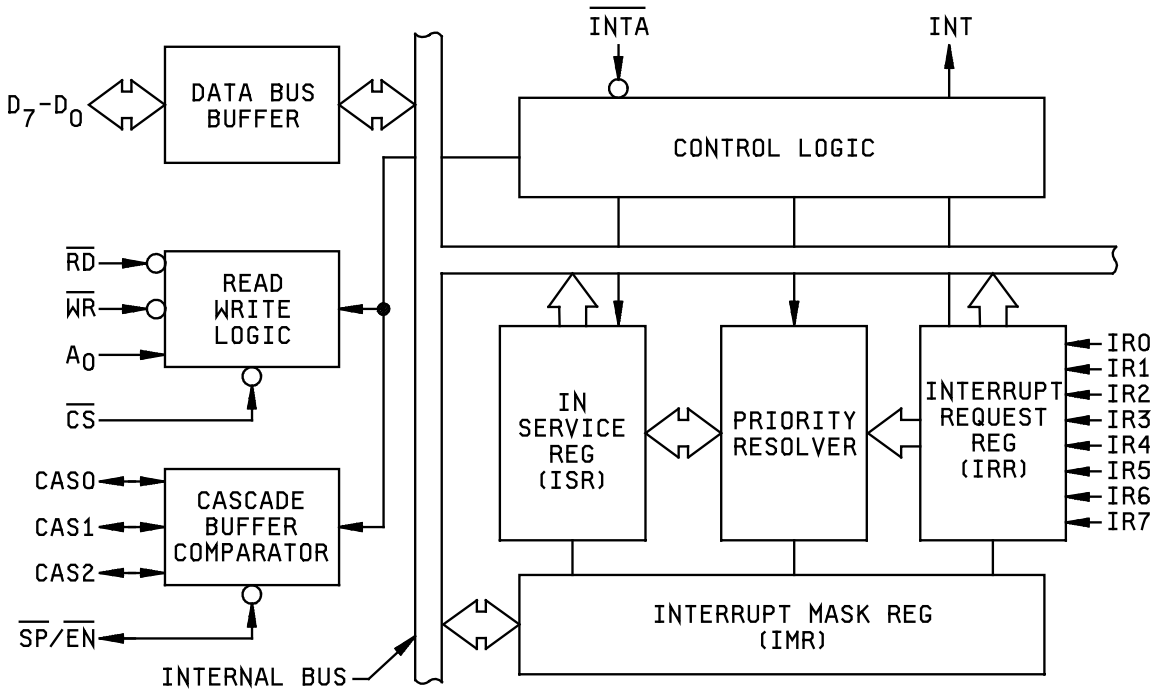
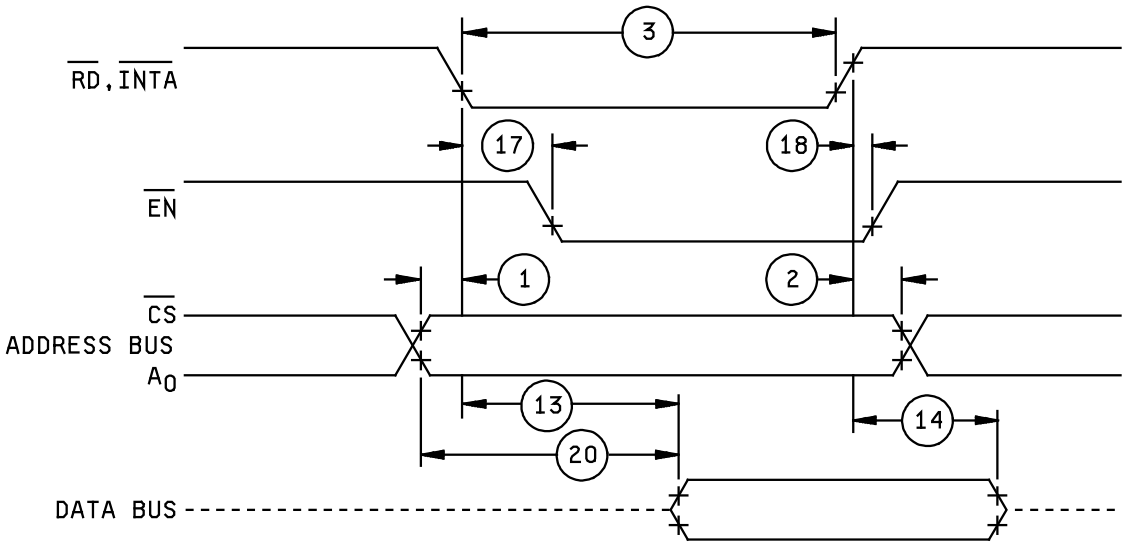


FIGURE 2. Functional block diagram.

Read/Interrupt Acknowledge cycle



Write cycle

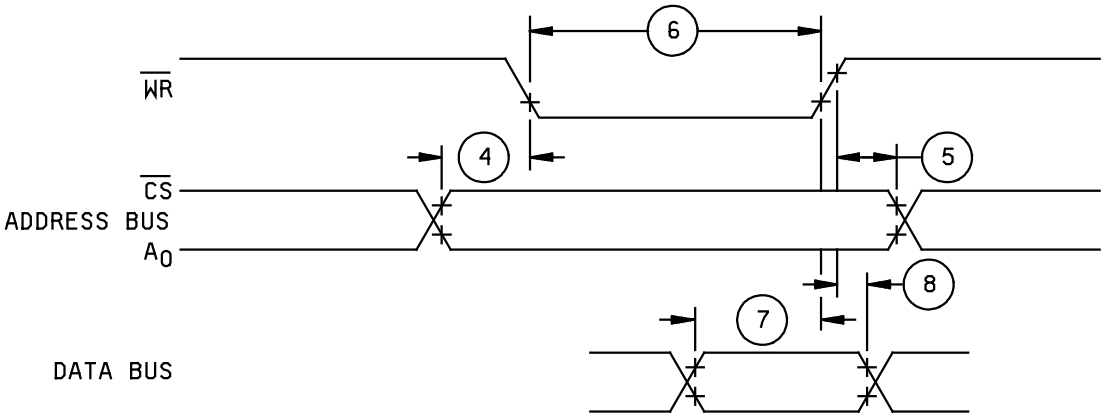
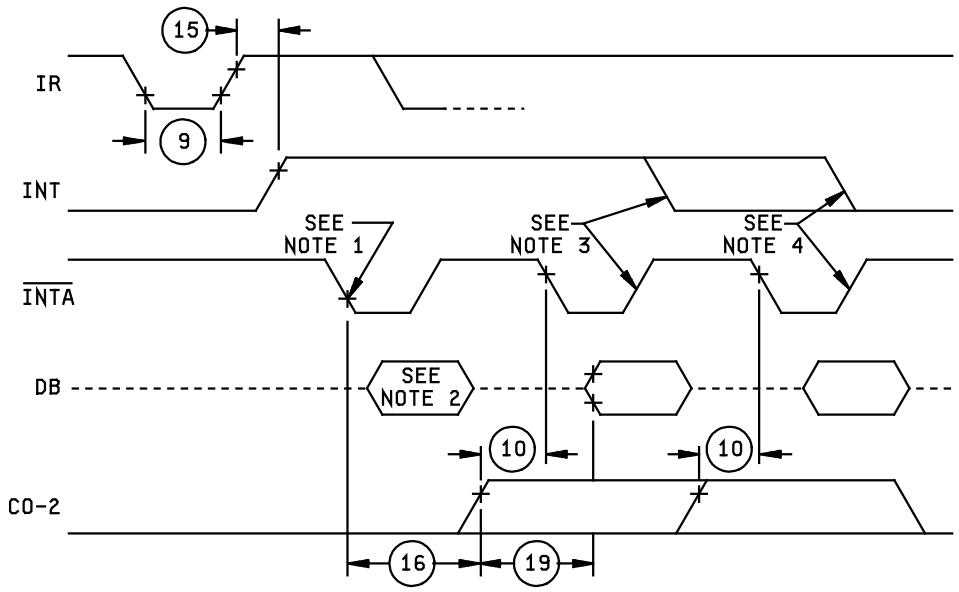


FIGURE 3. Switching waveforms.

Interrupt Acknowledge sequence



NOTES:
1. Interrupt request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
2. During the first $\overline{\text{INTA}}$, the DATA Bus is not active in 80C86/80C88 mode.
3. 80C86/80C88 mode.
4. 8080/8085 mode.

Other timing

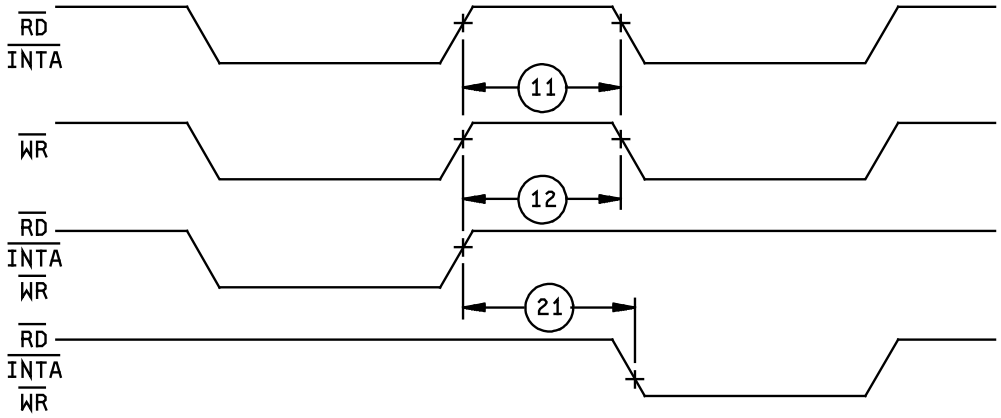
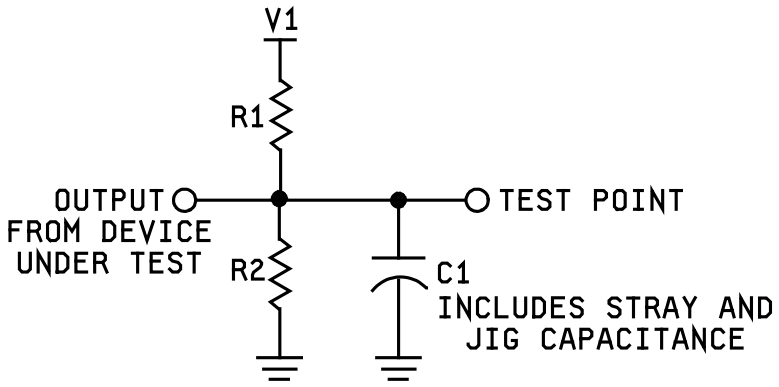
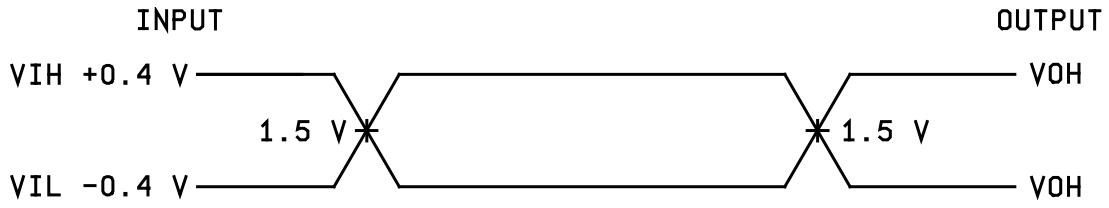


FIGURE 3. Switching waveforms - Continued.



Test Condition	V1	R1	R2	C1 Min
1	1.7 V	523Ω	OPEN	100 pF
2	V_{CC}	1.8 kΩ	1.8 kΩ	30 pF

Test Condition Definition Table



NOTE: AC Testing: All input signals must switch between V_{IL} – 0.4 V and V_{IH} + 0.4 V.
t_r and t_f are driven at 1.0 ns/V.

FIGURE 4. AC test circuit and waveform.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (+125°C only), 10

1/ PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-8108.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Pin descriptions. For pin descriptions, see table III herein.

TABLE III. Pin descriptions.

Symbol	Description
$\overline{RD}$	READ: A low on this pin when $\overline{CS}$ is low enables the device to release status onto the data bus for the CPU.
$\overline{WR}$	WRITE: A low on this pin when $\overline{CS}$ is low enables the device to accept command words from the CPU.
$\overline{CS}$	CHIP SELECT: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the device. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{INTA}$	INTERRUPT ACKOWLEDGE: This pin is used to enable device interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the buffered mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
D_7-D_0	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via this bus.
CAS0-CAS2	CASCADE LINES: The CAS lines from a private device bus to control a multiple device structure. These pins are outputs for a master device and inputs for a slave device.
INT	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
A_0	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the device to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for 80C86/88).
GND	GROUND: Ground.
V_{CC}	POWER SUPPLY: +5 V Supply pin. A 0.1 μF capacitor between V_{CC} and GND is recommended for decoupling.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-10-21

Approved sources of supply for SMD 5962-85016 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8501601YA	34371	MD82C59A-5B
5962-85016013A	3/	MR82C59A-5B
5962-8501602YA	34371	MD82C59A/B
5962-85016023A	34371	MR82C59A/B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	RENESAS Electronics INC. 1650 Robert J. Conlan Blvd. Palm Bay, FL 32905