

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Changes to recommended operating conditions, table I, and table II. Convert to military drawing format. Editorial changes throughout. Add device type 02. Add vendor CAGE 34649.	87-02-27	N. A. Hauck
C	Changes in accordance with NOR 5962-R053-93.	92-12-18	Monica L. Poelking
D	Changes in accordance with NOR 5962-R077-95.	95-04-19	Monica L. Poelking
E	Update boilerplate to MIL-PRF-38535 requirements. Correct drawing title to indicate device function. - CFS	03-08-05	Thomas M. Hess
F	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. - PHN.	05-03-17	Thomas M. Hess
G	Change IBHH and IBHL maximum limits in table I from -400 uA and 400 uA, respectively, to -450 uA and 450 uA, respectively, at -55C. - CFS.	06-11-06	Thomas M. Hess
H	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-08-06	Thomas M. Hess
J	Update boilerplate to current MIL-PRF-38535 requirements. - DRH	26-01-21	Muhammad A. Akbar

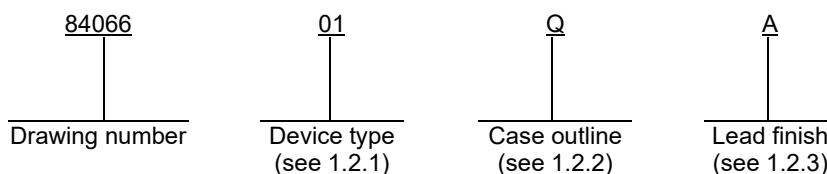


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REV	J	J	J	J																
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REV STATUS				REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
PMIC N/A					PREPARED BY	Greg A. Pitz				<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime</p> <p align="center">MICROCIRCUIT, DIGITAL, CMOS, PROGRAMMABLE PERIPHERAL INTERFACE, MONOLITHIC SILICON</p>										
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>					CHECKED BY	D. A. DiCenzo														
					APPROVED BY	N. A. Hauck														
					DRAWING APPROVAL DATE	84-12-03														
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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Frequency</u>	<u>Circuit function</u>
01	82C55A-5/B	5.0 MHz	Programmable peripheral interface
02	82C55A/B	8.0 MHz	Programmable peripheral interface

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) (Referenced to ground)	+8.0 V dc maximum
Input, output, or I/O applied voltage range	GND - 0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) ^{1/}	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Maximum junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-STD-1835
Case X	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Frequency of operation:	
Device type 01	0 to 5.0 MHz
Device type 02	0 to 8.0 MHz
Operating supply current (I_{CCOP})	10 mA maximum ^{2/}
Data float after READ (t_{DF}) (5) ^{3/}	10 ns minimum to 75 ns maximum
ACK = 1 to output float (t_{KD}) (23) ^{3/}	20 ns minimum to 250 ns maximum

^{1/} Must withstand the added P_D due to short circuit test e.g., I_{OS} .

^{2/} I_{CCOP} = 1 mA/MHz of peripheral read/write cycle time (ie: 1.0 μ s I/O read/write cycle time = 1 mA).

^{3/} See waveforms on figure 3 and test condition 2 on figure 3.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = +4.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V _{IH}	V _{CC} = 5.5 V	1, 2, 3	All	2.2		V
Low level input voltage	V _{IL}		1, 2, 3	All		0.8	V
High level output voltage	V _{OH}	I _{OH} = -2.5 mA <u>1/</u>	1, 2, 3	All	3.0		V
		I _{OH} = -100 μA <u>1/</u>			V _{CC} -0.4		
Low level output voltage	V _{OL}	I _{OL} = +2.5 mA <u>1/</u>	1, 2, 3	All		0.4	V
Low level input leakage current	I _{IL}	V _{CC} = 5.5 V V _{IN} = 0 V or V _{CC}	1, 2, 3	All	-1.0	1.0	μA
I/O pin leakage current	I _O	V _{CC} = 5.5 V V _O = 0 V or V _{CC}	1, 2, 3	All	-10.0	10.0	μA
Bus hold high leakage current	I _{BHH}	V _O = 3.0 V, V _{CC} = 4.5 V and 5.5 V Ports A, B, C	1, 2	All	-50	-400	μA
			3		-50	-450	
Bus hold low leakage current	I _{BHL}	V _O = 1.0 V, V _{CC} = 4.5 V and 5.5 V Port A only	1, 2	All	50	400	μA
			3		50	450	
Darlington drive current	I _{DAR}	Ports A, B, C <u>2/ 3/</u>	1, 2, 3	All	-2.5	<u>4/</u>	mA
Power supply current	I _{CCSB}	V _{CC} = 5.5 V, V _{IN} = V _{CC} or GND Outputs open	1, 2, 3	All		10	μA
Input capacitance	C _{IN}	Frequency = 1 MHz, see 4.3.1c All measurements are referenced to device ground. T _C = +25°C, V _{IN} = V _{CC} or GND	4	All		10	pF
I/O capacitance	C _{I/O}	Frequency = 1 MHz, see 4.3.1c All measurements are referenced to device ground. T _C = +25°C, V _{IN} = V _{CC} or GND	4	All		20	pF
Functional tests		See 4.3.1d <u>5/</u>	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = +4.5 V unless otherwise specified	Reference number 6/	Group A subgroups	Device type	Limits		Unit
						Min	Max	
Address stable before READ	t _{AR}	f = 1 MHz	1	9, 10, 11	All	0		ns
Address stable after READ	t _{RA}		2	9, 10, 11	All	0		ns
READ pulse width	t _{RR}		3	9, 10, 11	01	250		ns
					02	150		
Data valid from READ	t _{RD}		4 (1)	9, 10, 11	01		200	ns
					02		120	
Time between READS, WRITES, and READ and WRITE	t _{RV}		6	9, 10, 11	All	300		ns
Address stable before WRITE	t _{AW}		7	9, 10, 11	All	0		ns
Address stable after WRITE	t _{WA}		8	9, 10, 11	All	20		ns
WRITE pulse width	t _{WW}		10	9, 10, 11	All	100		ns
Data valid to WRITE high	t _{DW}		12	9, 10, 11	All	100		ns
Data valid after WRITE high	t _{WD}		13	9, 10, 11	All	30		ns
WR = 1 to output	t _{WB}		15 (1)	9, 10, 11	All		350	ns
Peripheral data before RD	t _{IR}		16	9, 10, 11	All	0		ns
Peripheral data after RD	t _{HR}		17	9, 10, 11	All	0		ns
ACK pulse width	t _{AK}		18	9, 10, 11	All	200		ns
STB pulse width	t _{ST}		19	9, 10, 11	All	100		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C V _{CC} = +4.5 V unless otherwise specified	Reference number 6/	Group A subgroups	Device type	Limits		Unit
						Min	Max	
Peripheral data before STB high	t _{PS}	f = 1 MHz	20	9, 10, 11	All	20		ns
Peripheral data after STB high	t _{PH}		21	9, 10, 11	All	50		ns
ACK = 0 to output	t _{AD}		22 (1)	9, 10, 11	All		175	ns
\overline{WR} = 1 to OBF = 0	t _{WOB}		24 (1)	9, 10, 11	All		150	ns
ACK = 0 to OBF = 1	t _{AOB}		25 (1)	9, 10, 11	All		150	ns
STB = 0 to IBF = 1	t _{SIB}		26 (1)	9, 10, 11	All		150	ns
\overline{RD} = 1 to IBF = 0	t _{RIB}		27 (1)	9, 10, 11	All		150	ns
\overline{RD} = 0 to INTR = 0	t _{RIT}		28 (1)	9, 10, 11	All		200	ns
STB = 1 to INTR = 1	t _{SIT}		29 (1)	9, 10, 11	All		150	ns
ACK = 1 to INTR = 1	t _{AIT}		30 (1)	9, 10, 11	All		150	ns
\overline{WR} = 0 to INTR = 0	t _{WIT}		31 (1)	9, 10, 11	All		200	ns
Reset pulse width 7/	t _{RES}		32	9, 10, 11	All	500		ns

1/ Interchanging of force and sense condition is permitted.

2/ Refers to test condition 3 as specified on figure 3.

3/ Guaranteed by V_{OH} test.

4/ No internal current limiting on port outputs. A resistor must be added externally to limit the current.

5/ Tested as follows: f = 1 MHz, V_{IN} = 2.6 V, V_{IL} = 0.4 V, C_L = 50 pF, V_{OH} ≥ 1.5 V, and V_{OL} ≤ 1.5 V.

6/ The reference number refers to the parameter being measured on figure 3 and the number identified in () refers to the test condition on figure 3.

7/ Period of initial reset pulse after power-on must be at least 50 μs. Subsequent reset pulses may be 500 ns minimum.

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Device types: 01 and 02			
Case outline Q			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA3	21	PB3
2	PA2	22	PB4
3	PA1	23	PB5
4	PA0	24	PB6
5	\overline{RD}	25	PB7
6	\overline{CS}	26	V _{CC}
7	GND	27	D7
8	A1	28	D6
9	A0	29	D5
10	PC7	30	D4
11	PC6	31	D3
12	PC5	32	D2
13	PC4	33	D1
14	PC0	34	D0
15	PC1	35	RESET
16	PC2	36	\overline{WR}
17	PC3	37	PA7
18	PB0	38	PA6
19	PB1	39	PA5
20	PB2	40	PA4

FIGURE 1. Terminal connections.

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Device types: 01 and 02			
Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA3	23	PB4
2	PA2	24	PB5
3	PA1	25	PB6
4	PA0	26	PB7
5	\overline{RD}	27	V _{cc}
6	\overline{CS}	28	NC
7	V _{ss}	29	NC
8	NC	30	D7
9	A1	31	D6
10	A0	32	D5
11	PC7	33	D4
12	PC6	34	D3
13	PC5	35	D2
14	PC4	36	D1
15	PC0	37	D0
16	PC1	38	RESET
17	PC2	39	NC
18	PC3	40	\overline{WR}
19	PB0	41	PA7
20	PB1	42	PA6
21	PB2	43	PA5
22	PB3	44	PA4

NC = No connection

FIGURE 1. Terminal connections - Continued.

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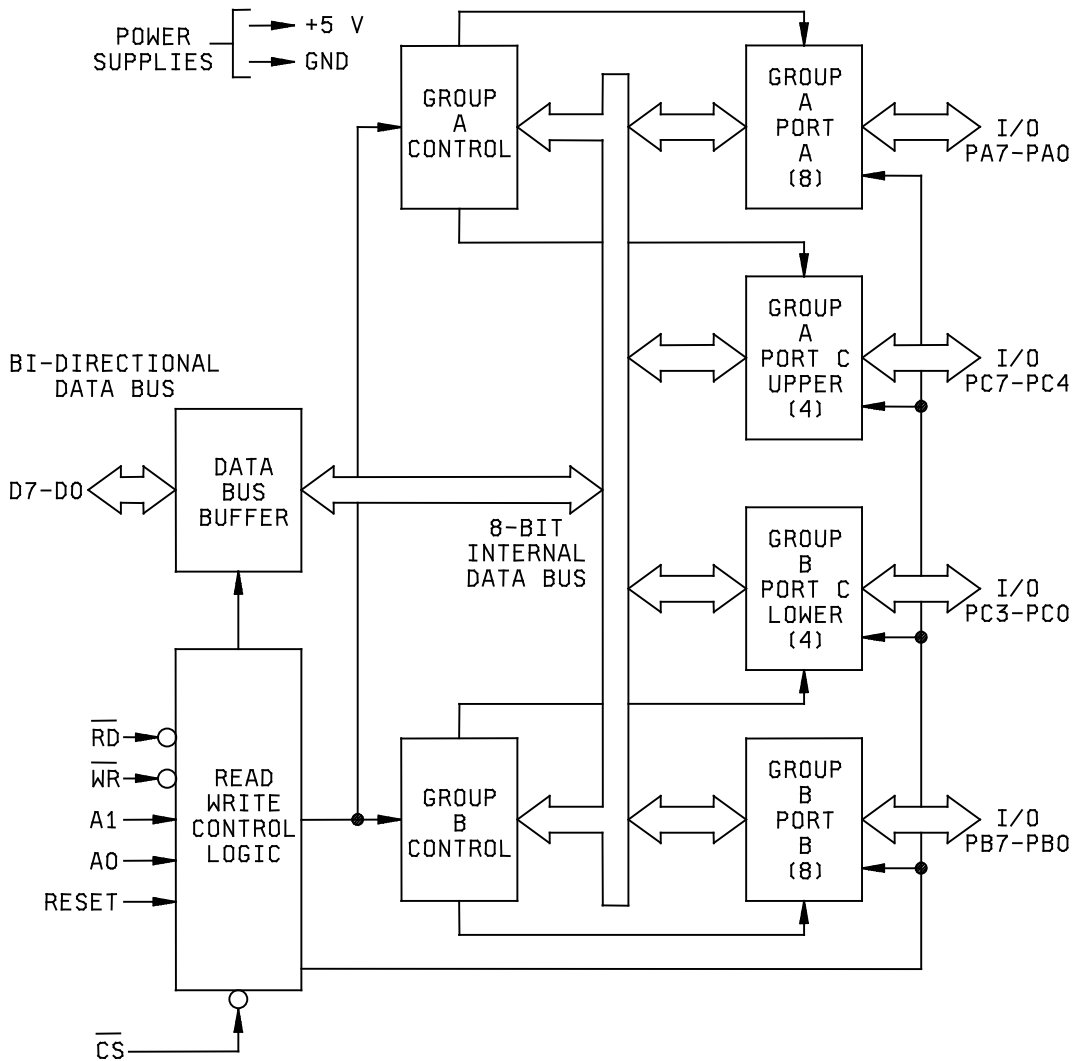


FIGURE 2. Block diagram.

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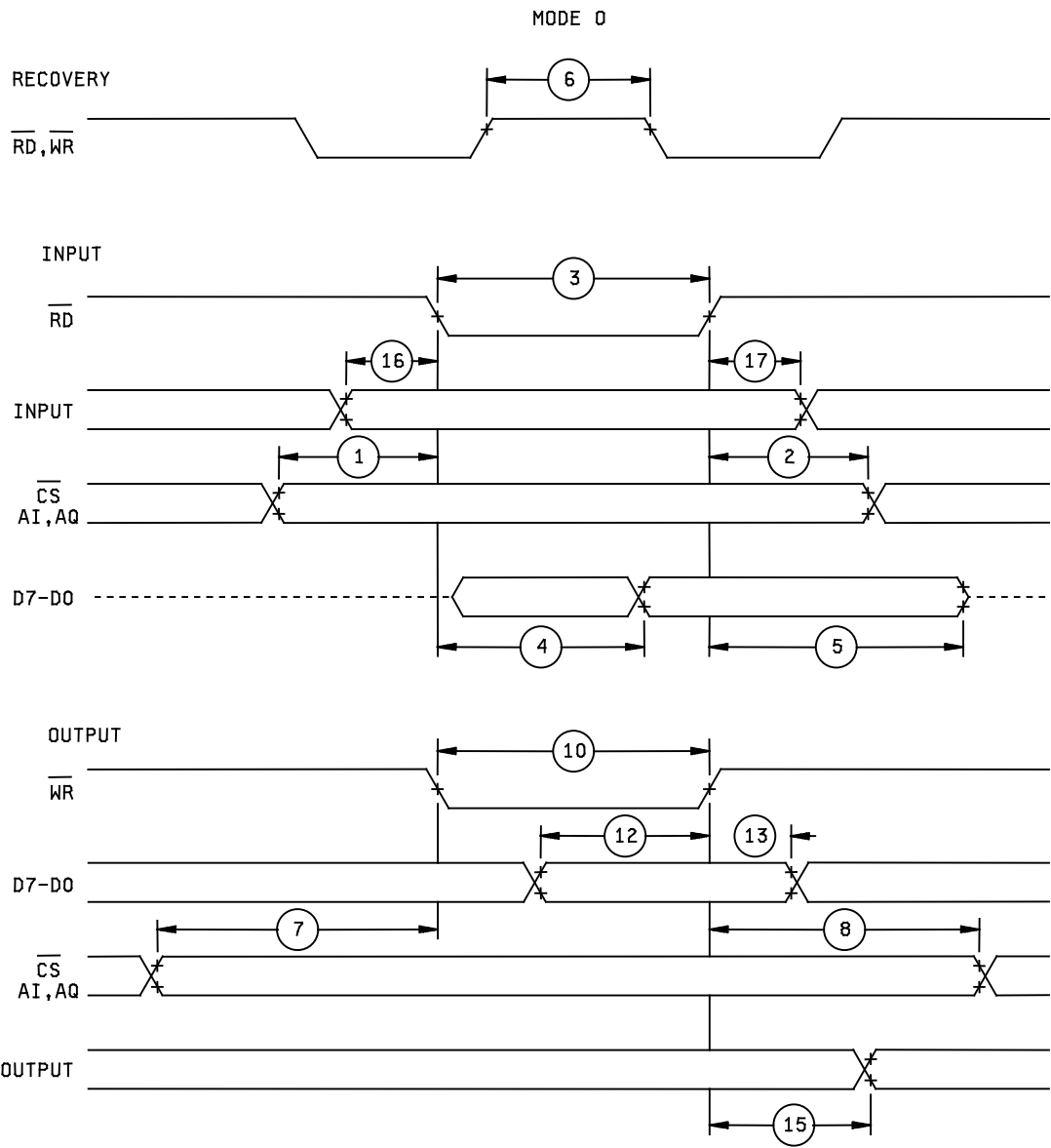


FIGURE 3. Switching waveforms and test circuits.

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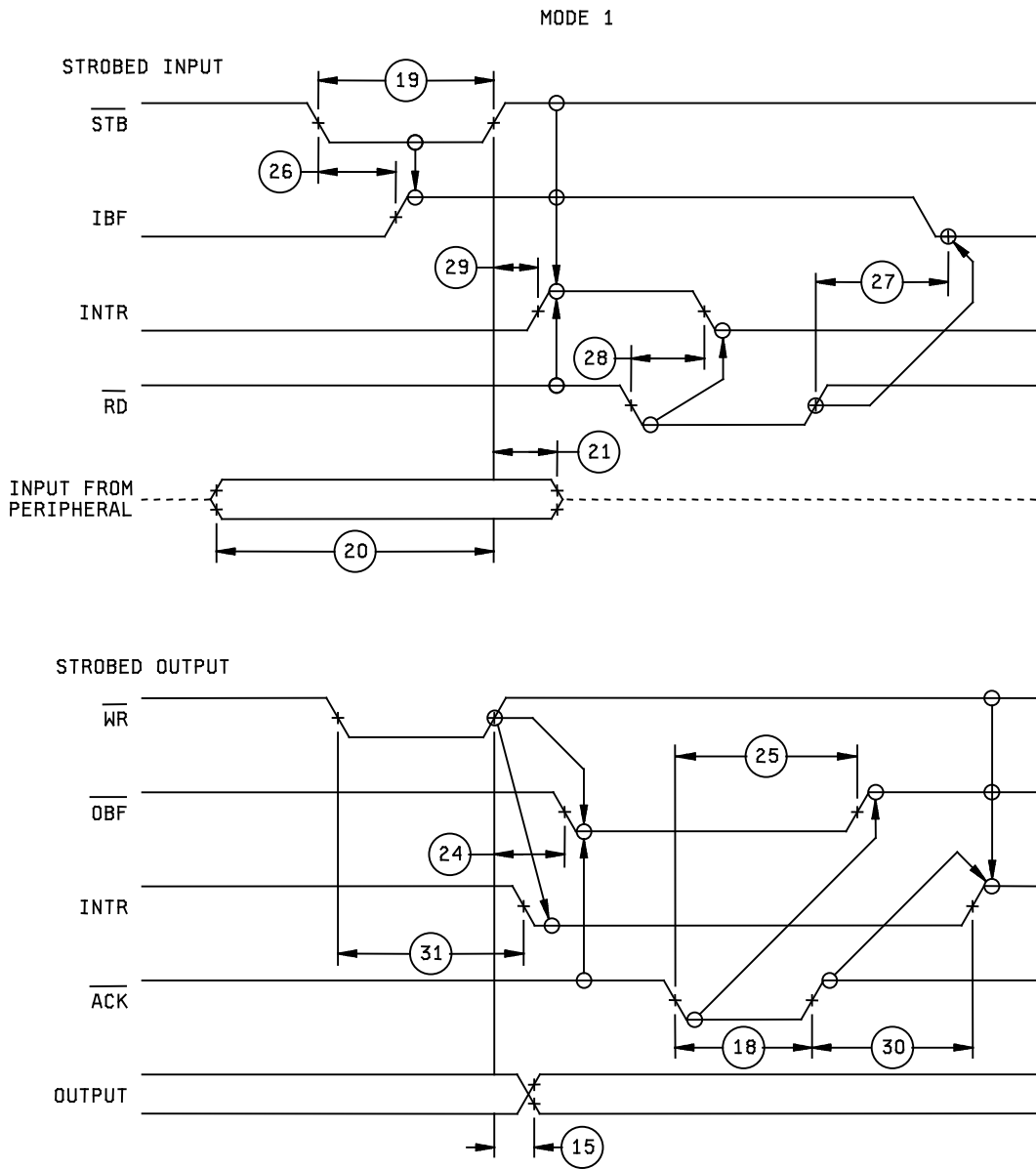


FIGURE 3. Switching waveforms and test circuits - Continued.

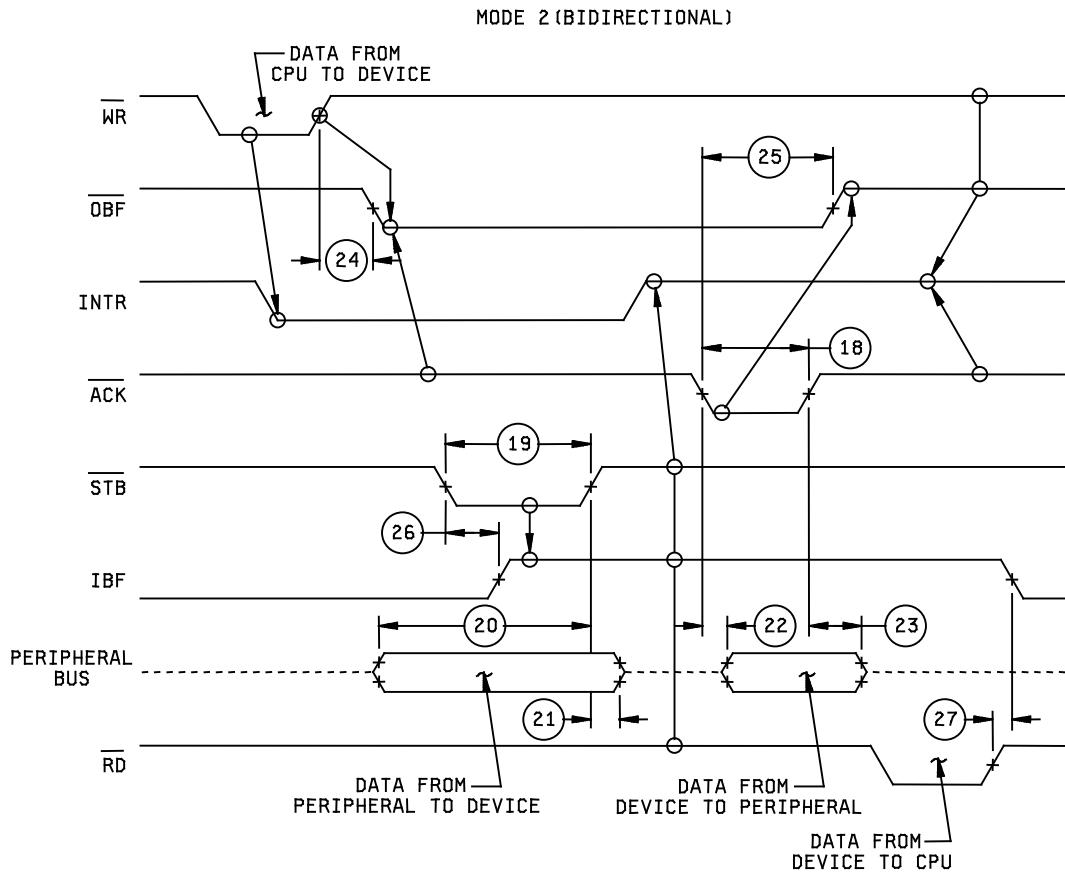
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MODE: ANY SEQUENCE WHERE \overline{WR} OCCURS BEFORE \overline{ACK} AND \overline{STB} OCCURS BEFORE \overline{RD} IS PERMISSIBLE
 (INTR=IBF•MASK• \overline{STB} • \overline{RD} + \overline{OBF} •MASK• \overline{ACK} • \overline{WR})

FIGURE 3. Switching waveforms and test circuits - Continued.

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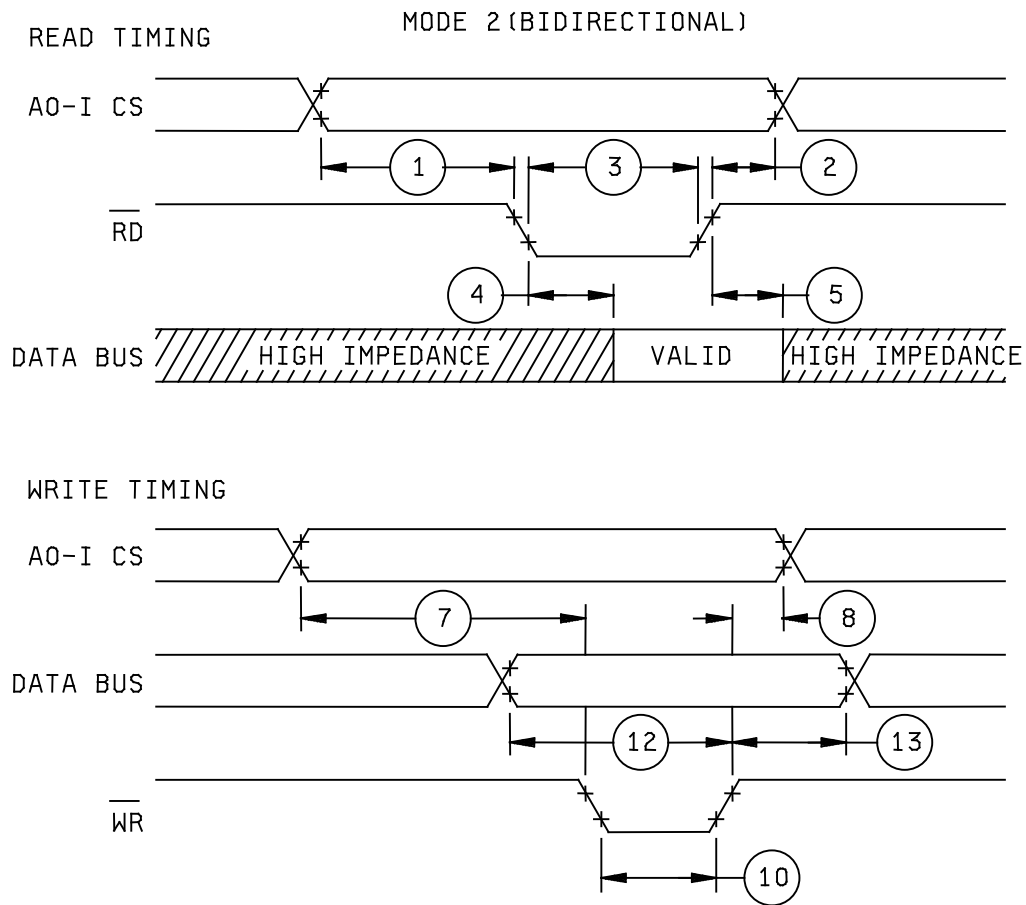


FIGURE 3. Switching waveforms and test circuits - Continued.

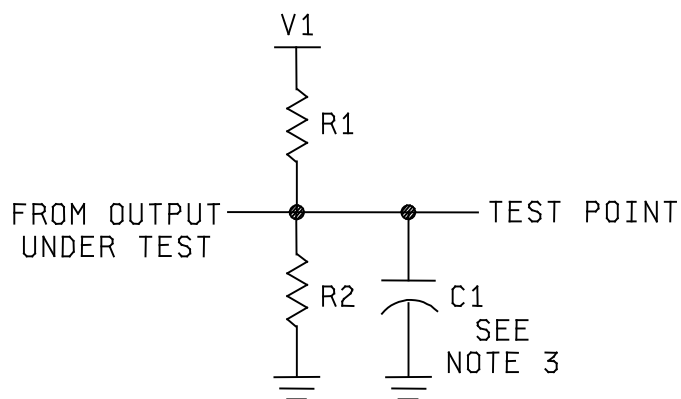
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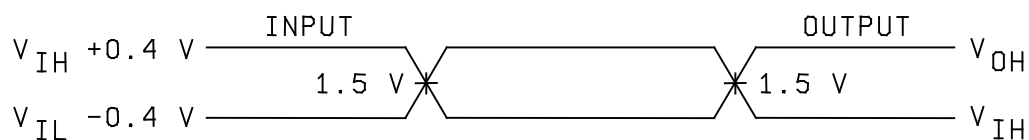
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Test Condition	V1	R1	R2	C1 (Minimum)
1	1.7 V	523 Ω	Open	150 pF
2	V _{cc}	2 k Ω	1.7 k Ω	50 pF
3	1.5 V	750 Ω	Open	Open



Notes:

1. All input signals must switch between $V_{IL} - 0.4 \text{ V}$ and $V_{IH} + 0.4 \text{ V}$.
2. Input rise and fall times are driven at 1 ns/V.
3. Includes stray and jig capacitance.

FIGURE 3. Switching waveforms and test circuits - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (+125°C only), 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the programming set and functionality of the device.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 693-9032.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 693-0178.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Pin descriptions.

<u>Name</u>	<u>Description</u>
D7 – D0	<u>Data bus.</u> This 3-state bi-directional 8-bit buffer is used to interface the device to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data buffer.
RESET	<u>Reset.</u> A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the device will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400 μA .
$\overline{\text{CS}}$	<u>Chip select.</u> A "low" on this input pin enables the communication between the device and the CPU.
$\overline{\text{RD}}$	<u>Read.</u> A "low" on this input pin enables the device to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the device.

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6.7 Pin descriptions - Continued.

<u>Name</u>	<u>Description</u>
\overline{WR}	<u>Write</u> . A "low" on this input pin enables the CPU to write data or control words into the device.
A0, A1	<u>Port select 0 and port select 1</u> . These input signals, in conjunction with the \overline{RD} and \overline{WR} inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A0 and A1).
PA7 – PA0	<u>Port A</u> . One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on port A.
PB7 – PB0	<u>Port B</u> . One 8-bit input/output latch/buffer and one 8-bit data input buffer.
PC7 – PC0	<u>Port C</u> . One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
V _{cc}	<u>Power</u> . The +5 volts power supply pin. A 0.1 μ F capacitor between V _{cc} and GND is recommended for decoupling.
GND	<u>Ground</u> . 0 volts.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 26-01-21

Approved sources of supply for SMD 84066 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
8406601QA	<u>3/</u>	MD82C55A-5/883
8406601XA	<u>3/</u>	MD82C55A-5/883
8406602QA	34371	MD82C55A/883
8406602XA	34371	MD82C55A/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

34371

Vendor name and address

Renesas Electronics America, Inc.
1650 Robert J. Conlan Blvd NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.