REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							
REV STATUS			REV																	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

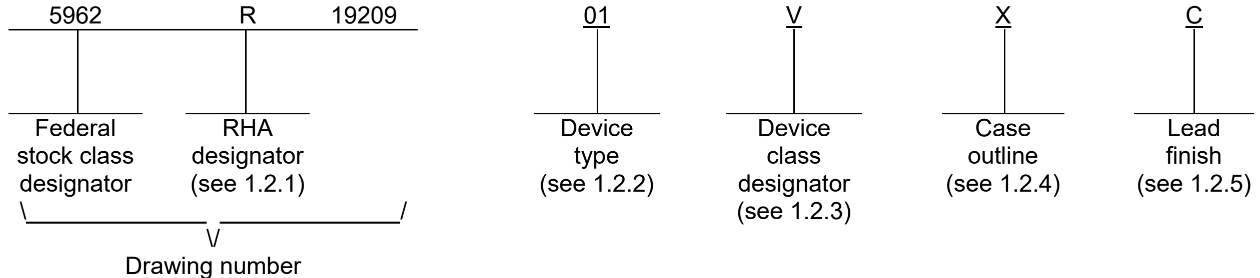
PMIC N/A	PREPARED BY RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY RAJESH PITHADIA	
	APPROVED BY JAMES R. ESCHMEYER	MICROCIRCUIT, LINEAR, DUAL OUTPUT POL, SYNCHRONOUS BUCK, AND LOW DROP OUT REGULATORS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 20-04-22	
AMSC N/A	REVISION LEVEL	SIZE A | CAGE CODE **67268** | **5962-19209**
		SHEET 1 OF 27

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70005SEH	Radiation hardened dual output point-of-load, integrated synchronous Buck, and low dropout regulators
02	ISL73005SEH	Radiation hardened dual output point-of load, integrated synchronous Buck, and low dropout regulators

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F28	28	Dual flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

B_VCC	B_GND - 0.3 V to B_GND + 6.5 V
B_VCC	B_GND - 0.3 V to B_GND + 6.0 V 2/ 3/
B_VINx	B_PGND - 0.3 V to B_PGND + 6.5 V
B_VINx	B_PGND - 0.3 V to B_PGND + 6.0 V 2/ 3/
L_VCC	L_GND - 0.3 V to L_GND + 6.5 V
L_VCC	L_GND - 0.3 V to L_GND + 6.0 V 2/ 3/
L_VINx	L_GND - 0.3 V to L_GND + 6.5 V
L_VINx	L_GND - 0.3 V to L_GND + 6.0 V 2/ 3/
B_LXx	B_PGND - 0.3 V; limit 6.5 V from B_VIN to B_VINx + 0.3 V; limit 6.5 V to B_PGND
B_LXx	B_PGND - 0.3 V; limit 6.0 V from B_VIN to B_VINx + 0.3 V; limit 6.0 V to B_PGND 2/ 3/
B_LXx (< 50 ns pulse width up to 1 MHz switching frequency)	B_PGND – 2.0 V; limit 6.5 V from B_VIN to B_VINx + 1.5 V; limit 6.5 V to B_PGND
L_OUT	L_PGND - 0.3 V to L_VIN + 0.3; limit 6.5 V
L_OUT	L_PGND - 0.3 V to L_VIN + 0.3 V; limit 6.0 V 2/ 3/
L_PG, B_PG, B_RT, B_SYNC, B_COMP, B_FB	B_GND - 0.3 V to B_VCC + 0.3 V
B_EN, L_EN, L_EA-, L_EA+, VREF, TEST	L_GND - 0.3 V to L_VCC + 0.3 V
B_SS	B_GND - 0.3 V to B_VCC + 0.3V; limit B_GND + 3.5 V
L_SS	L_GND - 0.3 V to L_VCC + 0.3V; limit L_GND + 3.5 V
B_GND to L_PGND, B_GND to L_GND, L_GND to L_PGND	- 0.3V to + 0.3 V
B_GND to B_PGND, L_GND to B_PGND, L_PGND to B_PGND	- 0.6V to + 0.6V
Power dissipation (P_D):	
T_A = +25°C	6.41 W
T_A = +125°C	1.28 W
T_C = +25°C	104 W
T_C = +125°C	20.8 W
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-ambient (θ_{JA})	19.5°C/W 4/
Thermal resistance, junction-to-case (θ_{JC})	1.2°C/W 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For operation in a heavy ion environment at LET = 86.4 MeV/(mg/cm^2) at T_C = 125°C and with buck converter sourcing 0 amps and 3.5 amps load current.

3/ For operation in a heavy ion environment at LET = 86.4 MeV/(mg/cm^2) at T_C = 125°C with low drop out (LDO) sourcing and sinking 1.2 amps load current.

4/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.

5/ For θ_{JC}, the “case temperature” location is the center of the package underside.

1.4 Recommended operating conditions.

B_VIN1, B_VIN2, B_VCC, L_VCC .... 3.3 V ±10 % to 5 V ±10%
L_VIN .... 1.0 V to L_VCC
Ambient operating temperature range (T_A) .... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s):
Device type 01 .... 100 krads(Si) 7/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s):
Device types 01 and 02 .... 50 krads(Si) 7/ 8/
Single event phenomena (SEP):
No SEL observed at B_VCC = L_VCC = B_VINx ≤ 6.0 V effective
linear energy transfer (LET) .... ≤ 86 MeV/(mg/cm^2) 9/
No SEB observed at B_VCC = L_VCC = B_VINx ≤ 6.0 V effective
linear energy transfer (LET) .... ≤ 86 MeV/(mg/cm^2) 9/
No Buck SEFI observed at effective linear energy transfer (LET) .... ≤ 43 MeV/(mg/cm^2) 9/
No Buck SET observed resulting in > 89 mV deviation at nominal 1.8 V and at effective
linear energy transfer (LET) .... ≤ 86 MeV/(mg/cm^2) 9/
No LDO SET observed resulting in > 39 mV deviation at nominal 0.9 V and at effective
linear energy transfer (LET) .... ≤ 86 MeV/(mg/cm^2) 9/

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7/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krad(Si), and condition D to a maximum total ionizing dose (TID) of 75 krad(Si).

8/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device type 02 is wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krad(Si) level.

9/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP/SEE characteristics but, are not production tested unless specified by the customer through the purchase order or contract. For more information on destructive SEE (SEB/SEFI) test results, customers are requested to contact manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Buck regulator electrical specifications							
Power supply section.							
Operating supply current - switching	IOP	B_EN = 2 V, 100 kHz switching, B_LXx floating	1,2,3	01, 02		15	mA
Shutdown supply current	ISDN	B_EN = GND	1,2,3	01, 02		3	mA
Enable pin characteristics.							
B_EN rising threshold	BEnRT		1,2,3	01, 02	1.6	2.0	V
B_EN falling threshold	BEnFT		1,2,3	01, 02	1.4	1.9	V
B_EN input hysteresis	BEnHys		1,2,3	01, 02	100		mV
B_EN pull down resistance	BEnPdrH	B_EN = 5.5 V	1,2,3	01, 02	80	160	kΩ
B_EN pull down resistance	BEnPdrL	B_EN = 1.4 V	1,2,3	01, 02	60	130	kΩ
Pulse width modulator (PWM) control logic.							
Switching frequency	tSF	B_RT resistor = 544 kΩ	9,10,11	01, 02	85	115	kHz
		B_RT resistor = 44 kΩ			875	1175	
B_LXx minimum on time	tON	B_VIN = B_VCC = 5.5 V, B_COMP = 180 mV, 1 kΩ from B_LXx to 2.75 V	9,10,11	01, 02	100	240	ns
B_LXx minimum on time	tON1	B_VIN = B_VCC = 3 V , B_COMP = 180 mV, 1 kΩ from B_LXx to 1.5 V	9,10,11	01, 02	115	325	ns
B_LXx minimum off time	tOFF	B_COMP = 180 mV, 1 kΩ to from B_LXx [B_VIN / 2]	9,10,11	01, 02	50	165	ns
External synchronization range	ESync	B_RT clock set to 90% of B_SYNC clock, 50% duty cycle clock input	9,10,11	01, 02	100	1000	kHz
B_SYNC input voltage 3/	SYNVIH		1,2,3	01, 02	2		V
	SYNVIL					0.8	
B_SYNC input leakage current	SYNLKG		1,2,3	01, 02	-1	1	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Soft start.							
Soft-start source current	ISSRC	SS = GND	1,2,3	01, 02	17	30	μA
Soft-start discharge on-resistance	SSRES		1,2,3	01, 02		6	Ω
Reference voltage.							
Reference voltage tolerance	V_{REF} + V_{IO}	V_{REF} + Error amplifier V_{IO}	1,2,3	01, 02	0.594	0.606	V
Error amplifier.							
Maximum output voltage	EAO	B_VCC = 5.5 V	1,2,3	01, 02	3.5		V
B_FB input leakage current	EAFB	VB_FB = 0.6 V, B_VINx = 5.5 V	1,2,3	01, 02		250	nA
Power MOSFET.							
Packaged upper device RDS(ON)	PURON	B_VINx = 3.0V, single B_LXx output	4,5,6	01, 02	80	245	mΩ
		B_VINx = 5.5V, single B_LXx output			65	210	
Packaged lower device RDS(ON)	PLRON	B_VINx = 3.0V, Single B_LXx output	4,5,6	01, 02	40	160	mΩ
		B_VINx = 5.5V, single B_LXx output			35	150	
Packaged power MOSFET matching, B_LX1 RDS(ON) to B_LX2 RDS(ON)	PONM		5	01, 02		15	%
B_LXx output leakage	LXLKG	B_EN = B_LXx = xGND, single B_LXx output	1,2,3	01, 02		3	μA
		B_EN = xGND, B_LXx = 5.5 V, single B_LXx output				15	
Deadtime 4/	tDEAD		9,10,11	01, 02	0	50	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power-good signal.							
B_PG overvoltage error threshold	BPGOVTH	B_FB as a % of VREF	1,2,3	01, 02	107	115	%
B_PG overvoltage error hysteresis	BPGOVHY	B_FB as a % of VREF	1,2,3	01, 02	1.5	5	%
B_PG undervoltage error threshold	BPGUVTH	B_FB as a % of VREF	1,2,3	01, 02	85	93	%
B_PG undervoltage error hysteresis	BPGUVHY	B_FB as a % of VREF	1,2,3	01, 02	1.5	5	%
B_PG drive	BPGDRV	B_VIN = 3 V, B_PG = 0.4V, B_EN = xGND	1,2,3	01, 02	7.2		mA
B_PG leakage	BPGLKG	B_VINx = B_PG = 5.5 V	1,2,3	01, 02		1	μA
Protection features.							
Undervoltage protection.							
Undervoltage trip threshold	UVTRIP	B_FB as a % of VREF, test mode	1,2,3	01, 02	71	79	%
Undervoltage recovery threshold	UVREC	B_FB as a % of VREF, test mode	1,2,3	01, 02	86	94	%
Overcurrent protection.							
Overcurrent Limit	OCL		1,2,3	01, 02	4	6.4	A
LDO electrical specifications. 5/							
DC characteristics.							
L_VIN voltage range	VINR	Minimum guaranteed by VDO3	1,2,3	01, 02	0.775	VCC	V
L_OUT voltage range	VOUTR	L_EA+ = 0.600 V, Minimum guaranteed by VDO3, Maximum guaranteed by VDO4	1,2,3	01, 02	0.6	L_VCC - 1.5	V
VREF voltage	VREF		1,2,3	01, 02	0.591	0.609	V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ 5/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LDO electrical specifications. 5/							
Power on reset (POR)							
B_VCC internal UVLO rising threshold	PORRT		1,2,3	01, 02	2.60	2.95	V
B_VCC internal UVLO falling threshold	PORFT		1,2,3	01, 02	2.45	2.80	V
B_VCC internal UVLO hysteresis	PORHys		1,2,3	01, 02	75	420	mV
DC characteristics.							
DC output voltage accuracy	VOUTx 7/	L_VCC = 5.5 V, L_VIN = [4.15V, 5.5 V], R1/R2 = 4.5, L_EA+ = 0.600 V, ILOAD = [10 mA, 1 A], VOUTx where x = 1, 3, 5, 7	1,2,3	01, 02	3.225	3.336	V
		L_VCC = 5.5 V, L_VIN = [4.15V, 5.5 V], R1/R2 = 4.5, L_EA+ = 0.600 V, ILOAD = [-10 mA, -1 A], VOUTx where x = 2, 4, 6, 8			3.285	3.397	
		L_VCC = [3.35 V, 5.5 V], L_VIN = [2 V, 3 V, 5.5V], R1/R2 = 1.5, L_EA+ = 0.600 V, ILOAD = {10 mA, 1 A}, VOUTx where x = 9, 11, 13, 15, 17, 19, 21, 23			1.463	1.519	
		L_VCC = [3.35 V, 5.5 V], L_VIN = [2 V, 3 V, 5.5V], R1/R2 = 1.5, L_EA+ = 0.600 V, ILOAD = [-10 mA, -1 A], VOUTx where x = 10, 12, 14, 16, 18, 20, 22, 24			1.490	1.546	
		L_VCC = [3.1 V, 5.5 V], L_VIN = [1.75 V, 3 V, 5.5 V], L_EA- = L_OUT, L_EA+ = 1.250 V, ILOAD = [10 mA, 1 A], VOUTx where x = 25, 27, 29, 31, 33, 35, 37, 39			1.235	1.258	
		L_VCC = [3.1 V, 5.5 V], L_VIN = [1.75 V, 3 V, 5.5 V], L_EA- = L_OUT, L_EA+ = 1.250 V, ILOAD = [-10 mA, -1 A], VOUTx where x = 26, 28, 30, 32, 34, 36, 38, 40			1.246	1.269	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ 5/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LDO electrical specifications – continued.							
DC characteristics – continued.							
DC output voltage accuracy – continued.	VOUTx 7/	L_VCC = [3 V, 5.5 V], L_VIN = [1.1 V, 3 V, 5.5 V], L_EA- = L_OUT,L_EA+ = 0.600 V, ILOAD = [10 mA, 1 A], VOUTx where x = 41, 43, 45, 47, 49, 51, 53, 55	1,2,3	01, 02	0.585	0.608	V
		L_VCC = [3 V, 5.5 V], L_VIN = [1.1 V, 3 V, 5.5 V], L_EA- = L_OUT,L_EA+ = 0.600 V, ILOAD = [-10 mA, -1 A], VOUTx where x = 42, 44, 46, 48, 50, 52, 54, 56			0.596	0.619	
Regulation Dead-Band	RegDB	L_VOUT difference between the two current cases: IOUT = {sourcing 10 mA, sinking 10 mA} for L_VCC = 5.5 V, L_VIN = 5.5 V, L_EA+ = 0.600 V, L_OUT = L_EA-	1,2,3	01, 02	5	15	mV
L_EA+, L_EA- input bias current	EALKG	L_EA+ =L_EA- = 0.6 V, L_VIN = 5.5 V	1,2,3	01, 02		1	μA
L_VCC pin current	IQ	L_OUT = 1.5 V; ILOAD = 1 A; L_VIN = 1.65 V; 3.0 V <L_VCC < 5.5 V	1,2,3	01, 02		10	mA
L_VCC pin current in Shutdown	ISHDN	L_EN = B_EN = 0 V, L_VCC = 5.5 V	1,2,3	01, 02		1000	μA
Dropout voltage, 6/ VDO	VDO1	IOUT = 1 A, L_OUT = 0.6 V; L_VIN = L_OUT + VDO; 3.0 V < L_VCC < 5.5 V	3	01, 02		115	mV
Dropout voltage, 6/ VDO	VDO2	IOUT = 1 A, L_OUT = 0.6 V; L_VIN = L_OUT + VDO; 3.0 V < L_VCC < 5.5 V	1	01, 02		145	mV
Dropout voltage, 6/ VDO	VDO3	IOUT = 1 A, L_OUT = 0.6 V; L_VIN = L_OUT + VDO; 3.0 V < L_VCC < 5.5 V	2	01, 02		175	mV
Dropout voltage, 8/ VDO	VDO4	IOUT = 1 A, L_OUT = 3.3 V; L_VIN = 3.8 V; L_VCC = L_OUT + VDO	1,2,3	01, 02		1.5	mV

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ 5/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LDO electrical specifications – continued.							
Protection features							
Positive overcurrent limit	LOCLP		1,2,3	01, 02	1.25	2	A
Negative overcurrent limit	LOCLN		1,2,3	01, 02	-2	-1.25	A
Thermal shutdown 4/ temperature	TSD	Junction temperature	4,5,6	01, 02	153	195	°C
AC ripple rejection and noise characteristics.							
1 kHz VIN supply ripple rejection	PSRR1	VP-P = 300 mV, f = 1 kHz, ILOAD = 1 A; L_VCC = 5 V, L_VIN = 3.15 V, L_OUT = 1.5 V	4,5,6	01, 02	60		dB
1kHz L_VCC supply ripple rejection	PSRR2	VP-P = 300 mV, f = 1 kHz, ILOAD = 1 A; L_VCC = 5 V, L_VIN = 3 V, L_OUT = 1.5 V	4,5,6	01, 02	50		dB
Enable pin characteristics							
L_EN rising threshold	LEnRT		1,2,3	01, 02	1.6	2.0	V
L_EN falling threshold	LEnFT		1,2,3	01, 02	1.4	1.9	V
L_EN input hysteresis	LEnHys		1,2,3	01, 02	100		mV
L_EN pull down resistance	LEnPdrH	L_EN = 5.5 V	1,2,3	01, 02	80	160	kΩ
L_EN pull down resistance	LEnPdrL	L_EN = 1.4 V	1,2,3	01, 02	60	130	kΩ
PGOOD characteristics							
L_PG overvoltage error threshold	LPGOVTH	L_EA- as a % of L_EA+, L_EA+ = 600 mV	1,2,3	01, 02	107	115	%
L_PG overvoltage error hysteresis	LPGOVHY	L_EA- as a % of L_EA+, L_EA+ = 600 mV	1,2,3	01, 02	1.5	5	%
L_PG undervoltage error threshold	LPGUVTH	L_EA- as a % of L_EA+, L_EA+ = 600 mV	1,2,3	01, 02	85	93	%
L_PG undervoltage error hysteresis	LPGUVHY	L_EA- as a % of L_EA+, L_EA+ = 600 mV	1,2,3	01, 02	1.5	5	%
L_PG drive	LPGDRV	L_VCC = 3 V, L_PG = 0.4 V, L_EN = L_GND	1,2,3	01, 02	7.2		mA
L_PG leakage current	LPGLKG	L_VIN = L_PG = 5.5 V	1,2,3	01, 02		1	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ Unless otherwise noted, B_VINx = B_VCC = 3 V - 5.5 V; B_GND = B_PGNDx = 0 V;
B_SYNC = B_LXx = open circuit; B_PG is pulled up to B_VCC with a 3 kΩ resistor; VREF is bypassed to L_GND with a 22 nF capacitor; B_SS is bypassed to B_GNDx with a 100 nF capacitor; IOUT = 0 A.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 02 is only tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein). Device type 02 is wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krad(Si) level.

Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Limits guaranteed during functional testing.

4/ Limits established by characterization or design and are not production tested.

5/ Unless otherwise noted, all parameters are guaranteed over the following specified conditions:
COUT = 150 μF tantalum, IL = 0 A.
Applications must follow thermal guidelines of the package to determine worst case junction temperature.

6/ Dropout is defined by the difference in L_VIN and L_OUT when the regulator produces a 2% drop in L_OUT from its nominal value.

7/ LDO VOUTx is set by connecting R1 between L_EA- and L_OUT and connecting R2 between L_EA- and L_GND. The regulated output is then nominally set to L_EA+ times (1 + R1/R2).

8/ Dropout is defined by the difference in L_VCC and L_OUT when the regulator produces a 2% drop in L_OUT from its nominal value.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP/SEE	Temperature (T_C)	B_VCC, B_VINx, L_VCC	Effective linear energy transfer (LET)
01, 02	No SEL	+125°C	≤ 6.0	≤ 86 MeV/(mg/cm^2)
	No SEB	+125°C	≤ 6.0	≤ 86 MeV/(mg/cm^2)
	No Buck SET > 89 mV	+25°C		≤ 86 MeV/(mg/cm^2)
	No LDO SET > 39 mV	+25°C		≤ 86 MeV/(mg/cm^2)
	No SEFI	+25°C	≥ 3.0	≤ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ All test conditions using a minimum of 4 units unless otherwise noted.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	B_SS	15	L_EA-
2	B_FB	16	L_GND
3	B_COMP	17	L_PGND
4	B_RT	18	L_OUT
5	B_VCC	19	L_VIN
6	B_SYNC	20	TEST
7	B_GND1	21	B_VIN1
8	B_GND2	22	B_LX1
9	VREF	23	B_PGND1
10	B_EN	24	B_PGND2
11	L_EN	25	B_LX2
12	L_VCC	26	B_VIN2
13	L_SS	27	B_PG
14	L_EA+	28	L_PG
Package lid. Internal connection to B_GND1 and B_GND2			

FIGURE 1. Terminal connections.

Terminal symbol	Description
B_SS	Soft-start input to the buck regulator. When B_EN is driven above 2 V, a 24 μA pull-up current charges a ceramic capacitor connected from B_SS to B_GNDx to set the soft-start ramp time.
B_FB	Inverting input to the buck error amplifier. A type III compensation network should be connected between this pin and the B_COMP pin.
B_COMP	Output of the buck regulator's error amplifier. An external compensation network should be connected between this pin and the B_FB pin.
B_RT	Oscillator frequency select input. Connect a resistor from this pin to B_GNDx to program the switching frequency from 100 kHz to 1 MHz.
B_VCC	Supply input to the internal buck control circuitry. Bypass B_VCC to B_GNDx using a ceramic capacitor as close as possible to the integrated circuit (IC). Use a low pass filter between the B_VINx and this pin to minimize noise on B_VCC.
B_SYNC	Clock frequency synchronization input to the buck regulator. These devices use it's internal oscillator until soft start is completed (B_PG is set to high-impedance), and then synchronizes to B_SYNC if a clock is present. The rising edge of B_SYNC starts a new PWM cycle (begins minimum off-time).
B_GND1	Buck signal ground pin and package lid connection.
B_GND2	Buck signal ground pin and package lid connection.
VREF	Output of the 600 mV reference voltage. Bypass this pin to L_GND with a 100 nF ceramic capacitor located as close as possible to the IC. This pin may be used as the LDO reference voltage by connecting VREF to L_EA+. Additional loading is not recommended.
B_EN	Enable input to the buck regulator. Driving this pin above 2 V enables the buck.
L_EN	Enable input to the LDO. Driving this pin above 2 V enables the LDO.
L_VCC	Bias supply pin to the LDO signal level circuitry and common functions circuitry.
L_SS	Soft-start input to the LDO. Connect a ceramic capacitor from L_SS to L_GND to set the soft-start output ramp time. When the LDO is enabled, a 24 μA pull-up current charges the ceramic capacitor.
L_EA+	Non-inverting input to the LDO error amplifier. Connect this pin to the VREF pin for typical applications or a resistor divider from the buck output for DDR memory power applications.
L_EA-	Inverting input to the LDO error amplifier.
L_GND	LDO signal ground pin.
L_PGND	LDO power-stage ground pin.
L_OUT	LDO output pin.
L_VIN	Input supply pin for the LDO power-stage metal oxide semiconductor field effect transistor (MOSFET). Must not exceed L_VCC.

FIGURE 1. Terminal connections - continued.

Terminal symbol	Description
TEST	Automatic test equipment (ATE) test signal, must be connected to L_GND.
B_VIN1	Power supply for the buck power-stage MOSFETs. Bypass B_VINx pins directly to B_PGNDx with ceramic capacitors located as close as possible to the IC. Must be the same voltage as B_VCC.
B_LX1	Buck regulator switch node connection. Output of the internal buck power MOSFETs, connect to the power inductor.
B_PGND1	Buck power-stage ground pin.
B_PGND2	Buck power-stage ground pin.
B_LX2	Buck regulator switch node connection. Output of the internal buck power MOSFETs, connect to the power inductor.
B_VIN2	Power supply for the buck power-stage MOSFETs. Bypass B_VINx pins directly to B_PGNDx with ceramic capacitors located as close as possible to the IC. Must be the same voltage as B_VCC.
B_PG	Power-good output for the buck regulator. This output is open-drain logic, connect a 10 kΩ to 100 kΩ pull-up resistor to B_VCC. May be wired-OR with L_PG to have a single power good signal. Bypass B_PG to B_GND with a 10 nF ceramic capacitor to mitigate SEE.
L_PG	Power-good output for the LDO. This output is open-drain logic, connect a 10 kΩ to 100kΩ pull-up resistor to L_VCC. May be wired-OR with B_PG to have a single power good signal. Bypass L_PG to L_GND with a 10nF ceramic capacitor to mitigate SEE.

FIGURE 1. Terminal connections - continued.

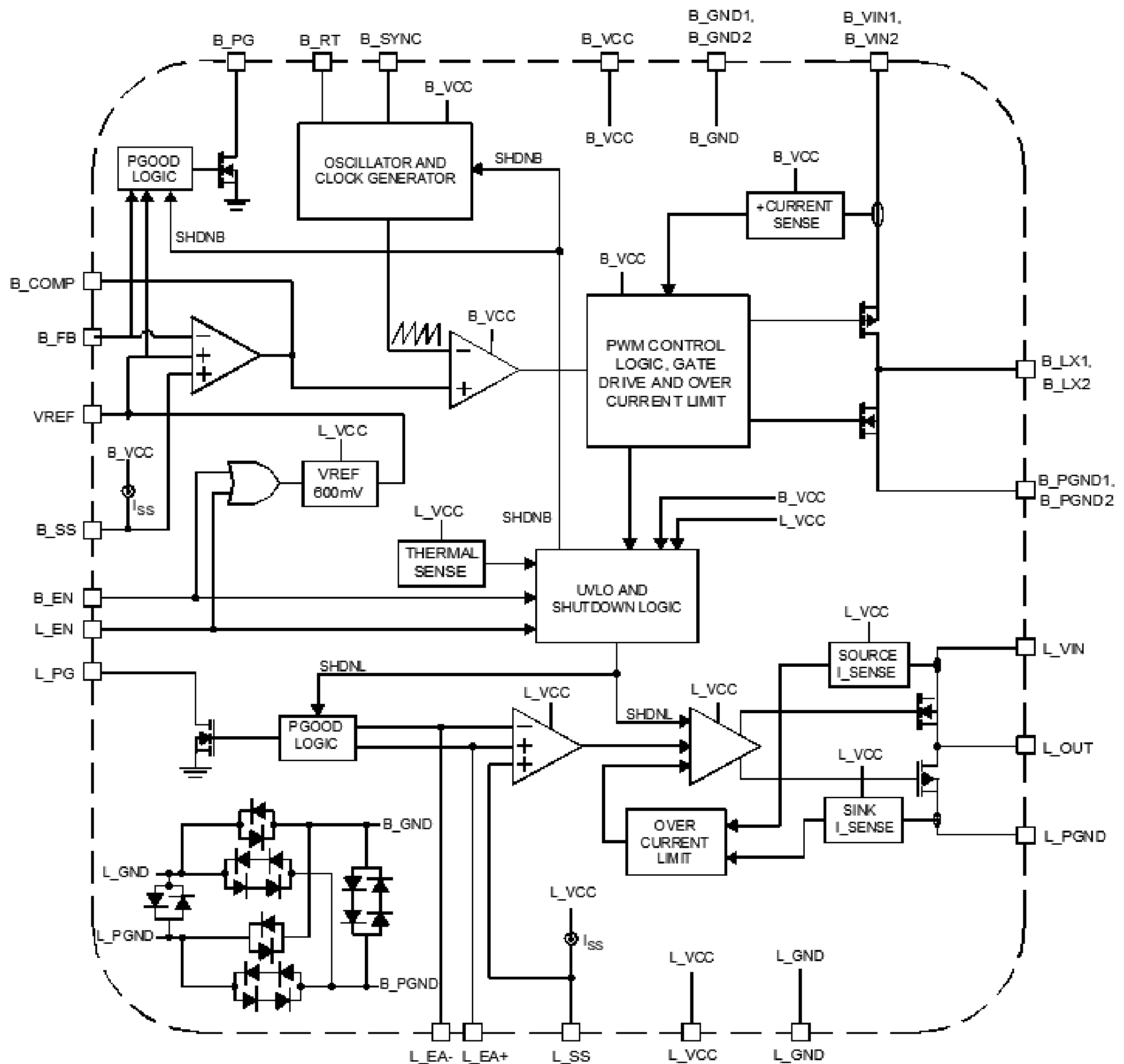


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-19209
		REVISION LEVEL	SHEET 16

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3, 1/ 2/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and Δ.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Device types	Delta limits		Limit
				Min	Max	
Reference voltage tolerance	VREF+VIO	V_{REF} + Error amplifier V_{IO}	01, 02	-2.0	+2.0	mV
Switching frequency	TSF	B_RT resistor = 544 kΩ	01, 02	-15.0	+15.0	kHz
Switching frequency	TSF	B_RT resistor = 44 kΩ	01, 02	-100.0	+100.0	kHz
Shutdown supply current	ISDN	B_EN = GND	01, 02	-0.45	+0.45	mA
Operating supply current - switching	IOP	B_EN = 2 V, 100 kHz switching, B_LXx floating	01, 02	-2.25	+2.25	mA
Regulation dead-band	RegDB	L_VOUT difference between the two current cases: IOUT = {sourcing 10 mA, sinking 10 mA} for L_VCC = 5.5 V, L_VIN = 5.5 V, R1 = 0 Ω, L_EA+ = 0.600 V	01, 02	-3.0	+3.0	mV
L_VCC pin current in Shutdown	ISHDW	L_EN = B_EN = 0 V, L_VCC = 5.5 V	01, 02	-150.0	+150.0	μA
L_VCC pin current	IQ	L_OUT = 1.5 V; ILOAD = 1 A; L_VIN = 1.65 V; 3.0 V < L_VCC < 5.5 V	01, 02	-1.5	+1.5	mA

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, conditions A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be 25°C for SET. The test temperature shall be 125°C for SEB and SEL.

f. Bias conditions shall be as specified in table IB.

g. For SEL, SEB, SET, and SEFI test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Occurrence of latchup (SEL).

d. Occurrence of burnouts (SEB).

e. Number of transients (SET).

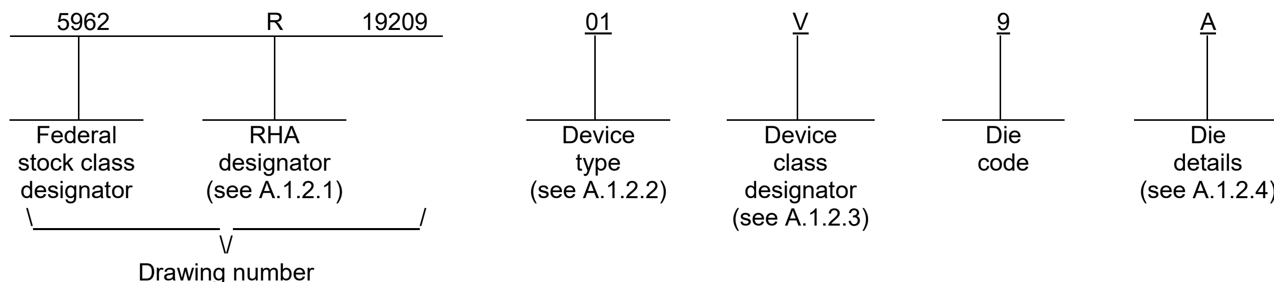
f. Number of single event functional interrupts (SEFI).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-19209

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70005SEH	Radiation hardened dual output point-of-load, integrated synchronous Buck, and low dropout regulators
02	ISL73005SEH	Radiation hardened dual output point-of load, integrated synchronous Buck, and low dropout regulators

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

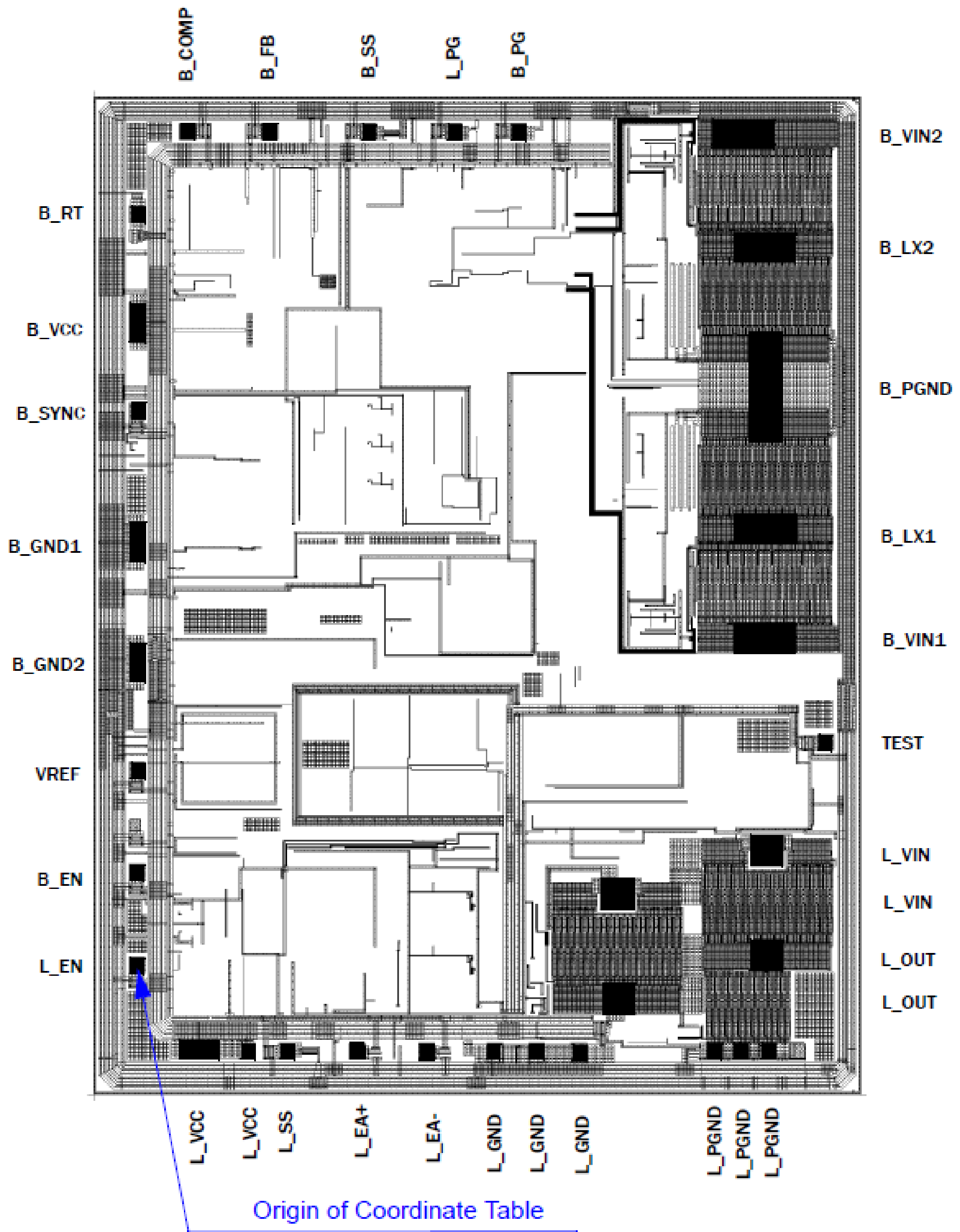


FIGURE A-1. Die bonding pad locations and electrical functions.

TABLE III. Layout X-Y coordinates (centroid of bond pad).

Pad name	Pad number	X coordinate (μm)	Y coordinate (μm)	Pad X dim. (μm)	Pad Y dim. (μm)	Bond wire dia. (0.001")
L_EN	1	0	0	125	125	1.5
B_EN	2	0	776	125	125	1.5
VREF	3	0	1,628	125	125	1.5
B_GND2	4	0	2,528	125	320	1.5
B_GND1	5	0	3,530	125	320	1.5
B_SYNC	6	0	4,621	125	125	1.5
B_VCC	7	0	5,364	125	320	1.5
B_RT	8	0	6,268	125	125	1.5
B_COMP	9	425	6,956	125	125	1.5
B_FB	10	1,106	6,956	125	125	1.5
B_SS	11	1,931	6,956	125	125	1.5
L_PG	12	2,644	6,956	125	125	1.5
B_PG	13	3,188	6,956	125	125	1.5
B_VIN2	14	5,057	6,935	508	254	3
B_LX2	15	5,238	6,016	508	254	3
B_PGND	16	5,242	4,831	254	894	3
B_LX1	17	5,238	3,646	508	254	3
B_VIN1	18	5,238	2,727	508	254	3
TEST	19	5,744	1,862	125	125	1.5
L_VIN	20	5,254	957	260	254	3
L_VIN	21	4,001	593	260	254	3
L_OUT	22	5,257	81	254	254	3
L_OUT	23	4,024	-283	254	254	3
L_PGND	24	4,820	-720	125	125	3
L_PGND	25	5,040	-720	125	125	3
L_PGND	26	5,260	-720	125	125	3
L_GND	27	2,986	-720	125	125	1.5
L_GND	28	3,334	-720	125	125	1.5
L_GND	29	3,685	-720	125	125	1.5
L_EA-	30	2,417	-720	125	125	1.5
L_EA+	31	1,838	-720	125	125	1.5
L_SS	32	1,249	-720	125	125	1.5
L_VCC	33	519	-720	320	125	1.5
L_VCC	34	921	-720	125	125	1.5

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 6504 μm x 8436 μm (256 mils x 332 mils)
Die thickness: 304.8 μm ± 25 μm (12.0 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5%/0.5%)
Thickness: 2.7 μm ± 0.4 μm
Backside metallization: None

Glassivation.
Type: Silicon dioxide and silicon nitride
Thickness: 0.3 μm ±0.03 μm and 1.2 μm ±0.12 μm

Substrate: 0.6 μM BiCMOS junction isolated

Assembly related information.
Substrate potential: Internal connection to B_GND1 and B_GND2
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-04-22

Approved sources of supply for SMD 5962-19209 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1920901VXC	34371	ISL70005SEHVF
5962R1920901V9A	34371	ISL70005SEHVX
5962L1920902VXC	34371	ISL73005SEHVF
5962L1920902V9A	34371	ISL73005SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.