REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
JAMES R. ESCHMEYER

DRAWING APPROVAL DATE
20-04-16

REVISION LEVEL

MICROCIRCUIT, LINEAR, 10 AMP PMOS LOAD SWITCH, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-19208**

SHEET 1 OF 28

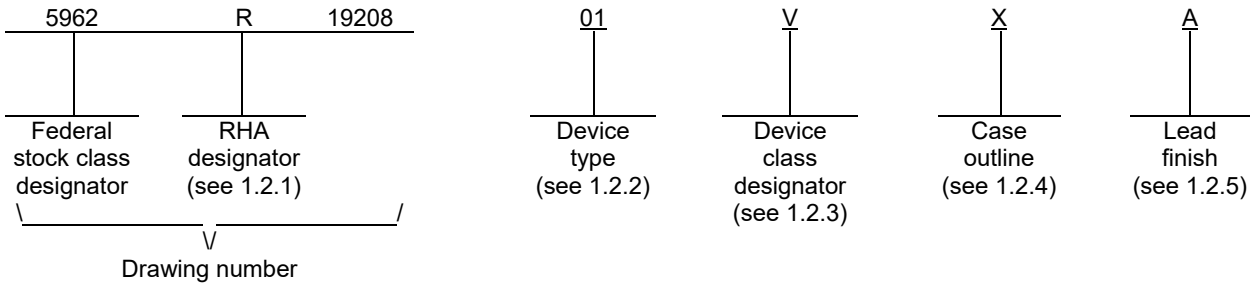
DSCC FORM 2233
APR 97

5962-E043-20

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70061SEH	Radiation hardened, 10 amp positive metal oxide semiconductor (PMOS) load switch
02	ISL73061SEH	Radiation hardened, 10 amp PMOS load switch

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F14	14	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

SWI, SWO, ON, DON to GND ..... -0.3 V to +6.5 V
SWI, SWO, ON, DON to GND under ion beam (SEE testing) ..... -0.3 V to +6.5 V 2/
I_{SW} continuous switch current ..... 13.78 A
I_{SWP} pulsed switch current, pulse < 1 ms, duty cycle 1%) ..... 20 A
Storage temperature range ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-ambient (θ_{JA}) (case outline X with epoxy) ..... 29°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA}) (case outline X with solder) ..... 25°C/W 3/
Thermal resistance, junction-to-case (θ_{JC}) ..... 3.5°C/W 4/

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A) ..... -55°C to +125°C
SWI input voltage range ..... 3.0 V to 5.5 V
ON, DON ..... 0 V to 5.5 V
I_{SW} ..... 0 A to 10 A

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s):
Device type 01 ..... 100 krads(Si) 5/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s):
Device types 01 and 02 ..... 50 krads(Si) 5/ 6/

Single event phenomena (SEP):
No SEL occurs at SWI = 6.7 V and at effective linear energy (LET) (see 4.4.4.3) ..... ≤ 86 MeV/(mg/cm^2) 7/
No SEB at SWI, SWO, ON, DON = 6.7 V occurs at surface LET (see 4.4.4.3) ..... ≤ 86 MeV/(mg/cm^2) 7/
Single event transients (SET) observed at an effective LET (see 4.4.4.3) ..... ≤ 86 MeV/(mg/cm^2) 7/
(Flux = 5 x 10^3 ions/(cm^2•s), Fluence = 1 x 10^7 ions/cm^2 and cross section = 20 µm^2 with ±30 mV)
The SET testing yielded two forms of SET, large and small events. The large events have been demonstrated to be double ion events. The small events exhibited roughly the same statistics and flux dependence as the large events and are likely double ion events. See the manufacturer's SEE test report for additional details.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Tested in a heavy ion environment at LET = 86 MeV/(mg/cm^2) at +125°C (T_C) for SEB. Refer to manufacturer single event effects test report for more information.
3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (two buried 1 ounce copper planes) using "direct attach" features with package base mounted to printed circuit board (PCB) thermal land (with thermal vias below) with either a) epoxy (10 mils thick with a "k" of 1W / m-K) or b) solder (~2 mils thick). See manufacturer for more information.
4/ For θ_{JC}, the case temperature location is the center of the package underside.
5/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krads(Si), and condition D to a maximum total ionizing dose (TID) of 75 krads(Si).
6/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krads(Si). Device type 02 is wafer acceptance tested to 75 krads(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krads(Si) level.
7/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but, are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results (see table IB), customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Control timing waveform. The control timing waveform shall be as specified on figure 4.

3.2.5 SWO timing waveform. The timing SWO waveform shall be as specified on figure 5.

3.2.6 Timing test circuit. The timing test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply currents								
Quiescent switch current	I_{SWQ}	V_{SWI} = 5.5 V, I_{SWO} = 0 A, V_{DON} = VSWI, V_{ON} = V_{SWI}, measure I_{SWI}		1,2,3	01, 02		39	µA
			M, D, P, L, R	1 2/			39	
		V_{SWI} = 3.6 V, I_{SWO} = 0 A, V_{DON} = VSWI, V_{ON} = V_{SWI}, measure I_{SWI}		1,2,3			29	
			M, D, P, L, R	1 2/			29	
SWI off switch current	$I_{SWI(OFF)}$	V_{SWI} = 5.5 V, R_L = 1 MΩ, V_{DON} = V_{SWI} and 0 V, V_{ON} = 0 V, measure I_{SWI}		1,2,3	01, 02		43	µA
			M, D, P, L, R	1 2/			43	
		V_{SWI} = 3.6 V, R_L = 1 MΩ, V_{DON} = V_{SWI} and 0 V, V_{ON} = 0 V, measure I_{SWI}		1,2,3			36	
			M, D, P, L, R	1 2/		-	36	
SWO off switch current	$I_{SWO(OFF)}$	V_{SWI} = 5.5 V, V_{ON} = V_{DON} = 0 V,		1,2,3	01, 02	-	10	µA
		V_{SWO} = 5.5 V	M, D, P, L, R	1 2/		-	10	
		V_{SWI} = 3.6 V, V_{ON} = V_{DON} = 0 V,		1,2,3		-	5	
		V_{SWO} = 3.6 V	M, D, P, L, R	1 2/		-	5	
Power switch								
Switch on resistance	r_{ON}	V_{SWI} = 5.5 V, I_{SWO} = 1 A, V_{ON} = V_{SWI}, V_{DON} = 0 V		1	01, 02	8	19	mΩ
				2		13	24	
				3		4	14	
			M, D, P, L, R	1 2/		8	19	
			Die	1 3/		-	10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power switch – continued.								
Switch on resistance	r_{ON}	V_{SWI} = 3.0 V, I_{SWO} = 1 A, $V_{ON} = V_{SWI}$, V_{DON} = 0 V		1	01, 02	11	21	mΩ
				2		15	25	
				3		6	16	
			M, D, P, L, R	1 2/		11	21	
			Die	1 3/		-	12	
Output discharge switch								
Discharge resistance	r_{DIS}	V_{SWI} = 5.5 V, V_{ON} = 0 V, $V_{DON} = V_{SWI}$, V_{SWO} = 5.5 V, measure I_{SWO} and calculate r_{DIS} = 5.5 V / I_{SWO}		1,2,3	01, 02	80	170	Ω
			M, D, P, L, R	1 2/		80	135	
		V_{SWI} = 3.0 V, V_{ON} = 0 V, $V_{DON} = V_{SWI}$, V_{SWO} = 3.0 V, measure I_{SWO} and calculate r_{DIS} = 3.0 V / I_{SWO}		1,2,3		100	235	
			M, D, P, L, R	1 2/		100	185	
ON and DON control logic								
Logic input threshold high	V_{ON_IH}	V_{SWI} = 5.5 V, $V_{DON} = V_{SWI}$, V_{ON} = 0.4 V, SWO = 1 MΩ, sweep V_{ON} from 0.4 V to 1.2 V; measure V_{ON} when rising edge of V_{SWO} = 50% of V_{SWI}.		1,2,3	01, 02		1.2	V
			M, D, P, L, R	1 2/			1.2	
Logic input threshold high	V_{DON_IH}	V_{SWI} = 5.5 V, V_{ON} = 0 V, V_{DON} = 0.4 V, V_{SWO_F} = 5.5 V through 1 Ω resistor at SWO, sweep V_{DON} from 0.4 V to 1.2 V; measure V_{DON} when $I_{SWO\_F} > 10$ µA.		1,2,3	01, 02		1.2	V
			M, D, P, L, R	1 2/			1.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ON and DON control logic – continued.							
Logic input threshold low	V_{ON_IL}	V_{SWI} = 5.5 V V_{DON} = V_{SWI}, V_{ON} = 1.2 V, SWO = 1 MΩ, sweep V_{ON} from 1.2 V to 0.4 V; measure V_{ON} when falling edge of V_{SWO} = 50% of V_{SWI}.	1,2,3	01, 02	0.4		V
		M, D, P, L, R	1 2/		0.4		
Logic input threshold low	V_{DON_IL}	V_{SWI} = 5.5 V, V_{ON} = 0 V, V_{DON} = 1.2 V, V_{SWO_F} = 3.5 V through 1 Ω resistor at SWO, sweep V_{DON} from 1.2 V to 0.4 V; measure V_{DON} when $I_{SWO\_F} < 10$ µA.	1,2,3	01, 02	0.4		V
		M, D, P, L, R	1 2/		0.4		
Logic input hysteresis	V_{ONHYS} V_{DONHYS}	V_{ONHYS} = V_{ON_IH} - V_{ON_IL}, V_{DONHYS} = V_{DON_IH} - V_{DON_IL}	1,2,3	01, 02	50	270	mV
		M, D, P, L, R	1 2/		50	220	
Pull down resistance	R_{ONPD} R_{DONPD}	R_{ONPD} = V_{ON_IH} / I_{ON} , R_{DONPD} = V_{DON_IH} / I_{DON}	1,2,3	01, 02	2	4	MΩ
		M, D, P, L, R	1 2/		2	4	
Under Voltage Lockout (UVLO)							
UVLO falling voltage	$UVLO_{Falling}$	V_{SWI} = V_{ON} = 3.0 V, V_{DON} = 0 V, R_L = 25 Ω to GND, ramp V_{SWI} / V_{ON} down simultaneously in -10 mV steps until $V_{SWO} < 0.1$ V, report this voltage as $UVLO_{Falling}$	1,2,3	01, 02	1.7	2.6	V
		M, D, P, L, R	1 2/		1.7	2.6	
UVLO rising voltage	$UVLO_{Rising}$	V_{SWI} = V_{ON} = 0.25 V, V_{DON} = 0 V, R_L = 25 Ω to GND, ramp V_{SWI} / V_{ON} up simultaneously in 10 mV steps until $V_{SWO} > 1$ V, report this voltage as $UVLO_{Rising}$	1,2,3	01, 02	1.7	2.6	V
		M, D, P, L, R	1 2/		1.7	2.6	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Under Voltage Lockout (UVLO) - continued							
UVLO hysteresis	$UVLO_{HYS}$	$UVLO_{HYS} = UVLO_{Rising} - UVLO_{Falling}$	1,2,3	01, 02	25	250	mV
		M, D, P, L, R	1 2/		25	250	
Reverse current protection 4/							
RCP enter threshold voltage	V_{RCP_ENTER}	V_{SWI} = 5.5 V, $V_{ON} = V_{SWI}$, V_{DON} = 0 V, sweep V_{SWO} from V_{SWI} to V_{SWI} +150 mV	1,2,3	01, 02		140	mV
		M, D, P, L, R	1 2/			140	
		V_{SWI} = 3.0 V, $V_{ON} = V_{SWI}$, V_{DON} = 0 V, sweep V_{SWO} from V_{SWI} to V_{SWI} +150 mV	1,2,3			70	
		M, D, P, L, R	1 2/			70	
RCP exit threshold voltage	V_{RCP_EXIT}	V_{SWI} = 5.5 V, $V_{ON} = V_{SWI}$, V_{DON} = 0 V, sweep V_{SWO} from V_{RCP_ENTER} to V_{SWI} -100 mV	1,2,3	01, 02	-80		mV
		M, D, P, L, R	1 2/		-80		
		V_{SWI} = 3.0 V, $V_{ON} = V_{SWI}$, V_{DON} = 0 V, sweep V_{SWO} from V_{RCP_ENTER} to V_{SWI} -100 mV	1,2,3		-45		
		M, D, P, L, R	1 2/		-45		
Timing (see figures 4, 5, 6) 4/							
V_{SWO} turn on time	t_{ON}	V_{SWI} = 5.5V, C_L = 1 µF, R_L = 1.8 Ω, measure from V_{ON} = V_{ON_IH} to V_{SWO} = 10% of V_{SWI}	9,10,11	01, 02		125	µs
		M, D, P, L, R	9 2/			125	
		V_{SWI} = 3.0 V, C_L = 1 µF, R_L = 1 Ω, measure from V_{ON} = V_{ON_IH} to V_{SWO} = 10% of V_{SWI}	9,10,11			160	
		M, D, P, L, R	9 2/			160	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing –continued. (see figures 4, 5, 6) 4/							
V_{SWO} rise time 10% to 90%	t_{RISE}	V_{SWI} = 5.5 V, C_L = 1 µF, R_L = 1.8 Ω, V_{SWO} = 10% to 90%	9	01, 02	500	750	µs
			10		550	780	
			11		550	890	
		M, D, P, L, R	9 2/		500	750	
		V_{SWI} = 3.0 V, C_L = 1 µF, R_L = 1 Ω, V_{SWO} = 10% to 90%	9		380	590	
			10		450	635	
			11		400	670	
		M, D, P, L, R	9 2/		380	590	
V_{SWO} turn off time	t_{OFF}	V_{SWI} = 5.5 V, C_L = 1 µF, R_L = 1.8 Ω, Measure from V_{ON} = V_{ON_IL} to V_{SWO} = 90% of V_{SWI}	9,10,11	01, 02	-	5	µs
		M, D, P, L, R	9 2/		-	5	
		V_{SWI} = 3.0 V, C_L = 1 µF, R_L = 1 Ω, Measure from V_{ON} = V_{ON_IL} to V_{SWO} = 90% of V_{SWI}	9,10,11		-	6	
		M, D, P, L, R	9 2/		-	6	
V_{SWO} fall time 90% to 10%	t_{FALL}	V_{SWI} = 5.5 V, C_L = 1 µF, V_{SWO} = 90% to 10%, R_L = 1.8 Ω	9,10,11	01, 02	4	12	µs
		M, D, P, L, R	9 2/		4	9.5	
		V_{SWI} = 3.0 V, C_L = 1 µF, V_{SWO} = 90% to 10%, R_L = 1 Ω	9,10,11		3	9	
		M, D, P, L, R	9 2/		3	6.5	
RCP response time	t_{REV}	V_{SWI} = 5.5 V, V_{ON} = 5.5 V, V_{DON} = 0 V; start with V_{SWO} = V_{SWI} = 5.5 V, sweep V_{SWO} from 5.5 V to 5.6 V with 5000V/s slew rate; measure time from V_{RCP_ENTER} to when I_{RCP} has returned to 0 A. 5/	9,10,11	01, 02		8	µs
		M, D, P, L, R	9 2/		-	12	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
RCP response time	t_{REV}	V_{SWI} = 3.0 V, V_{ON} = 3.0 V, V_{DON} = 0 V; start with V_{SWO} = V_{SWI} = 3.0 V, sweep V_{SWO} from 3.0 V to 3.1 V with 5000 V/s slew rate; measure time from V_{RCP_ENTER} to when I_{RCP} has returned to 0 A. 5/		9,10,11	01, 02		10	µs
			M, D, P, L, R	9 2/		-	14	

1/ Unless otherwise specified: V_{SWI} = V_{ON} = 5.5 V, V_{DON} = 0 V, R_L = 1.8 Ω.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and levels M, D, P, and L of irradiation for condition D. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krads(Si) and condition D to TID level 75 krads(Si) (see 1.5 herein).
RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However device type 02 is only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krads(Si). Device type 02 is wafer acceptance tested to 75 krads(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krads(Si) level.

Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ RON resistance of the die only, excludes packaging and bond wire resistance.

4/ RCP and timing parameters are not tested during wafer die probe testing. Die limit specifications for these parameters are not available. Packaging and bond wire parasitic impedance do affect the specification performance of these parameters.

5/ I_{RCP} is the current referenced from SWO to SWI when $V_{SWO} > V_{SWI}$ but V_{RCP_ENTER} has not been met.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET)
01, 02	No SEL at SWI = 6.7 V observed	125°C	Effective LET= 86 MeV/(mg/cm^2) 3/ 4/
	No SEB at SWI = 6.7 V observed	125°C	Surface LET= 86 MeV/(mg/cm^2) 3/ 4/
	SET observed	25°C	LET= 86 MeV/(mg/cm^2) 3/ 4/

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Heavy ion testing performed at the Texas A&M University (TAMU) K500 super-conducting cyclotron facility. The irradiations were done with Gold ion beam to fluence level 1 x 10^7 ions/cm^2 at a flux of about 1 x 10^4 ions/(cm^2•s). No single event latch-up (SEL) or single-event burn out (SEB) was observed when irradiated with Gold ions at fluence 1 x 10^7 ions/cm^2 at with bias voltage 6.7 V corresponding to an surface LET of 86 MeV/(mg/cm^2). SET observed at flux= 5 x 10^3 ions/(cm^2•s), Fluence = 1 x 10^7 ions/cm^2 and cross section = 20 µm^2 with magnitude ±30 mV. The SET testing yielded two forms of SET, large and small events. The large events have been demonstrated to be double ion events. The small events exhibited roughly the same statistics and flux dependence as the large events and are likely double ion events. See the manufacturer's SEE test report for additional details.

4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

Case X

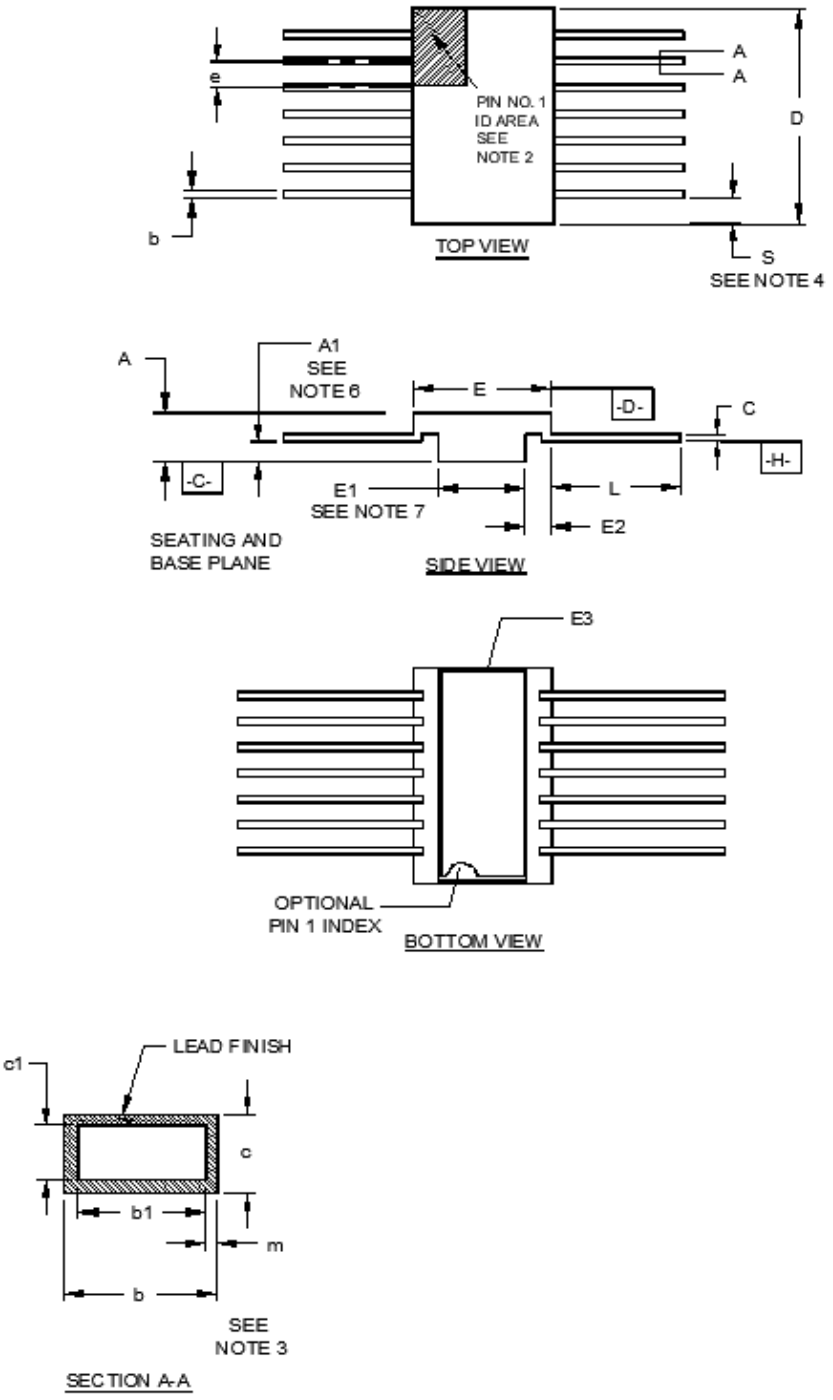


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.085	.115	2.16	2.92
A1	.026	.045	0.66	1.14
b	.015	.022	0.38	0.56
b1	.015	.019	0.38	0.48
c	.004	.009	0.10	0.23
c1	.004	.006	0.10	0.15
D	.376	.390	9.55	9.91
E	.248	.260	6.30	6.60
E1	.167	.183	4.24	4.65
E2	.030	---	0.76	---
E3	.005 REF		0.127 REF	
e	.050 BSC		1.27 BSC	
m	---	.0015	---	0.040
s	.005	---	0.13	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measure at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by .0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is a solderable metal surface.

FIGURE 1. Case outline.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	SWI	8	GND
2	SWI	9	DON
3	SWI	10	SWO
4	SWI	11	SWO
5	SWI	12	SWO
6	SWI	13	SWO
7	ON	14	SWO
Package lid. Tied internally to terminal 8 (GND).			
Bottom metal thermal pad. Tied internally to terminal 8 (GND).			

Terminal symbol	Description
SWI	Switch input.
ON	Logic control input. ON = High: Switch ON, ON = Low: Switch OFF.
GND	Ground connection. Lid and External Bottom Metal are internally tied to pin 8.
DON	Logic input to enable or disable discharge FET circuit function. DON = High: Discharge FET circuit active, DON = Low: Discharge FET circuit inactive.
SWO	Switch output.
Package lid. Internally tied to the ground pin of the package, pin 8.	
Bottom metal thermal pad. Bottom metal thermal pad for heat sink purposes. Internally tied to the ground pin of the package, pin 8.	

FIGURE 2. Terminal connections.

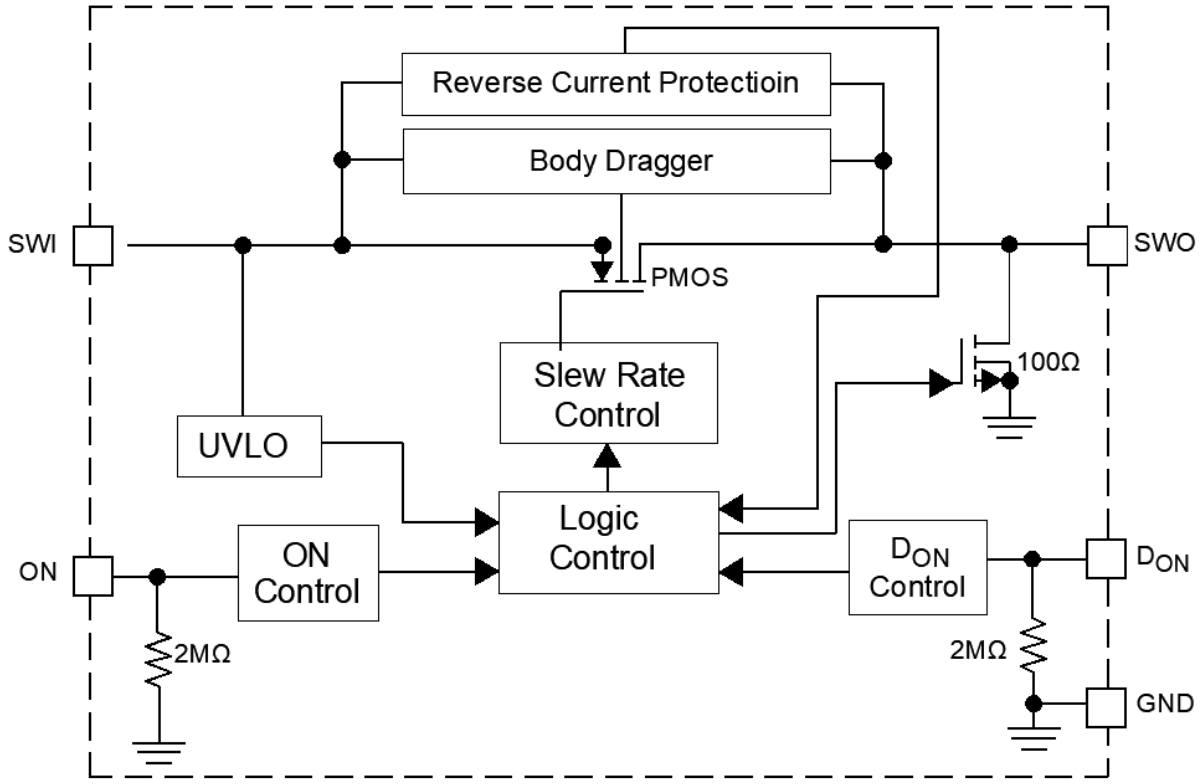


FIGURE 3. Block diagram.

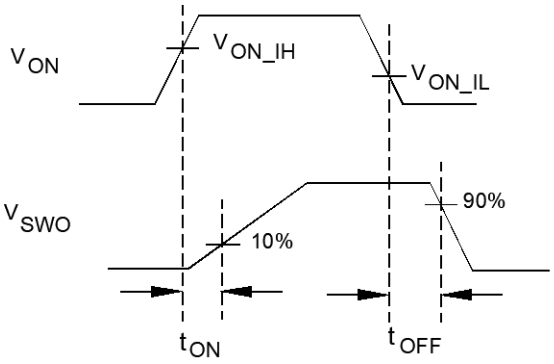


FIGURE 4. Control timing waveforms.

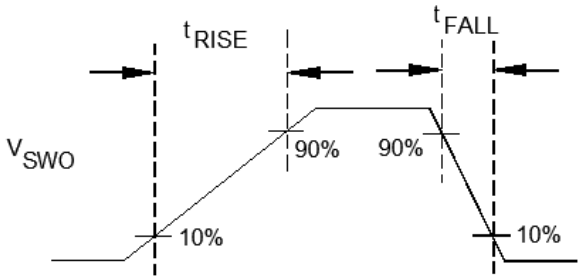


FIGURE 5. SWO timing waveforms.

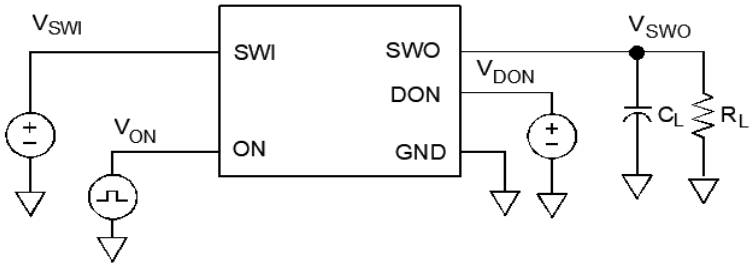


FIGURE 6. Timing test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1 ,2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and delta.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
Switch on resistance Ron_3p0	R_{ON}	V_{SWI} = 3.0 V, I_{SW} = 1 A, $V_{ON} = V_{SWI}$, V_{DON} = 0 V	±2.0 mΩ
Switch on resistance Ron_5p5	R_{ON}	V_{SWI} = 5.5 V, I_{SW} = 1 A, $V_{ON} = V_{SWI}$, V_{DON} = 0 V	±2.0 mΩ
Quiescent switch current ISWQ_5p5	I_{SWQ}	V_{SWI} = 5.5 V, I_{SWO} = 0 A, $V_{ON} = V_{DON} = V_{SWI}$	±3.8 μA
SWI off switch current ISWIOff1_5p5	$I_{SWI(OFF)}$	V_{SWI} = 5.5 V, R_L = 1 MΩ, V_{ON} = 0 V, $V_{DON} = V_{SWI}$ and 0 V	±4.2 μA
SWO off switch current ISWOOff3_5p5	$I_{SWO(OFF)}$	V_{SWI} = 5.5 V, $V_{ON} = V_{DON}$ = 0 V, V_{SWO} = 5.5 V	±1.0 μA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

c. Single event burn-out (SEB) observances.

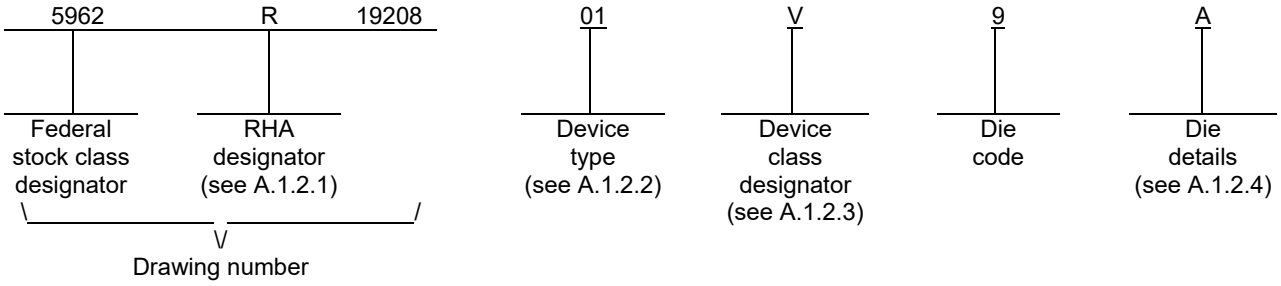
d. Single event transient (SET) observances.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-19208

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70061SEH	Radiation hardened 10A PMOS protection switch
02	ISL73061SEH	Radiation hardened 10A PMOS protection switch

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.7 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

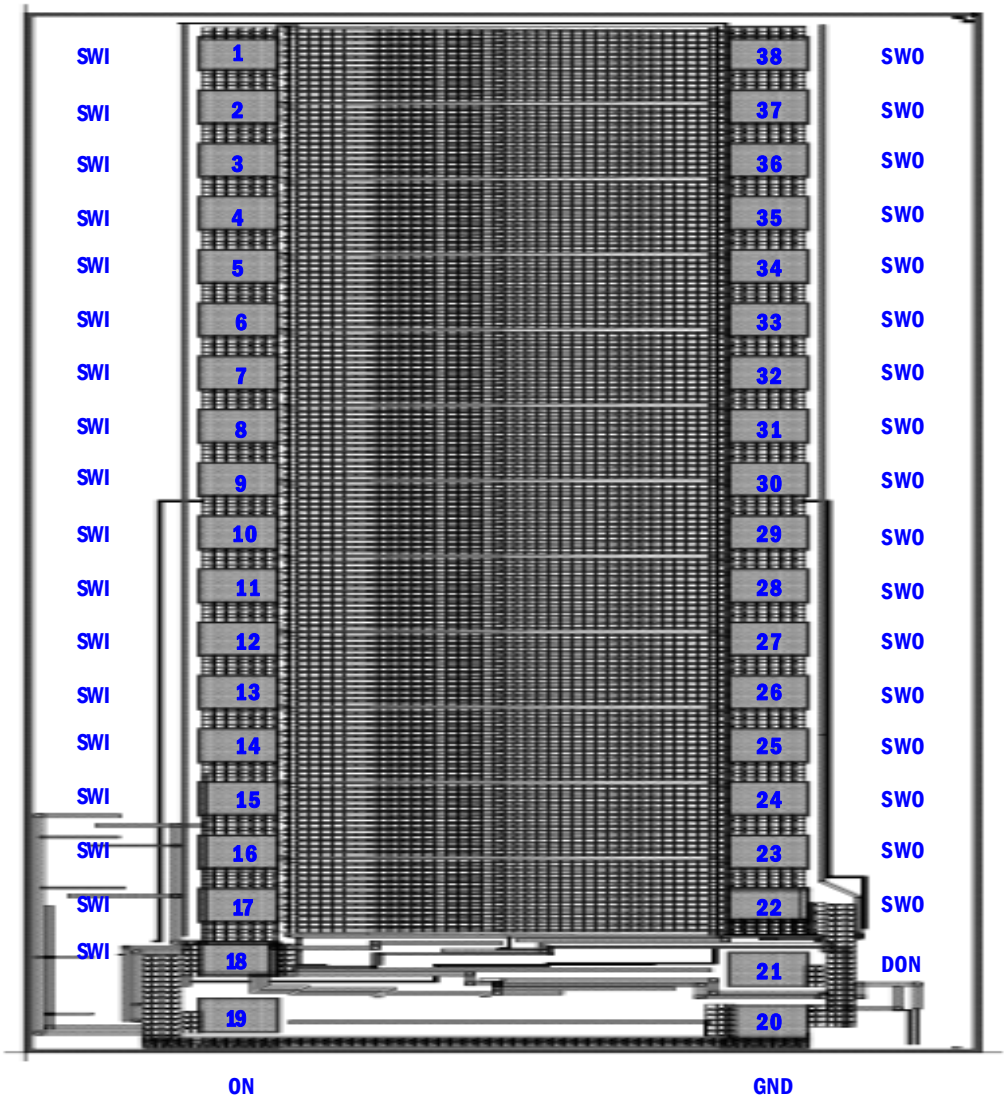


FIGURE A-1. Die bonding pad locations and electrical functions.

Die layout X – Y coordinates

Pad name	Pad number	X (μm)	Y (μm)	Pad name	Pad number	X (μm)	Y (μm)
SWI	1	-636.8	2679.6	SWO	38	636.8	2701.05
SWI	2	-636.8	2379.6	SWO	37	636.8	2401.05
SWI	3	-636.8	2079.6	SWO	36	636.8	2101.05
SWI	4	-636.8	1779.6	SWO	35	636.8	1801.05
SWI	5	-636.8	1479.6	SWO	34	636.8	1501.05
SWI	6	-636.8	1179.6	SWO	33	636.8	1201.05
SWI	7	-636.8	879.6	SWO	32	636.8	901.05
SWI	8	-636.8	579.6	SWO	31	636.8	601.05
SWI	9	-636.8	279.6	SWO	30	636.8	301.05
SWI	10	-636.8	-20.4	SWO	29	636.8	1.05
SWI	11	-636.8	-320.4	SWO	28	636.8	-298.95
SWI	12	-636.8	-620.4	SWO	27	636.8	-598.95
SWI	13	-636.8	-920.4	SWO	26	636.8	-898.95
SWI	14	-636.8	-1220.4	SWO	25	636.8	-1198.95
SWI	15	-636.8	-1520.4	SWO	24	636.8	-1498.95
SWI	16	-636.8	-1820.4	SWO	23	636.8	-1798.95
SWI	17	-636.8	-2120.4	SWO	22	636.8	-2098.95
SWI	18	-636.8	-2420.4	DON	21	636.8	-2398.95
ON	19	-636.8	-2720.4	GND	20	636.8	-2698.95

Die layout X – Y coordinates notes:

1. Origin of coordinates is the center of the die.
2. Pad size for all pads: 185 μm x 185 μm.
3. Bond wire size: 0.002 inch.

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size : 2413 µm x 5969 µm
Die thickness: 483 µm ± 25 µm.

Interface materials.
Top metallization: AlCu (0.5%)
Thickness: 2.7 µm ± 0.4 µm
Backside metallization: None

Glassivation.
Type: Silicon oxide and silicon nitride
Thickness: 0.3 µm ± 0.03 µm and 1.2 µm ± 0.12 µm

Process.
P6

Assembly related information.
Substrate potential: Ground

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-04-16

Approved sources of supply for SMD 5962-19208 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1920801VXC	34371	ISL70061SEHVF
5962R1920801V9A	34371	ISL70061SEHVX
5962L1920802VXC	34371	ISL73061SEHVF
5962L1920802V9A	34371	ISL73061SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406