REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Neutron testing information to paragraph 1.5 and add paragraph 4.4.4.2 Neutron testing. Renumber Table IA footnotes to show sequence. - ro	25-03-14	J. ESCHMEYER

Revision Status of Sheets

REV	A	A	A																			
SHEET	23	24	25																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
19-05-10

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

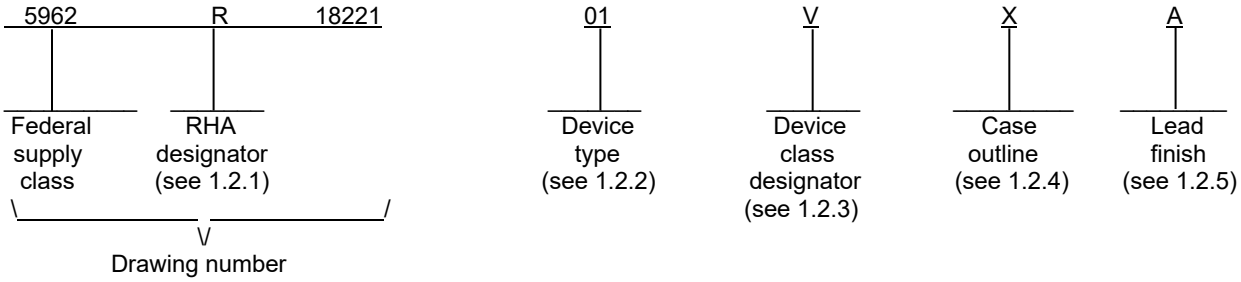
MICROCIRCUIT, LINEAR, 16 CHANNEL DRIVER CIRCUIT WITH INTEGRATED DECODER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-18221**
		SHEET 1 OF 25		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL72814SEH	Radiation hardened, 16 channel driver circuit with integrated decoder
02	ISL73814SEH	Radiation hardened, 16 channel driver circuit with integrated decoder

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F28	28	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

V_{CC} to GND	-0.3 V to +14.7 V
V_{CHX} to GND	-0.3 V to +42 V
V_{CHX} to GND under ion beam (RHA SEE testing)	-0.3 V to +34 V 2/
V_{COM} to GND	+42 V
V_{COM} to GND under ion beam (RHA SEE testing)	+34 V 2/
V_{COM} to highest positive CHX voltage	[V_{CHX} – 0.3] V to +42 V
V_{COM} to highest positive CHX voltage under ion beam (RHA SEE testing)	[V_{CHX} – 0.3] V to +34 V 2/
Logic input voltage (EN, Ax)	[GND – 0.3 V] to [V_{CC} + 0.3] V
Logic input current (EN, Ax)	±15 mA
Power dissipation, (P_D) (case temperature 125°C)	1.3 W
Peak I_{CHX} (100 ms)	1.1 A
Maximum supply turn-on ramp rate (V_{COM})	1 V/µs
Maximum supply turn-on ramp rate (V_{CC})	1 V/µs
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-ambient (θ_{JA})	34.5°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JC})	18.8°C/W 4/

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
V_{CC} supply voltage	3.0 V to 13.2 V
V_{CHX}	5 V to 34 V
Maximum lifetime channel current duty cycle limit versus I_{CHx}: 5/	
400 mA	100%
500 mA	73%
600 mA	51%
700 mA	37%
Maximum lifetime channel current duty cycle limit versus I_{CHx}: 6/	
250 mA	100%
300 mA	70%
400 mA	39%
500 mA	25%
600 mA	17%
700 mA	13%

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Tested in a heavy ion environment at LET = 86 MeV/(mg/cm^2) at +125°C (T_C) for SEB. Refer to manufacturer single event effects test report for more information.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer for more information.

4/ For θ_{JC}, the case temperature location is the center of the package underside.

5/ Based on assumed 1.6 x 10^5 hours Metallic Electro-migration limited lifetime at 125°C junction temperature to 0.1% failures.

6/ Based on assumed 1.6 x 10^5 hours Metallic Electro-migration limited lifetime at 150°C junction temperature to 0.1% failures.

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s):
Device type 01 ..... 100 krad(Si) 7/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s):
Devices type 01 and 02 ..... 50 krad(Si) 7/ 8/
Neutron irradiation Displacement Damage (DD) test (1 MeV equivalent) ..... 1×10^{13} neutron/cm^2

Single event phenomena (SEP):
No SEL occurs at effective linear energy transfer (LET) (see 4.4.4.3) ..... ≤ 86 MeV/(mg/cm^2) 9/ 10/
No SEB at V_{CHx} and V_{COM} = 34 V occurs at surface LET (see 4.4.4.3) ..... ≤ 86 MeV/(mg/cm^2) 10/
Single event transients (SET) observed at an effective LET (see 4.4.4.3)
(SET magnitude of 300 mA at a cross section 3.1×10^{-5}cm^2 per channel) ..... = 20 MeV/(mg/cm^2) 10/

7/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krad(Si), and condition D to a maximum total ionizing dose (TID) of 75 krad(Si). However, the device 01 is marked at the high dose rate condition A to TID level 100 krad(Si) of RHA level R.

8/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device type 02 is wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krad(Si) of RHA level L.

9/ Devices are manufactured in a dielectrically isolated silicon on insulator(SOI) process wherein latch up is verified and no latch-up has occurred.

10/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but, are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
POWER SUPPLY							
Supply current	I_{CC}	V_{CC} = 3.6 V, 13.2 V, CHX = OPEN, EN = V_{CC}, COM = 0 V, A0 – A3 = 0 V	1, 2, 3	01, 02	4.5	8.5	mA
		M, D, P, L, R	1 2/		4.5	8.5	
Quiescent supply current	I_{CCQ}	V_{CC} = 3.6 V, 13.2 V, CHX = OPEN, EN = 0 V, COM = 0 V, A0 – A3 = 0 V	1, 2, 3	01, 02	350	800	µA
		M, D, P, L, R	1 2/		350	800	
DRIVER CIRCUIT							
Single channel leakage current	I_{CHLK}	V_{CHX} (under test) = 34 V, All other V_{CHX} channels = 35 V, V_{CC} = 3 V, 5.5 V, COM = 35 V, A0 – A3 = 0 V, EN = 0 V	1, 3	01, 02	-25	25	nA
			2		10	90	
		M, D, P, L, R	1 2/		-25	25	
All channels + COM leakage current	$I_{TOTCHLK}$	$V_{CH0 – CH15}$ = COM = 34 V, V_{CC} = 3 V, 5.5 V, A0 – A3 = 0 V,	1, 3	01, 02	-30	30	nA
			2		-30	1000	
		EN = 0 V M, D, P, L, R	1 2/		-30	100	
Output channel saturation voltage	V_{CHx} (SAT)	I_{CHx} = 700 mA, COM = 35 V, V_{CC} = 3 V, 5.5 V, EN = V_{CC}	1, 2, 3	01, 02	0.85	1.5	V
		M, D, P, L, R	1 2/		0.85	1.5	
		I_{CHx} = 600 mA, COM = 35 V, V_{CC} = 3 V, 5.5 V, EN = V_{CC}	1, 2, 3		0.8	1.4	
		M, D, P, L, R	1 2/		0.8	1.4	
		I_{CHx} = 500 mA, COM = 35 V, V_{CC} = 3 V, 5.5 V, EN = V_{CC}	1, 2, 3		0.65	1.35	
		M, D, P, L, R	1 2/		0.65	1.35	
		I_{CHx} = 350 mA, COM = 35 V, V_{CC} = 3 V, 5.5 V, EN = V_{CC}	1, 2, 3		0.6	1.3	
		M, D, P, L, R	1 2/		0.6	1.3	
		I_{CHx} = 200 mA, COM = 35 V, V_{CC} = 3 V, 5.5 V, EN = V_{CC}	1, 2, 3		0.5	1.2	
		M, D, P, L, R	1 2/		0.5	1.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
COM to CHx Inductive kickback clamp diode forward voltage	V_F	I_{CHx} = 200 mA, COM = 0 V, V_{CC} = 0 V, A0 – A3 = 0 V,		1, 2, 3	01, 02	0.85	1.3	V
		EN = 0 V	M, D, P, L, R	1 2/		0.85	1.3	
		I_{CHx} = 700 mA, COM = 0 V, V_{CC} = 0 V, A0 – A3 = 0 V,		1, 2, 3		1.0	2.25	
		EN = 0 V	M, D, P, L, R	1 2/		1.0	2.25	
COM to CHx inductive kickback clamp diode leakage current	I_R	V_{COM} = 34 V, V_{CC} = 0 V, A0 – A3 = 0 V, EN = 0 V, CHx channel under test = 0 V, other CHx channels = open.		1, 2, 3	01, 02	-15	15	nA
			M, D, P, L, R	1 2/		-15	15	
DECODER AND ENABLE INPUTS								
High logic level voltage	V_{IH}	V_{CC} = 3.0 V, 13.2 V, COM = V_{CC}		1, 2, 3	01, 02	2		V
			M, D, P, L, R	1 2/		2		
Low logic level voltage	V_{IL}	V_{CC} = 3.0 V, 13.2 V, COM = V_{CC}		1, 2, 3	01, 02		0.8	V
			M, D, P, L, R	1 2/			0.8	
Input high current	I_{IH}	V_{CC} = 3.0 V, 5.5 V, COM = V_{CC}, put input logic input (A0 – A3 and EN) = 2.0 V.		1, 2, 3	01, 02	-250	250	nA
			M, D, P, L, R	1 2/		-250	250	
Input low current	I_{IL}	V_{CC} = 3.0 V, 5.5 V, COM = V_{CC}, put input logic input (A0 – A3 and EN) = 0.8 V.		1, 2, 3	01, 02	-250	250	nA
			M, D, P, L, R	1 2/		-250	250	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
SWITCHING CHARACTERISTICS								
Enable turn-on time, 3/ 4/	t_{EN}	V_{CC} = 3.0 V, 13.2 V, COM = 35 V, A0 - A3 = 0 V. CH0 channel connected to 97 Ω to 34 V, other CHx channels connected to 10 kΩ to 34 V.		9, 10, 11	01, 02		5	µs
		See Figure 4.	M, D, P, L, R	9 2/			5	
Disable turn-off time, 3/ 4/	t_{DIS}	V_{CC} = 3.0 V, 13.2 V, COM = 35 V, A0 - A3 = 0 V. CH0 channel under test connected to 97 Ω to 34 V, other CHx channels connected to 10 kΩ to 34 V.		9, 10, 11	01, 02		15	µs
		See Figure 4.	M, D, P, L, R	9 2/			15	

1/ Unless otherwise specified, V_{CC} = 3 V to 13.2 V, V_{CHX} = 34 V, V_{IH} (logic level high) = V_{CC}, V_{IL} (logic level low) = GND.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 02 is only tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein). Device type 02 is wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and is marked at the standard 50 krad(Si) level.

Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Addressing should only be changed while EN = 0, otherwise multiple outputs can be momentarily activated. See manufacturer data sheet, section titled "Ensuring Break-Before-Make (BBM) Operation".

4/ After disabling (EN = 0) and changing addresses, delay at least 10 µs before enabling (EN = 1) to the new channel. This prevents multiple outputs from being momentarily ON at the same time. See manufacturer data sheet, section titled "Ensuring Break-Before-Make (BBM) Operation".

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET) at bias $V_{CHx} = V_{COM} = +34$ V.
01, 02	No SEL observed	125°C	Effective LET= 86 MeV/(mg/cm^2) 3/ 4/
	No SEB observed	125°C	Surface LET= 86 MeV/(mg/cm^2) 3/ 4/
	SET observed	25°C	LET= 20 MeV/(mg/cm^2) 5/

1/ For SEP test conditions, see 4.4.4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Devices are manufactured in a dielectrically isolated silicon on insulator (SOI) process wherein latch up is verified and no latch-up has occurred. No single-event burnout (SEB) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(mg/cm^2).

4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

5/ SET observed at magnitude of 300 mA to a cross section 3.1 x 10^{-5}cm^2 per channel.
For SET test V_{CC} = 3.0 V and V_{CHx} = +34 V.
See manufacturer's single event effects report for further details.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A1	15	GND
2	A2	16	CH8
3	A3	17	CH9
4	GND	18	CH10
5	CH0	19	CH11
6	CH1	20	GND
7	CH2	21	CH12
8	CH3	22	CH13
9	GND	23	CH14
10	CH4	24	CH15
11	CH5	25	GND
12	CH6	26	VCC
13	CH7	27	EN
14	COM	28	A0
Package lid.	Tied internally to terminal 15 (GND).		

FIGURE 1. Terminal connections

A3	A2	A1	A0	EN	CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	0
0	0	0	1	1	1
0	0	1	0	1	2
0	0	1	1	1	3
0	1	0	0	1	4
0	1	0	1	1	5
0	1	1	0	1	6
0	1	1	1	1	7
1	0	0	0	1	8
1	0	0	1	1	9
1	0	1	0	1	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	1	13
1	1	1	0	1	14
1	1	1	1	1	15

NOTE: The truth table is verified by the Output channel saturation voltage ($V_{CHx(SAT)}$) test and uses the Low logic level voltage (V_{IL}) and High logic level voltage (V_{IH}) tests to check the individual addressing.

FIGURE 2. Truth table.

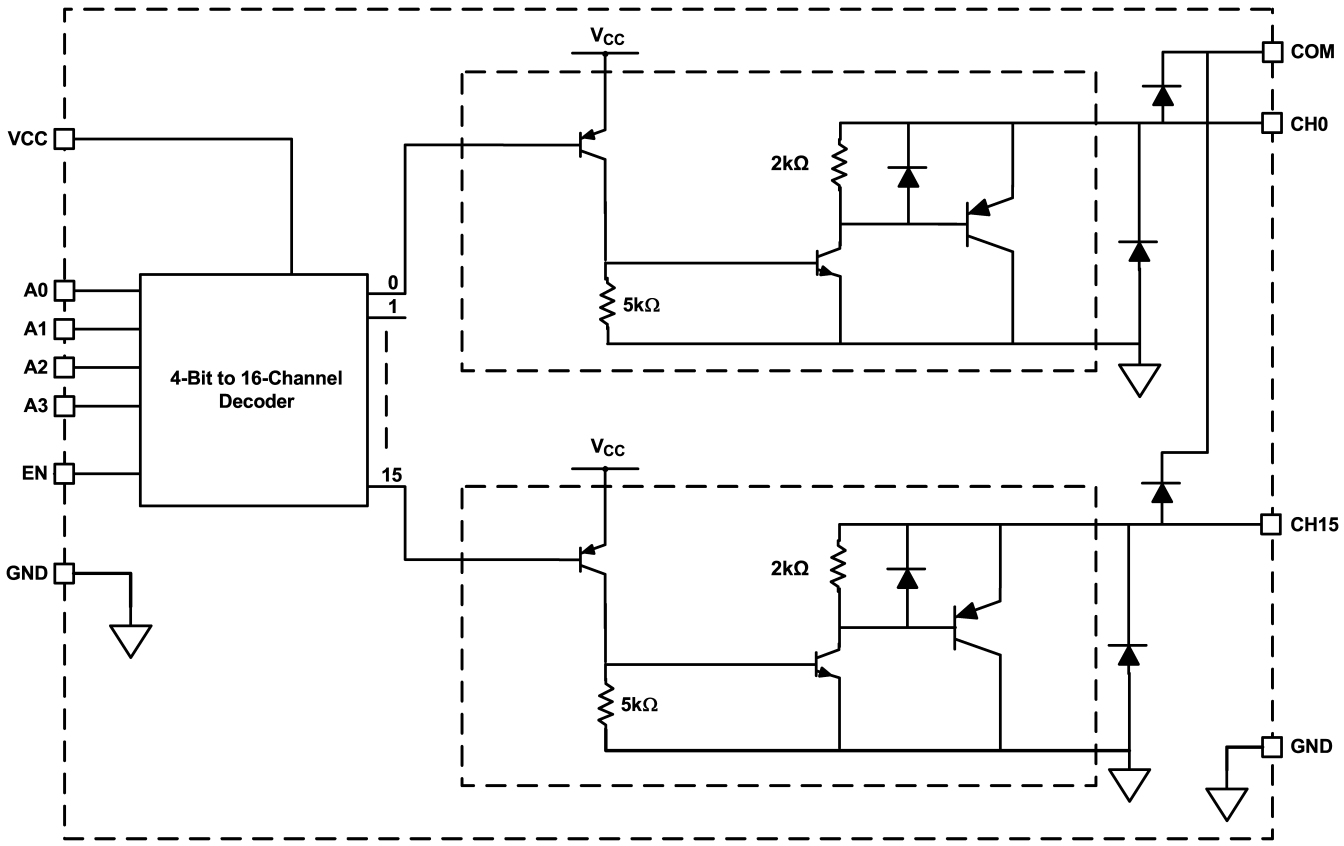


FIGURE 3. Logic diagram.

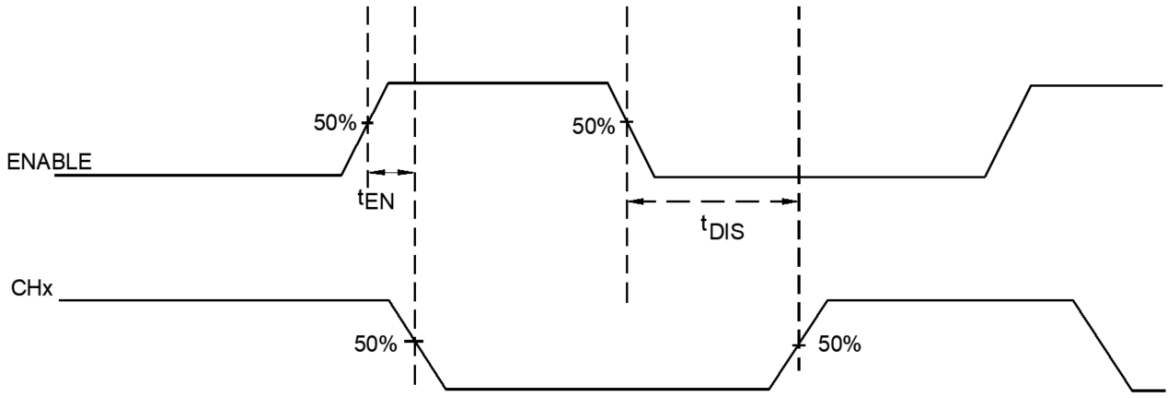


FIGURE 4. Timing diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, the truth table shall include verifying the functionality of the device.

c. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1 ,2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and delta.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.2 Neutron testing. When specified in the purchase order or contract, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ± 5°C after an exposure of 1×10^{13} neutrons/cm^2 (minimum).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
COM to CHx Inductive kickback clamp diode leakage current	I_R	V_{COM} = 34 V, V_{CC} = 0 V, A0 – A3 = 0 V, EN = 0 V, CHx channel under test = 0 V, other CHx channels = open.	±2 nA
Quiescent supply current	I_{CCQ}	V_{CC} = 3.6 V, 13.2 V, CHx = OPEN, EN = 0 V, COM = 0 V, A0 – A3 = 0 V	± 75 μA
Supply current	I_{CC}	V_{CC} = 3.6 V, 13.2 V, CHx = OPEN, EN = V_{CC}, COM = 0 V, A0 – A3 = 0 V	±0.8 mA
Input high current	I_{IH}	V_{CC} = 3.0 V, 5.5 V, COM = V_{CC}, (A0 – A3 and EN) = 2.0 V.	±25 nA
Input low current	I_{IL}	V_{CC} = 3.0 V, 5.5 V, COM = V_{CC}, (A0 – A3 and EN) = 0.8 V.	± 25nA
Single channel leakage current	I_{CHLK}	V_{CHX} (under test) = 34 V, All other V_{CHx} channels = 35 V, V_{CC} = 3 V, 5.5 V, COM = 35 V, A0 – A3 = 0 V, EN = 0 V	±20nA
Output channel saturation voltage	$V_{CHx(SAT)}$	I_{CHx} = 700 mA, V_{CC} = 3 V, 5.5 V, COM = 35 V, EN = V_{CC}	± 0.1V

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

c. Single event burn-out (SEB) observances.

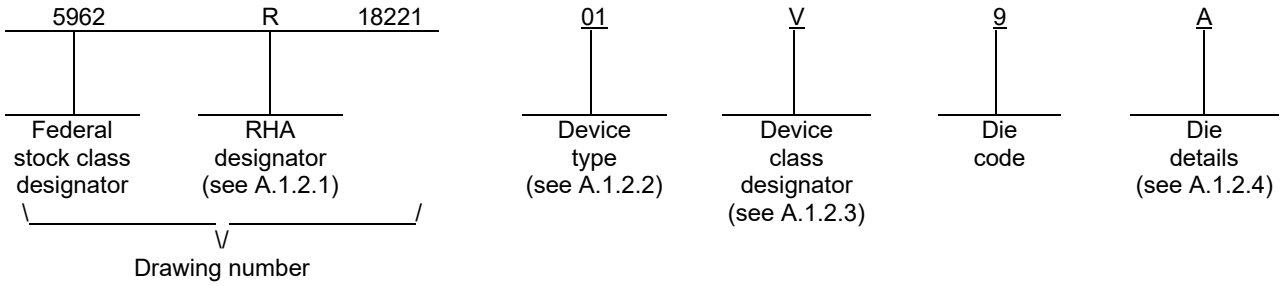
d. Single event transient (SET) observances.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-18221

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL72814SEH	16 channel driver circuit with integrated decoder
02	ISL73814SEH	16 channel driver circuit with integrated decoder

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2 and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

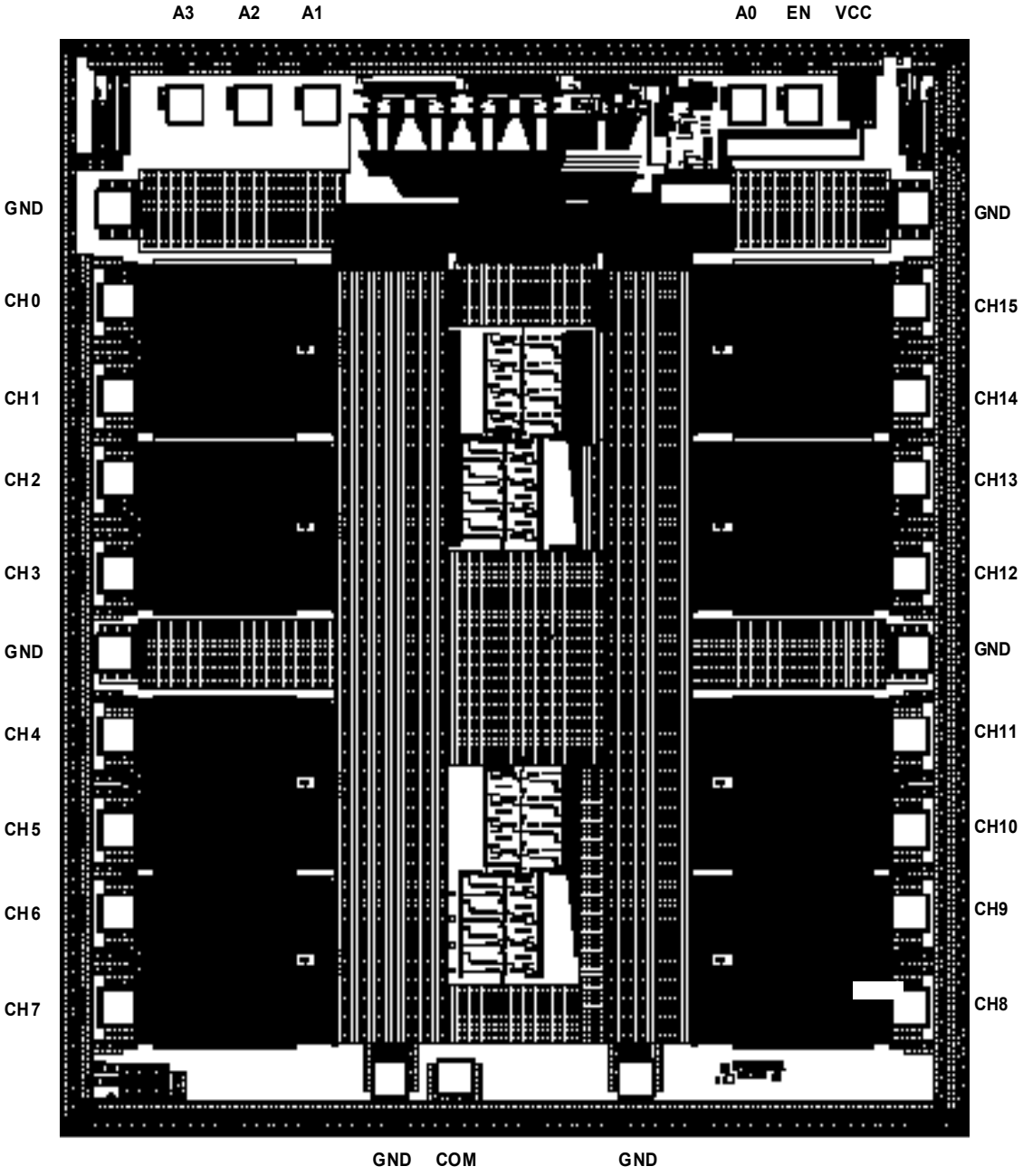


FIGURE A-1. Die bonding pad locations and pad names.

Die layout X – Y coordinates

Pad name	Pad number	X (μm)	Y (μm)
VCC	P1	2020.5	2771.5
EN	P2	1704.0	2749.0
A0	P3	1372.0	2749.0
A1	P4	-1137.0	2749.0
A2	P5	-1537.0	2749.0
A3	P6	-1937.0	2749.0
GND	P7	-2347.5	2154.5
CH0	P8	-2327.0	1624.0
CH1	P9	-2327.0	1088.0
CH2	P10	-2327.0	616.0
CH3	P11	-2327.0	80.0
GND	P12	-2347.5	-374.5
CH4	P13	-2327.0	-846.0
CH5	P14	-2327.0	-1382.0
CH6	P15	-2327.0	-1854.0
CH7	P16	-2327.0	-2390.0
GND	P17	-729.0	-2792.0
COM	P18	-345.5	-2792.0
GND	P19	719.5	-2792.0
CH8	P20	2327.0	-2390.0
CH9	P21	2327.0	-1854.0
CH10	P22	2327.0	-1382.0
CH11	P23	2327.0	-846.0
GND	P24	2347.5	-374.5
CH12	P25	2327.0	80.0
CH13	P26	2327.0	616.0
CH14	P27	2327.0	1088.0
CH15	P28	2327.0	1624.0
GND	P29	2347.5	2154.5

Die layout X – Y coordinates notes:

1. Origin of coordinates is the center of the die.
2. Pad size for all pads: 195 μm x 195 μm.
3. Bond wire size: 0.002 inch.
4. Pad Number P17 does not get bonded out in the package version.

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Die physical dimensions.
Die size: 5461 microns x 6350 microns.
Die thickness: 482.6 microns ± 25.4 microns.

Interface materials.
Top metallization: AlCu (99.5% / 0.5%)
Thickness: 30 kÅ

Backside finish.
Silicon

Glassivation.
Type: Nitrox
Thickness: 15 kÅ

Process.
Dielectrically isolated advanced bipolar technology – PR40

Assembly related information.
Substrate potential: Floating

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 25-03-14

Approved sources of supply for SMD 5962-18221 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1822101VXC	34371	ISL72814SEHVF
5962R1822101V9A	34371	ISL72814SEHVX
5962L1822102VXC	34371	ISL73814SEHVF
5962L1822102V9A	34371	ISL73814SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406