REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	24-01-26	J. ESCHMEYER

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
18-10-03

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, PRECISION CURRENT SOURCE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-18217**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

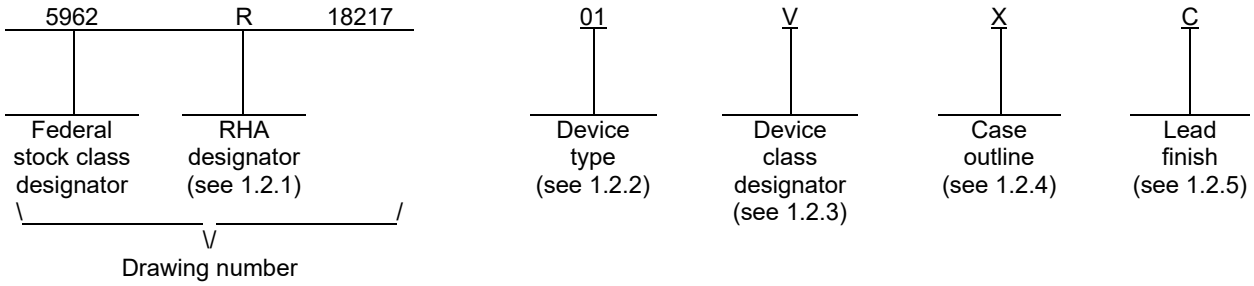
5962-E138-24

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70591SEH	Radiation hardened, 100 μA precision current source
02	ISL73591SEH	Radiation hardened, 100 μA precision current source
03	ISL70592SEH	Radiation hardened, 1 mA precision current source
04	ISL73592SEH	Radiation hardened, 1 mA precision current source

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	4	Ceramic metal seal flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Maximum supply voltage	42 V
Maximum supply voltage under heavy ion beam SEB test	35 V 2/
Maximum reverse voltage	-0.5 V
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-ambient (θ_{JA})	173°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA})	53°C/W 4/
Thermal resistance, junction-to-ambient (θ_{JC})	11°C/W 5/

1.4 Recommended operating conditions.

Supply voltage range	3 V to 40 V
Supply voltage under heavy ion beam SEB test	3 V to 35 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) :	
Device types 01 and 03	100 krad(Si) 6/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s) :	
Device types 01, 02, 03, and 04	50 krad(Si) 6/ 7/
Single event phenomena (SEP):	
No single event burn out (SEB) occurs at surface LET (at V = 35 V) (see 4.4.4.2)	≤ 86 MeV/(mg/cm^2) 8/
Single event transient (SET) observed at surface LET (see 4.4.4.2)	≥ 2.7 MeV/(mg/cm^2) 8/
No Single event latch-up (SEL) occurs at surface LET (see 4.4.4.2)	≤ 86 MeV/(mg/cm^2) 8/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Tested in a heavy ion environment at LET = 86 MeV/(mg/cm^2) and 125°C case temperature. Refer to manufacturer single event effects test report for more information.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (2 buried 1 oz. planes). Air GAP between package and printed circuit board (PCB). See manufacturer for more information.

4/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board with direct attach features (2 buried 1 oz planes, thermal land under package with 16 vias touching 1 of the buried planes). Package base mounted to PCB thermal land with 0.25 mm (~ 10 mil) thick adhesive material with “k” of 1 W/m-K.

5/ For θ_{JC}, the case temperature location is the center of the package underside.

6/ Device types 01 and 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krad(Si), and condition D to a maximum total ionizing dose (TID) of 75 krad(Si). The devices are marked at the high dose rate condition A to TID level 100 krad(Si).

7/ Device types 02 and 04 are tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device types 02 and 04 are wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) TID level.

8/ Manufacturer supplying device types 01-04 has performed heavy ion SEE test and observed no SEB or SEL with gold (Au) at normal incidence, corresponding to a surface LET of 86 MeV(mg/cm^2), with a bias +V = 35 V and case temperature = 125°C. SET were observed at surface LET = 2.7 MeV/(mg/cm^2) with neon (Ne) at a bias of 35 V and a ±1% trigger on current. Device types 01 and 02 under these conditions exhibited a cross section of 1.02 x 10^{-4}cm^2 and an extreme deviation of -12.1 µA. Device types 03 and 04 exhibited a cross section of 3.20 x 10^{-4}cm^2 and an extreme deviation of +340 µA. Device types 01-04 are manufactured using a silicon on insulator (SOI) technology. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

Special marking for device class V for case outline X. The marking of the PIN number may be reduced to the RHA designator, the 5 digit drawing designator, the device type (single digit), and device class (for example, R1821701V on the 01 device type).

Device type 01 part number marking for device class V will be R1821701V.
Device type 02 part number marking for device class V will be L1821702V.
Device type 03 part number marking for device class V will be R1821703V.
Device type 04 part number marking for device class V will be L1821704V.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
100 µA current source specifications								
Output current at 40 V	I_{O40V}	+V = 40 V		1	01, 02	99.79	100.69	µA
				2		99.33	100.47	
				3		99.39	100.78	
			M, D, P, L, R	1 2/		99.44	100.80	
Output current at 30 V	I_{O30V}	+V = 30 V		1	01, 02	99.75	100.43	µA
				2		99.39	100.23	
				3		99.22	100.34	
			M, D, P, L, R	1 2/		99.29	100.57	
Output current at 20 V	I_{O20V}	+V = 20 V		1	01, 02	99.71	100.38	µA
				2		99.39	100.16	
				3		99.12	100.23	
			M, D, P, L, R	1 2/		99.23	100.53	
Output current at 12 V	I_{O12V}	+V = 12 V		1	01, 02	99.67	100.38	µA
				2		99.35	100.15	
				3		99.04	100.18	
			M, D, P, L, R	1 2/		99.16	100.54	
Output current at 3 V	I_{O3V}	+V = 3 V		1	01, 02	99.58	100.42	µA
				2		99.26	100.26	
				3		98.88	100.12	
			M, D, P, L, R	1 2/		99.03	100.58	
Output impedance	R_{OUT}	+V = 3 V to 40 V, five point box method, points: 3 V, 12 V, 20 V, 30 V, and 40 V.		1,2,3	01, 02	40		MΩ
			M, D, P, L, R	1 2/		40		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
100 µA current source specifications – continued.								
Turn-on time	t_{ON}	+V = 0 V to 3.1 V with a 3.1 V / 10 µs ramp, R_L = 1 kΩ, measure from 10% of +V to when V_{OUT} has settled to within 0.5% of V_{OUT} final value of 100 mV, see figures 4, 5		9, 10, 11	01, 02		260	µs
			M, D, P, L, R	9 2/			260	
		+V = 0 V to 40 V with a 40 V / 100µs ramp, R_L = 1 kΩ, measure from 10% of +V to when V_{OUT} has settled to within 0.5% of V_{OUT} final value of 100mV, see figures 4, 5		9, 10, 11	01, 02		190	
			M, D, P, L, R	9 2/			190	
1 mA current source specifications								
Output current at 40 V	I_{O40V}	+V = 40 V		1	03, 04	0.9994	1.0078	mA
				2		0.9944	1.0066	
				3		0.9957	1.0100	
			M, D, P, L, R	1 2/		0.9990	1.0110	
Output current at 30 V	I_{O30V}	+V = 30 V		1	03, 04	0.9986	1.0052	mA
				2		0.9945	1.0031	
				3		0.9933	1.0051	
			M, D, P, L, R	1 2/		0.9950	1.0080	
Output current at 20 V	I_{O20V}	+V = 20 V		1	03, 04	0.9980	1.0040	mA
				2		0.9940	1.0019	
				3		0.9919	1.0038	
			M, D, P, L, R	1 2/		0.9940	1.0070	
Output current at 12 V	I_{O12V}	+V = 12 V		1	03, 04	0.9972	1.0036	mA
				2		0.9929	1.0012	
				3		0.9910	1.0032	
			M, D, P, L, R	1 2/		0.9930	1.0070	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
1 mA current source specifications – continued.								
Output current at 3 V	I_{O3V}	+V = 3 V		1	03, 04	0.9960	1.0039	mA
				2		0.9914	1.0016	
				3		0.9897	1.0027	
			M, D, P, L, R	1 2/		0.9910	1.0070	
Output impedance	R_{OUT}	+V = 3 V to 40 V, five point box method, points: 3 V, 12 V, 20 V, 30 V, and 40 V.		1,2,3	03, 04	4		MΩ
			M, D, P, L, R	1 2/		4		
Turn-on time	t_{ON}	+V = 0 V to 3.1 V with a 3.1 V / 10 µs ramp, R_L = 1 kΩ, measure from 10% of +V to when V_{OUT} has settled to within 0.5% of V_{OUT} final value of 100 mV, see figures 4, 5		9, 10, 11	03, 04		230	µs
			M, D, P, L, R	9 2/			230	
		+V = 0 V to 40 V with a 40 V / 100 µs ramp, R_L = 1 kΩ, measure from 10% of +V to when V_{OUT} has settled to within 0.5% of V_{OUT} final value of 100 mV, see figures 4, 5		9, 10, 11	03, 04		170	
			M, D, P, L, R	9 2/			170	

1/ Unless otherwise specified, +V = 20 V

2/ RHA device types 01 and 03 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device types 01 and 03 are only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein).
RHA device types 02 and 04 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device types 02 and 04 are only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krad(Si). Device types 02 and 04 are wafer acceptance tested 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) level.
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET)
01, 02, 03, 04	No SEL occurs +V = 35 V	125°C	Normal incidence LET ≤ 86 MeV/(mg/cm^2) 3/ 5/
	No SEB occurs at +V = 35 V	125°C	Normal incidence LET ≤ 86 MeV/(mg/cm^2) 3/ 5/
	SET observed	25°C	Normal incidence LET ≥ 2.7 MeV/(mg/cm^2) 4/ 5/

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The manufacturer supplying device types 01-04 has performed heavy ion SEE tests and observed no SEB or SEL with gold (Au) at normal incidence, corresponding to a surface LET of 86 MeV(mg/cm^2), with a bias +V = 35 V and case temperature = 125°C. For more information on SEP test results, customers are requested to contact the manufacturer.

4/ SET were observed at surface LET = 2.7 MeV/(mg/cm^2) with neon (Ne) at a bias of 35 V and a ±1% trigger on current. Device types 01 and 02 under these conditions exhibited a cross section of 1.02 x 10^{-4}cm^2 and an extreme deviation of -12.1 µA. Device types 03 and 04 exhibited a cross section of 3.20 x 10^{-4}cm^2 and an extreme deviation of +340 µA. For more information on SEP test results, customers are requested to contact the manufacturer.

5/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract.

Case X

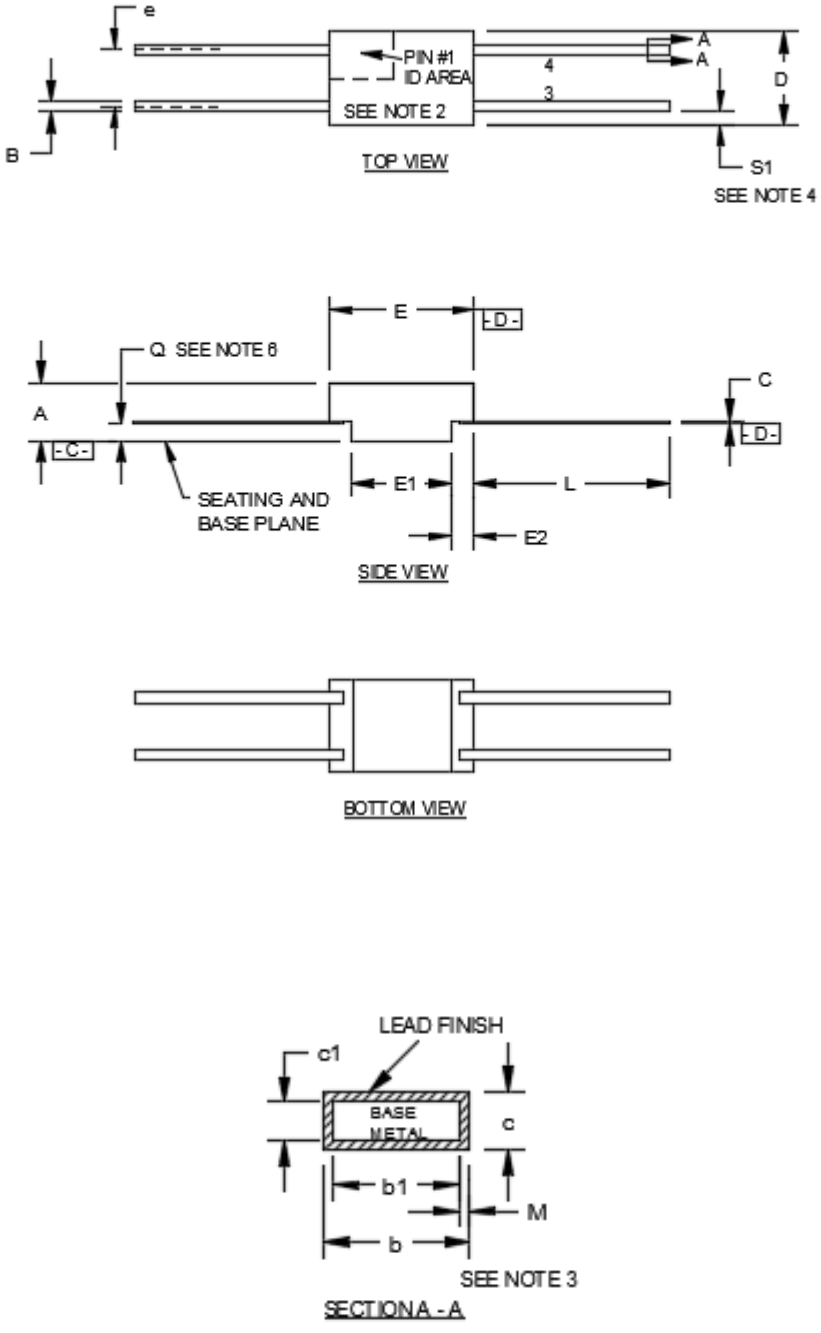


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.090	.112	2.29	2.84
b	.015	.022	0.38	0.56
b1	.015	.019	0.38	0.48
B	.015	.022	0.38	0.56
c	.004	.009	0.10	0.23
c1	.004	.006	0.10	0.15
D	.157	.173	3.99	4.39
e	.100 BSC		2.54 BSC	
E	.245	.265	6.22	6.75
E1	.167	.183	4.24	4.65
E2	.03	---	0.76	---
L	.325	.370	8.26	9.40
M	---	.0015	---	0.04
Q	.026	.038	0.66	0.97
S1	.005	---	0.13	---

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Index area: A notch or a pin 1 and shall be located adjacent to pin 1 and shall within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by .0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is a ceramic surface.

FIGURE 1. Case outline - continued.

Device types	01, 02, 03, 04	
Case outline	X	
Terminal number	Terminal symbol	Description
1	+V	Positive voltage lead, range 3 V to 40 V with respect to -V.
2	DNC	DNC (DO NOT CONNECT) = OPEN (Float). Internally connected
3	DNC	DNC (DO NOT CONNECT) = OPEN (Float). Internally connected
4	-V	Negative voltage lead.
---	Package lid	Internally connected to -V (pin 4).

FIGURE 2. Terminal connections.

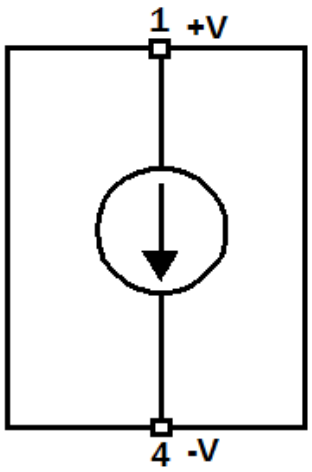
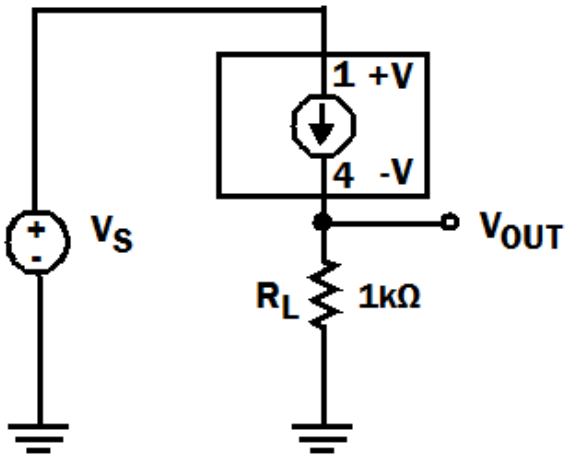
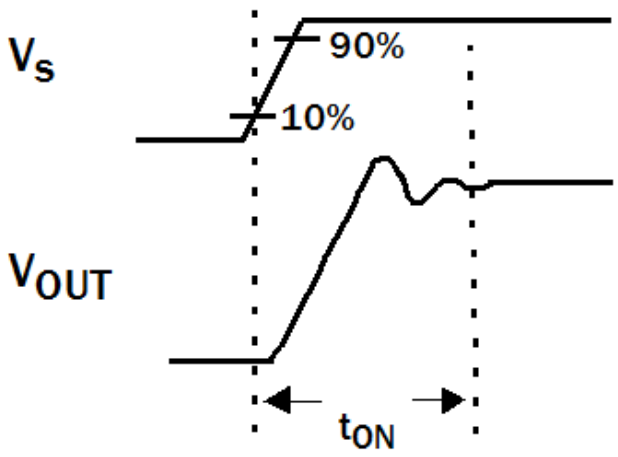


FIGURE 3. Block diagram.



NOTE: Unless otherwise specified, 0 V to 40 V ramp rate 40 V / 100 μs.

FIGURE 4. Electrical turn-on time test circuit.



NOTE: Measure from 10% of V_S to when V_{OUT} has settled to within 0.5% of V_{OUT} final value.

FIGURE 5. Electrical turn-on time waveform.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1 ,2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and delta.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Device type	Min	Max	Units
100 μA current source						
Output current at 40 V	I_{O40V}	+V = 40 V	01, 02	-	0.25	μA
Output current at 20 V	I_{O20V}	+V = 20 V		-	0.25	
Output current at 3 V	I_{O3V}	+V = 3 V		-	0.25	
1 mA current source						
Output current at 40 V	I_{O40V}	+V = 40 V	03, 04	-	0.0025	mA
Output current at 20 V	I_{O20V}	+V = 20 V		-	0.0025	
Output current at 3 V	I_{O3V}	+V = 3 V		-	0.0025	

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEB test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

c. Single event burn-out (SEB) observances.

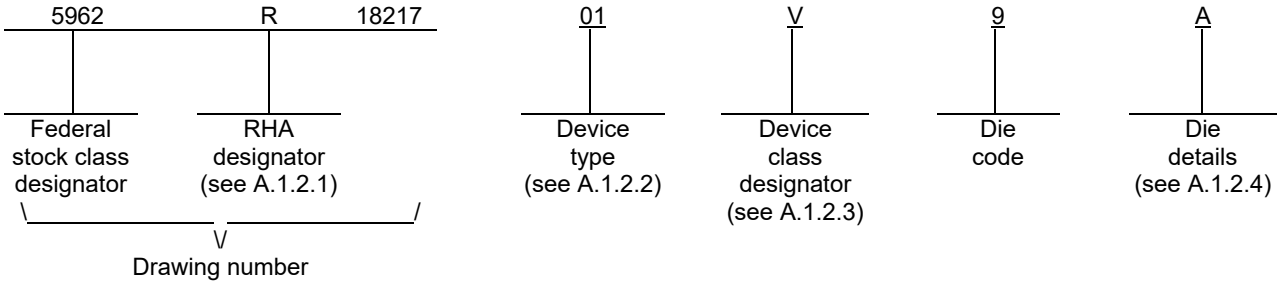
d. Single event transient (SET) observances.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-18217

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70591SEH	Radiation hardened, 100 μA precision current source
02	ISL73591SEH	Radiation hardened, 100 μA precision current source
03	ISL70592SEH	Radiation hardened, 1 mA precision current source
04	ISL73592SEH	Radiation hardened, 1 mA precision current source

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

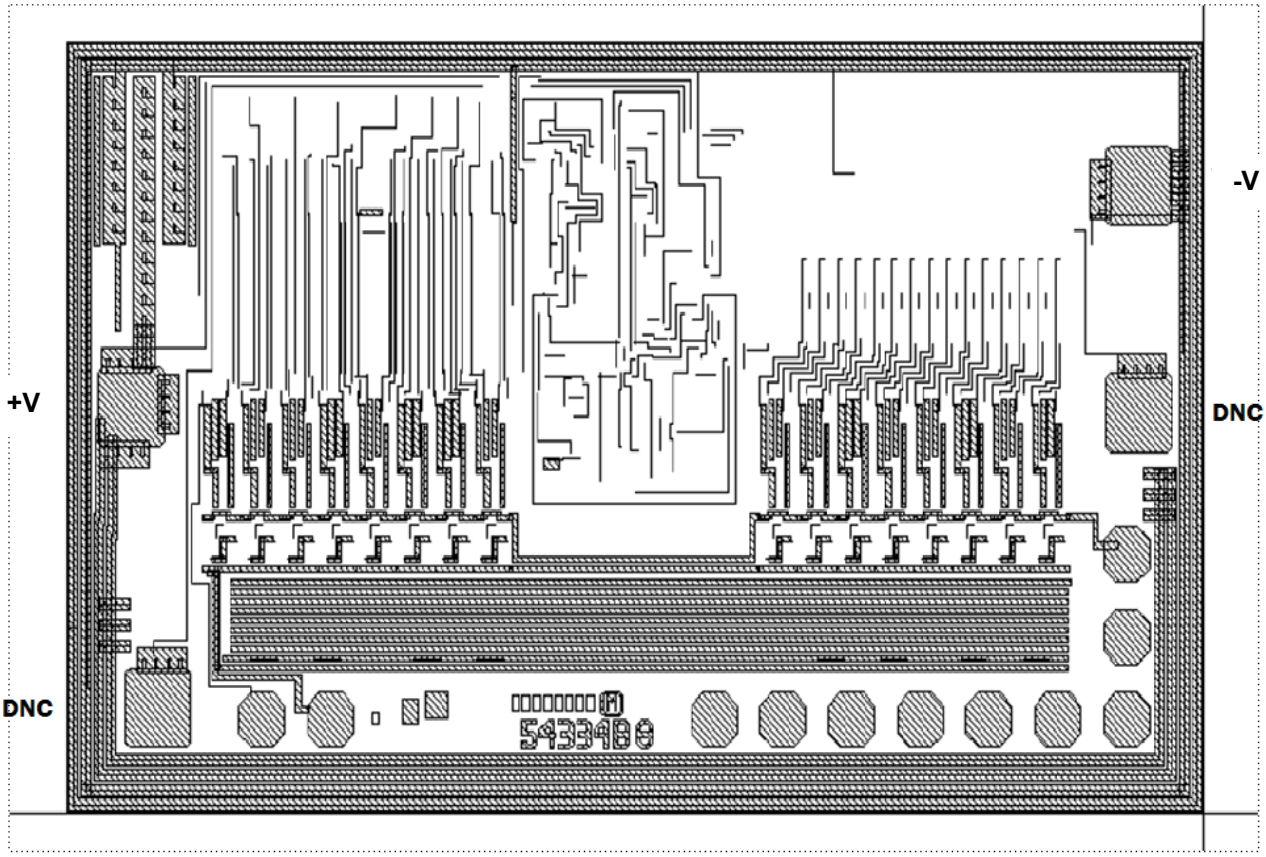


FIGURE A-1. Die bonding pad locations and electrical functions.

Layout X-Y coordinates					
Pad names	Pad numbers	X (μm)	Y (μm)	dX (μm)	dY (μm)
+V	1	-1025.5	34.5	110.0	110.0
DNC	2				
DNC	3				
-V	4	1025.5	408.0	110.0	110.0.

Note: Origin of the coordinates is the center of the die. Pads sorted in counter clock wise direction.

Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 2413 μm x 1397 μm (95 mils x 55 mils)
Die thickness: 483 μm ± 25.4 μm (19 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5% / 0.5%)
Thickness: 30 kÅ

Backside finish.
Silicon

Glassivation.
Type: Nitrox
Thickness: 15 kÅ

Process.
Dielectrically Isolated Advanced Bipolar Technology – PR40

Assembly related information.
Substrate potential: Tied to -V pin.
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-01-26

Approved sources of supply for SMD 5962-18217 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1821701VXC	34371	ISL70591SEHVF
5962R1821701V9A	34371	ISL70591SEHVX
5962L1821702VXC	34371	ISL73591SEHVF
5962L1821702V9A	34371	ISL73591SEHVX
5962R1821703VXC	34371	ISL70592SEHVF
5962R1821703V9A	34371	ISL70592SEHVX
5962L1821704VXC	34371	ISL73592SEHVF
5962L1821704V9A	34371	ISL73592SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert Conlan Blvd. NE Palm Bay, FL 32905-3406