REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to title block by deleting the word SILICON. Update document paragraphs to current MIL-PRF-38535 requirements. - ro	23-02-22	J. ESCHMEYER

Revision Status of Sheets

REV	A																				
SHEET	23																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RICK OFFICER CHECKED BY RAJESH PITHADIA	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
	APPROVED BY CHARLES F. SAFFLE DRAWING APPROVAL DATE 18-01-30	MICROCIRCUIT, LINEAR, SINGLE LOW SIDE FET DRIVER, MONOLITHIC GaN
AMSC N/A	REVISION LEVEL A	SIZE A | CAGE CODE **67268** | **5962-17233**
		SHEET 1 OF 23

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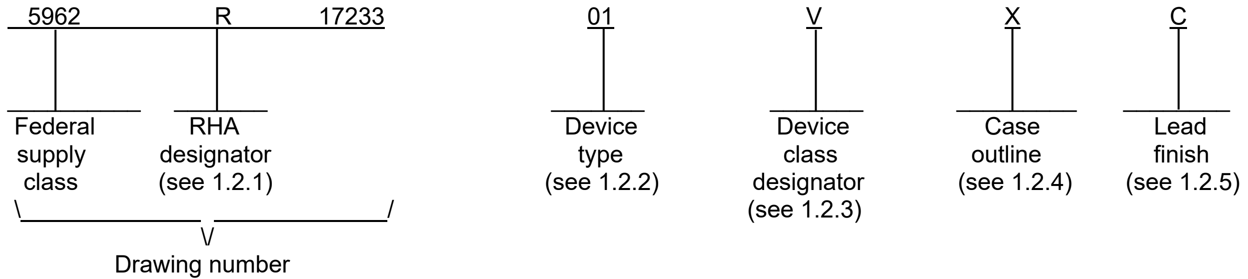
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70040SEH	Radiation hardened, single low side gallium nitride (GaN) field effect transistor (FET) driver
02	ISL73040SEH	Radiation hardened, single low side gallium nitride (GaN) field effect transistor (FET) driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Bottom terminal chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) .... GND - 0.3 V to GND +16.5 V
Non-inverting input (IN), inverting input (INB) .... GND - 0.3 V to GND +16.5 V
Low output (OUTL), high output (OUTH), gate drive voltage (VDRV) .... GND - 0.3 V to GND +6.5 V
Supply voltage (V_{DD}) .... GND - 0.3 V to GND +16.5 V 2/
Non-inverting input (IN), inverting input (INB .... GND - 0.3 V to GND +16.5 V 2/
Low output (OUTL), high output (OUTH), gate drive voltage (VDRV .... GND - 0.3 V to GND +6.2 V 2/
Storage temperature range .... -65°C to +150°C
Maximum junction temperature (T_J) .... +150°C
Lead temperature (soldering, 10 seconds) .... +275°C
Thermal resistance, junction-to-ambient (θ_{JA}) .... 59°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JC}) .... 10°C/W 4/

1.4 Recommended operating conditions.

V_{DD} supply voltage .... 4.5 V to 13.2 V
IN, INB .... 4.5 V to 13.2 V
Ambient operating temperature range (T_A) .... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) :
Device type 01 .... 100 krad(Si) 5/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s) :
Device types 01 and 02 .... 50 krad(Si) 5/ 6/
Single event phenomena (SEP):
No single event latchup (SEL) occurs at surface LET (see 4.4.4.3) .... ≤ 86 MeV/(mg/cm^2) 7/
No single event burn out (SEB) occurs at surface LET (see 4.4.4.3) .... ≤ 86 MeV/(mg/cm^2) 7/
Single event transient (SET) observed at surface LET (see 4.4.4.3) .... ≤ 86 MeV/(mg/cm^2) 7/
(with saturated x-section =1.7x10^{-6} cm^2) .... ≤ 86 MeV/(mg/cm^2) 7/

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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Tested in a heavy ion environment at LET = 86 MeV/(mg/cm^2) at +125°C (T_C) for SEB. Refer to manufacturer single event effects test report for more information.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer for more information.

4/ For θ_{JC}, the case temperature location is the center of the package underside.

5/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krad(Si), and condition D to a maximum total ionizing dose (TID) of 75 krad(Si). The devices are marked at the high dose rate condition A to a TID level 100 krad(Si).

6/ Device type 02 has been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device type 02 are wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) TID level.

7/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

Special marking for device class V for case outline X. The marking of the PIN number may be reduced to the RHA designator, the 5 digit drawing designator, the device type (single digit), and device class (for example, R172331V on the 01 device type).

Device type 01 part number marking for device class V will be R172331V.
Device type 02 part number marking for device class V will be L172332V.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535..

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Power supply							
Quiescent supply current	I_{DDQ}	V_{DD} = 4.5 V, IN = 0 V, INB = V_{DD}	1,2,3	01, 02		2.5	mA
		M, D, P, L, R, V_{DD} = 4.5 V, IN = 0 V, INB = V_{DD}	1 2/			2.5	
		V_{DD} = 13.2 V, IN = 0 V, INB = V_{DD}	1,2,3			2.5	
		M, D, P, L, R, V_{DD} = 13.2 V, IN = 0 V, INB = V_{DD}	1 2/			2.5	
Operating supply current	I_{DDO}	V_{DD} = 4.5 V, f_{PWM} = 500 kHz	1,2,3	01, 02		13	mA
		M, D, P, L, R, V_{DD} = 4.5 V, f_{PWM} = 500 kHz	1 2/			13	
		V_{DD} = 13.2 V, f_{PWM} = 500 kHz	1,2,3			15	
		M, D, P, L, R, V_{DD} = 13.2 V, f_{PWM} = 500 kHz	1 2/			15	
Gate drive voltage							
Output voltage	V_{DRV}	V_{DD} = 4.5 V	1,2,3	01, 02	4.29		V
		M, D, P, L, R, V_{DD} = 4.5 V	1 2/		4.29		
		V_{DD} = 13.2 V	1,2,3		4.34	4.71	
		M, D, P, L, R, V_{DD} = 13.2 V	1 2/		4.34	4.71	
Current limit on V_{DRV}	I_{LIM}	V_{DD} = 4.5 V, 13.2 V	1, 2, 3	01, 02	50	300	mA
		M, D, P, L, R, V_{DD} = 4.5 V, 13.2 V	1 2/		50	300	
Under voltage protection							
V_{DRV} rising threshold	V_{RDRV}		1, 2, 3	01, 02	3.75	4.15	V
		M, D, P, L, R	1 2/		3.75	4.15	
V_{DRV} falling threshold	V_{FDRV}		1, 2, 3	01, 02	3.4	4	V
		M, D, P, L, R	1 2/		3.4	4	
V_{DRV} threshold hysteresis	V_{HDRV}		1, 2, 3	01, 02	100	375	mV
		M, D, P, L, R	1 2/		100	375	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input pins							
High level threshold	V_{IH}		1, 2, 3	01, 02		2	V
		M, D, P, L, R	1 2/			2	
Low level threshold	V_{IL}		1, 2, 3	01, 02	1		V
		M, D, P, L, R	1 2/		1		
Input voltage hysteresis	V_{IHYS}		1, 2, 3	01, 02	120	450	mV
		M, D, P, L, R	1 2/		120	450	
Input pull up/down resistor	R_{EN}	IN to V_{SS}, INB to V_{DD}	1, 2, 3	01, 02	97	362	kΩ
		M, D, P, L, R, IN to V_{SS}, INB to V_{DD}	1 2/		97	362	
Input leakage current	I_{IN}/I_{INB}		1, 2, 3	01, 02	-1	1	μA
		M, D, P, L, R	1 2/		-1	1	
OUTH output							
Peak source 3/ current	I_{SRC}	C_L = 220 nF	1, 2, 3	01, 02	1	3	A
		M, D, P, L, R, C_L = 220 nF	1 2/		1	3	
Driver output resistance	R_{ONP}	I_{OUTH} = 45 mA	1, 2, 3	01, 02		3.2	Ω
		M, D, P, L, R, I_{OUTH} = 45 mA	1 2/			3.2	
OUTH leakage current	I_{LKP}	OUTH = 0 V, 4.5 V	1, 2, 3	01, 02	-1	1	μA
		M, D, P, L, R, OUTH = 0 V, 4.5 V	1 2/		-1	1	
OUTL output							
Peak sink 3/ current	I_{SNK}	C_L = 220 nF	1, 2, 3	01, 02	1.5	4.0	A
		M, D, P, L, R, C_L = 220 nF	1 2/		1.5	4.0	
Driver output resistance	R_{ONN}	OUTH = VDRV, I_{OUTL} = -45 mA	1, 2, 3	01, 02		1	Ω
		M, D, P, L, R, OUTH = VDRV, I_{OUTL} = -45 mA	1 2/			1	
		OUTH = OUTL, I_{OUTL} = -45 mA	1, 2, 3			3	
		M, D, P, L, R, OUTH = OUTL, I_{OUTL} = -45 mA	1 2/			3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OUTL output – continued.							
Gate hold-off resistance	R_{OUTL-P}	V_{DD} = 0 V, OUTL = 0.7 V	1, 2, 3	01, 02	400	700	Ω
		M, D, P, L, R, V_{DD} = 0 V, OUTL = 0.7 V	1 2/		400	700	
Power supply							
Turn ON propagation delay	t_{DON}	C_L = 1000 pF	9,10,11	01, 02	15	65	ns
		M, D, P, L, R, C_L = 1000 pF	9 2/		15	65	
Turn OFF propagation delay	t_{DOFF}	C_L = 1000 pF	9,10,11	01, 02	15	65	ns
		M, D, P, L, R, C_L = 1000 pF	9 2/		15	65	
Propagation delay matching	t_{DM}	$\lvert t_{DON} - t_{DOFF} \rvert$	9,10,11	01, 02	-8	8	ns
		M, D, P, L, R, $\lvert t_{DON} - t_{DOFF} \rvert$	9 2/		-8	8	
Rise time (10% to 90%) 3/	t_{RISE}	C_L = 10,000 pF	9,10,11	01, 02	21	90	ns
		M, D, P, L, R, C_L = 10,000 pF	9 2/		21	90	
Fall time (90% to 10%) 3/	t_{FALL}	C_L = 10,000 pF	9,10,11	01, 02	16	50	ns
		M, D, P, L, R, C_L = 10,000 pF	9 2/		16	50	

1/ Unless otherwise specified, V_{DD} = 4.5 V - 13.2 V, V_{SS} and V_{SSP} = 0 V, V_{IH} = 5.0 V, V_{IL} = 0 V. No load on OUTH or OUTL.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and levels M, D, P, and L of irradiation for condition D. However, device type 01 is only tested at the “R” level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein).
RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D.
However, device type 02 is only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krad(Si). Device type 02 is wafer acceptance tested 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) level.
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Test only applies to packaged parts due to hardware limitations at wafer probe.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET)
01 02	No SEL occurs	125°C	Normal incidence LET = 86 MeV/(mg/cm^2) 3/ 5/
	No SEB occurs	25°C	Normal incidence LET = 86 MeV/(mg/cm^2) 3/ 5/
	SET observed	25°C	Normal incidence LET = 86 MeV/(mg/cm^2) 4/ 5/

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(mg/cm^2) with bias V_{DD} = 16.5 V.

4/ Single-event transient (SET) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(cm^2/mg) with dynamic condition at V_{DD} = 4.5 V and 13.2 V for ±20 ns perturbations on a 500 kHz signal with fluence = 1 x 10^7 ion/cm^2 at x-section = 1.7 x 10^{-6} cm^2.

5/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

Case outline X

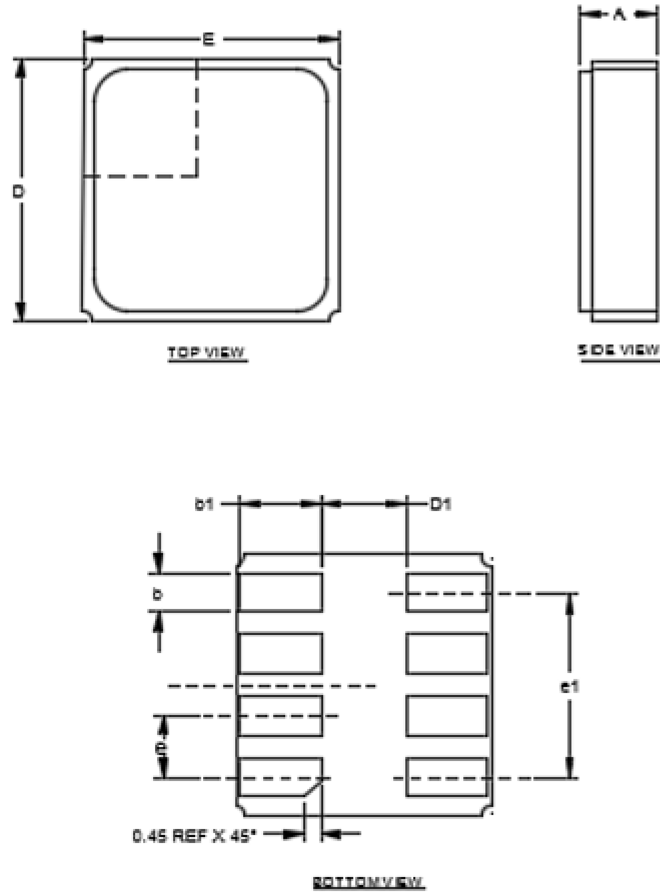


FIGURE 1. Case outline.

Case outline X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0622	.0779	1.58	1.98
b	.0322	.0385	0.82	0.98
b1	.0716	.0779	1.82	1.98
D	.2311	.2413	5.87	6.13
D1	.0755	.0818	1.92	2.08
E	.2311	.2413	5.87	6.13
e	.0519	.0582	1.32	1.48
e1	.1622	.1685	4.12	4.28

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The corner shape (radius, chamber, etc.) may vary at the manufacturer's option from that shown on the drawing.
3. The package thickness dimension is the package height before solder dipped.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD}	This is the supply for internal linear regulator of the device. The supply to V_{DD} should be locally bypassed using at least a 4.7 μF ceramic capacitor.
2	IN	Non-inverting input pin which controls OUTH and OUTL outputs. These inputs have TTL/CMOS type thresholds. When using this device in an inverting application this should be tied to V_{DD} to enable the outputs.
3	INB	Inverting input pin which controls OUTH and OUTL outputs. These inputs have TTL/CMOS type thresholds. When using this device in a non-inverting application this should be tied to V_{SS} to enable the outputs.
4	V_{SS}	Supply ground. Connect this pin to VSSP via the printed circuit board (PCB) ground plane.
5	VSSP	Power supply ground, Connect this pin to V_{SS} via the PCB ground plane.
6	OUTL	The output low pin is the gate driver turn-off output. Connect to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-off speed.
7	OUTH	The output high pin is the gate driver turn-on output. Connect to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-on speed.
8	VDRV	This pin is the output of the internal linear regulator and the gate drive voltage. This pin should be locally bypassed using at least a 4.7 μF ceramic capacitor.
---	Package lid	Internally connected to VSSP (Pin 5).

FIGURE 2. Terminal connections.

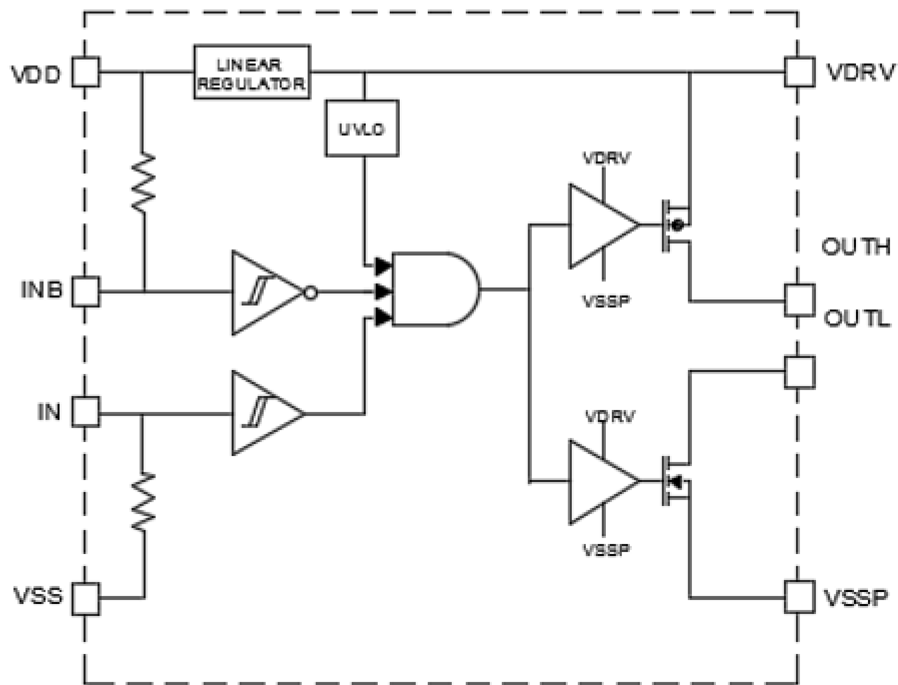


FIGURE 3. Functional block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1 ,2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and delta.

2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Device type	Min	Max	Units
Quiescent supply current	I_{DDQ}	V_{DD} = 13.2 V	01, 02	-0.25	0.25	mA
Operating supply current	I_{DDO}	V_{DD} = 13.2 V	01, 02	-1.5	+1.5	mA
Output drive voltage	V_{DRV}	V_{DD} = 13.2 V	01, 02	-0.074	0.074	V
Input leakage current	I_{IN}, I_{INB}		01, 02	-0.5	0.5	µA
Output leakage current	I_{LKP}	OUTH = 0 V, 4.5 V	01, 02	-0.5	0.5	µA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing.
The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

c. Single event burn-out (SEB) observances.

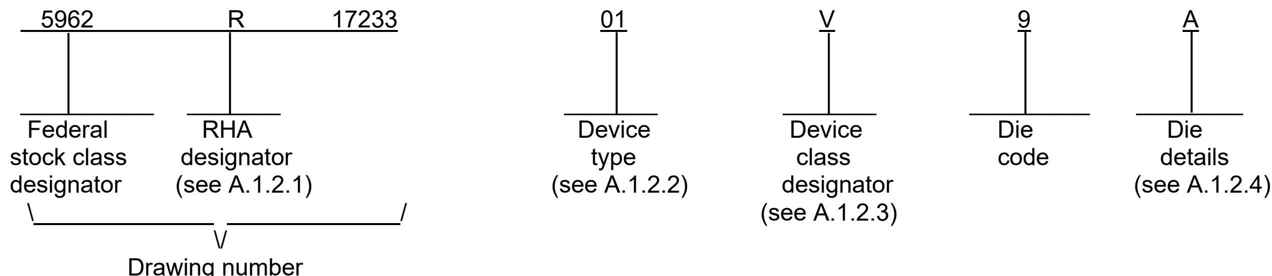
d. Single event transient (SET) observances.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-17233

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70040SEH	Radiation hardened, single low side GaN FET driver
02	ISL73040SEH	Radiation hardened, single low side GaN FET driver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-17233

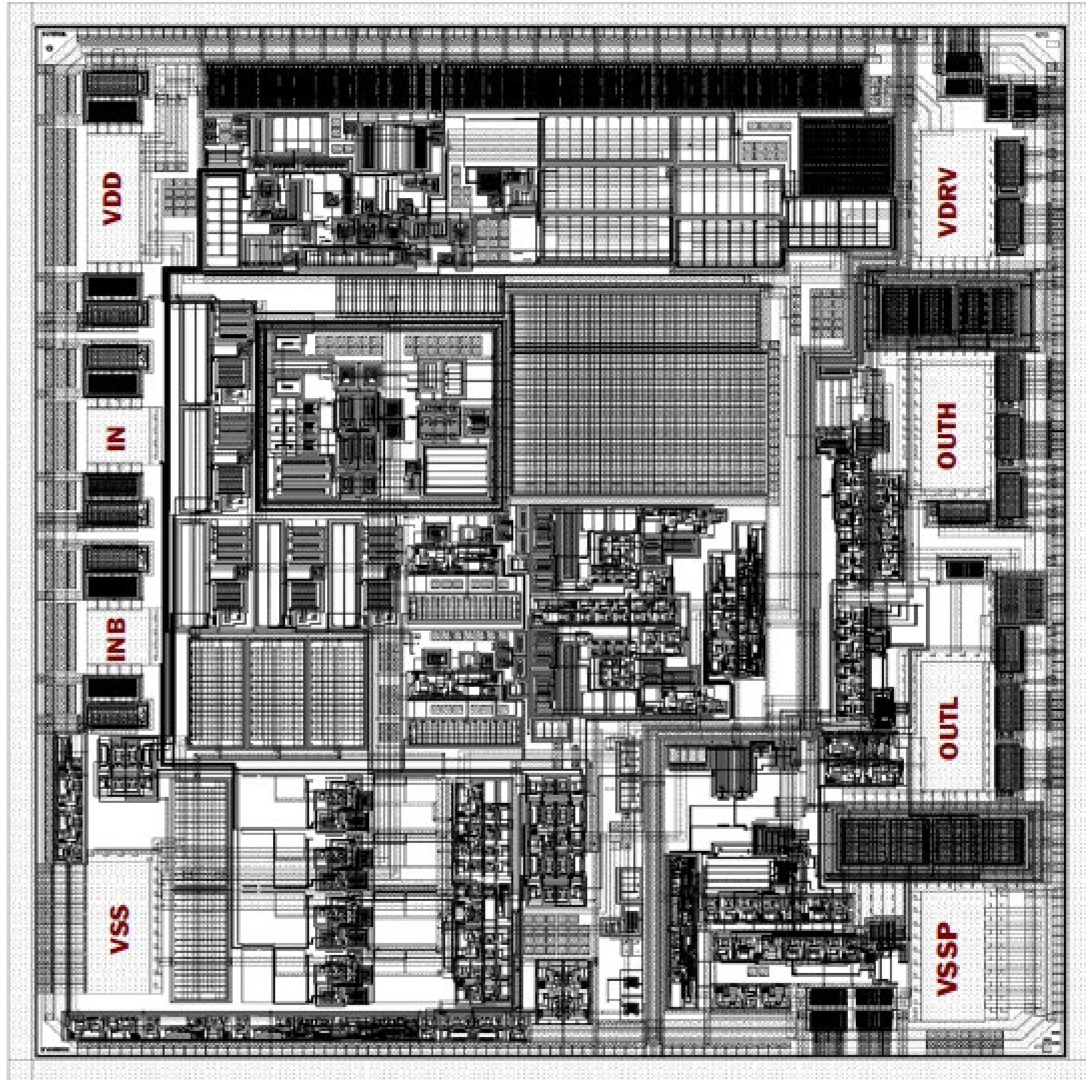


FIGURE A-1. Die bonding pad locations and electrical functions.

Pad name	Pad number	X µm	Y µm	dX µm	dY µm
V_{DD}	1	171.0	1968.15	120	290
IN	2	171.0	1423.85	120	135
INB	3	171.0	964.25	120	135
V_{SS}	4	171.0	298.2	120	290
VSSP	5	1878.65	231.0	120	290
OUTL	6	1878.65	758.5	120	290
OUTH	7	1878.65	1446.95	120	290
VDRV	8	1878.65	1973.85	120	290

Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 2230 µm x 2483 µm (87.8 mils x 97.8 mils)
Die thickness: 305 µm ± 25.4 µm (12 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5% / 0.5%)
Thickness: 2.7 µm ± 0.4 µm

Backside finish.
Silicon

Glassivation.
Type: Silicon oxide and silicon nitride
Thickness: 0.3 µm ± 0.03 µm to 1.2 µm ± 0.12 µm

Process.
0.6 µm BiCMOS junction isolated

Assembly related information.
Substrate potential: GND (V_{SS})
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-02-22

Approved sources of supply for SMD 5962-17233 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1723301VXC	34371	ISL70040SEHVL
5962R1723301V9A	34371	ISL70040SEHVX
5962L1723302VXC	34371	ISL73040SEHVL
5962L1723302V9A	34371	ISL73040SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert Conlan Blvd. Palm Bay, FL 32905

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.