REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current MIL-PRF-38535 requirements. - ro	24-05-09	J. ESCHMEYER

Revision Status of Sheets

REV	A	A	A																			
SHEET	23	24	25																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RICK OFFICER CHECKED BY RAJESH PITHADIA	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	APPROVED BY CHARLES F. SAFFLE DRAWING APPROVAL DATE 17-12-13	MICROCIRCUIT, LINEAR, QUAD POWER SUPPLY SEQUENCER, MONOLITHIC SILICON		
AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE 67268	5962-17225
		SHEET 1 OF 25		

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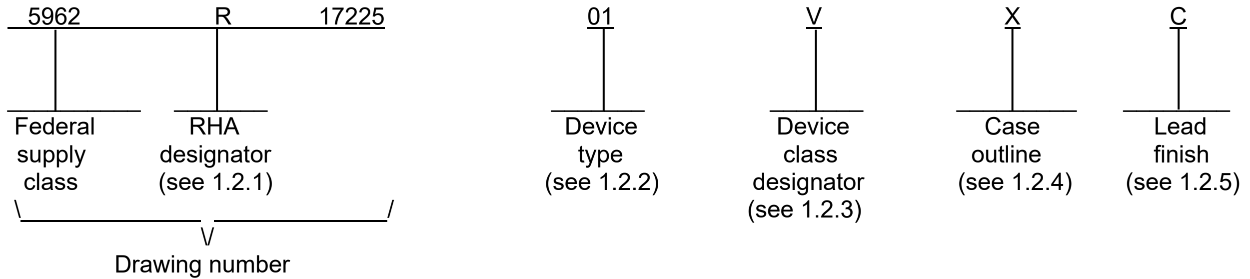
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70321SEH	Radiation hardened, quad power supply sequencer
02	ISL73321SEH	Radiation hardened, quad power supply sequencer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	18	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +16 V
V_{DD} to GND under ion beam (RHA SEE testing)	-0.3 V to +14.7 V 2/
VCC5 to GND	+6.5 V
VCC5 Iout	200 mA
V_{REF} Iout	0.0 mA
UP, VMx, PGTMR, TDLY, INIT	GND - 0.3 V to VCC5 +0.3 V
ENx, KILL, DONE (V_{DD} < 5 V)	GND - 0.3 V to GND +12 V
ENx, KILL, DONE (V_{DD} ≥ 5 V)	GND - 0.3 V to GND +16 V
ENx, KILL, DONE sink current	-15 mA
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-ambient (θ_{JA})	73°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JC})	3°C/W 4/

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
V_{DD} supply voltage	3.3 V ±10 % to 12 V ±10 %
Timer delay resistors	10 kΩ to 100 kΩ
V_{DD} capacitor	≥ 100 nF
V_{REF} capacitor	220 nF ±20%
VCC5 capacitor	470 nF ±20%

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Tested in a heavy ion environment at LET = 86 MeV/(cm^2/mg) at +125°C (T_C) for SEB. Refer to manufacturer single event effects test report for more information.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer for more information.

4/ For θ_{JC}, the case temperature location is the center of the package underside.

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) :
Device type 01 .... 100 krad(Si) 5/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s) :
Device types 01 and 02 .... 50 krad(Si) 5/ 6/

Single event phenomena (SEP) :

No single event latchup (SEL) occurs at effective (LET) (see 4.4.4.3) .... ≤ 86 MeV/(cm^2/mg) 7/
No single event burn out (SEB) occurs at surface LET (see 4.4.4.3) .... ≤ 86 MeV/(cm^2/mg) 7/
No single event transient (SET) or single event functional interrupt (SEFI) occurs
at surface LET (see 4.4.4.3) .... ≤ 20 MeV/(cm^2/mg) 8/

Single event transient (SET) or Single event functional interrupt (SEFI) observed at
surface LET (see 4.4.4.3) (fluence = 1 x 10^7 ion/cm^2 with V_{DD} = 3 V with saturated
x-section = 1.06 x 10^{-5} cm^2) .... ≤ 86 MeV/(cm^2/mg) 8/

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5/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) of 100 krad(Si), and condition D to a maximum total ionizing dose (TID) of 75 krad(Si). The devices are marked at the high dose rate condition A to a TID level 100 krad(Si).

6/ Device type 02 has been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device type 02 are wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) TID level.

7/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

8/ During SET/SEFI test, manufacturer used copper (Cu) ion beam at surface LET= 20 MeV/(cm^2/mg), fluence = 1 x 10^7 ion/cm^2 and V_{DD} = 3 V, and observed no SET or SEFI event with less than cross section 2.5 x 10^{-8} cm^2. However, using gold (Au) ion beam at fluence = 1 x 10^7 ion/cm^2 and V_{DD} = 3 V at surface LET = 86 MeV(mg/cm^2), and observed SET and SEFI with a saturated x-section = 1.06 x 10^{-5} cm^2.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC JEP 163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C		Group A subgroups	Device type	Limits		Unit
						Min	Max	
V_{DD} power supply								
3 V quiescent supply current	IDDQ_3	V_{DD} = 3 V, UP and INIT = 0.5 V		1,2,3	01, 02		6	mA
			M, D, P, L, R	1 2/			6	
13.2 V quiescent supply current	IDDQ_13	V_{DD} = 13.2 V, UP and INIT = 0.5 V		1,2,3	01, 02		8	mA
			M, D, P, L, R	1 2/			8	
3 V operating supply current	IDD_3	V_{DD} = 3 V, UP and INIT = 0.7 V, EN tied to VM to 5 V		1,2,3	01, 02		6	mA
			M, D, P, L, R	1 2/			6	
13.2 V operating supply current	IDD_13	V_{DD} = 13.2 V, UP and INIT = 0.7 V, EN tied to VM to 5 V		1,2,3	01, 02		8	mA
			M, D, P, L, R	1 2/			8	
Rising undervoltage lockout	UVLO	V_{DD} rising to V_{REF} rising, VCC5 = 45 mA		1,2,3	01, 02	2.8	2.95	V
			M, D, P, L, R	1 2/		2.8	2.95	
Undervoltage lockout hysteresis	UVLO hys	UVLO - V_{DD} falling to V_{REF}		1,2,3	01, 02	30	100	mV
		turn-off	M, D, P, L, R	1 2/		30	100	
Time from V_{DD} to inputs being active	t_{VDD_INPUT}	V_{DD} rising to inputs active, t_{DLY} timer disabled		9.10.11	01, 02		3	ms
			M, D, P, L, R	9 2/			3	
VCC5 linear regulator								
Output voltage	VCC5	V_{DD} = 13.2 V, I_{LOAD} = 45 mA		1, 2, 3	01, 02	4.5	5.5	V
			M, D, P, L, R	1 2/		4.5	5.5	
VCC5 current limit	I_{LIM}			1, 2, 3	01, 02	50	200	mA
			M, D, P, L, R	1 2/		50	200	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Reference voltage								
Reference voltage	V_{REF}			1, 2, 3	01, 02	594	606	mV
			M, D, P, L, R	1 2/		594	606	
INIT, UP, VM1, VM2, VM3,VM4 comparator inputs								
Comparator rising threshold voltage	V_{TH}			1, 2, 3	01, 02	591	609	mV
			M, D, P, L, R	1 2/		591	609	
Comparator input leakage current	I_{LK}	$V_{UP} = V_{VMx} = 0.5$ V		1, 2, 3	01, 02	-50	50	nA
			M, D, P, L, R	1 2/		-50	50	
Hysteresis current	I_{HYS}	$V_{UP} = V_{VMx} = 0.7$ V		1, 2, 3	01, 02	-28	-20	μA
			M, D, P, L, R	1 2/		-28	-20	
Timer disabled delay time from VM, UP, INIT input to EN output	$DISt_{VM_EN\ dly}$	t_{DLY} = VCC5 rising VM > VM_{VTH} to EN rising start		9,10,11	01, 02	1.5	4.5	μs
			M, D, P, L, R	9 2/		1.5	4.5	
EN1, EN2, EN3, EN4 Outputs								
Drive (sink) current	I_{ENS}	$V_{DD} = 3.0$ V, $V_{ENx} = 0.4$V		1, 2, 3	01, 02	8		mA
			M, D, P, L, R	1 2/		8		
Leakage current	I_{ENLK}	$V_{DD} = V_{ENx} = 13.2$ V		1, 2, 3	01, 02		0.3	μA
			M, D, P, L, R	1 2/			0.3	
DONE input/output								
Drive (sink) current	I_{DNS}	$V_{DD} = 3.0$ V, $V_{DONE} = 0.4$ V		1, 2, 3	01, 02	8		mA
			M, D, P, L, R	1 2/		8		
Leakage current	I_{DNLK}	$V_{DD} = V_{DONE} = 13.2$ V		1, 2, 3	01, 02		5	μA
			M, D, P, L, R	1 2/			5	
Input Vth for 'LOW'	V_{IL}			1, 2, 3	01, 02	0.8		V
			M, D, P, L, R	1 2/		0.8		
Input Vth for 'HIGH'	V_{IH}			1, 2, 3	01, 02		1.4	V
			M, D, P, L, R	1 2/			1.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Delay and power good timer								
10 kΩ delay timer	t_{DLY_10}	t_{DLY} resistor = 10 kΩ		9,10,11	01, 02	1.8	2.2	ms
			M, D, P, L, R	9 2/		1.8	2.2	
100 kΩ delay timer	t_{DLY_100}	t_{DLY} resistor = 100 kΩ		9,10,11	01, 02	18	22	ms
			M, D, P, L, R	9 2/		18	22	
10 kΩ power good timer	t_{PG_10}	PGTMR resistor = 10 kΩ		9,10,11	01, 02	3.6	4.4	ms
			M, D, P, L, R	9 2/		3.6	4.4	
100 kΩ power good timer	t_{PG_100}	PGTMR resistor = 100 kΩ		9,10,11	01, 02	36	44	ms
			M, D, P, L, R	9 2/		36	44	
KILL input/output								
Drive (sink) current	I_{KS}	V_{DD} = 3.0 V, V_{KILL} = 0.4 V		1, 2, 3	01, 02	7		mA
			M, D, P, L, R	1 2/		7		
Leakage current	I_{KLK}	V_{DD} = V_{KILL} = 13.2 V		1, 2, 3	01, 02		5	μA
			M, D, P, L, R	1 2/			5	
Input Vth for 'LOW'	V_{IL}	V_{DD} = 3.0 V		1, 2, 3	01, 02	0.8		V
			M, D, P, L, R	1 2/		0.8		
Input Vth for 'HIGH'	V_{IH}	V_{DD} = 3.0 V		1, 2, 3	01, 02		1.4	V
			M, D, P, L, R	1 2/			1.4	
Minimum time to trigger a KILL input	t_{KON}			9,10,11	01, 02		1.4	μs
			M, D, P, L, R	9 2/			1.4	
Delay from KILL low to all EN low	t_{KDLY}			9,10,11	01, 02		1.6	μs
			M, D, P, L, R	9 2/			1.6	
VM < 0.591 V to KILL low	t_{KRESP}			9,10,11	01, 02		1.6	μs
			M, D, P, L, R	9 2/			1.6	

1/ Unless otherwise specified, V_{DD} = 3 V to 13.2 V.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein). RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 02 is only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krad(Si). Device type 02 is wafer acceptance tested 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D and are marked at the standard 50 krad(Si) level.
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Linear energy transfer (LET)
01 02	No SEL occurs	125°C	Normal Incidence LET ≤ 86 MeV/(cm^2/mg) 3/ 4/
	No SEB occurs	125°C	Normal Incidence LET ≤ 86 MeV/(cm^2/mg) 3/ 4/
	SET, SEFI free	25°C	Normal Incidence LET ≤ 20 MeV/(cm^2/mg) 5/

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(cm^2/mg).
4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.
5/ During SET/SEFI test, manufacturer used copper (Cu) ion beam at surface LET= 20 MeV(cm^2/mg), fluence = 1 x 10^7 ion/cm^2 with V_{DD} = 3 V, and observed no SET or SEFI event with less than cross section 2.5 x10^{-8} cm^2. However, using gold (Au) ion beam at fluence = 1 x 10^7 ion/cm^2 and V_{DD} = 3 V at surface LET = 86 MeV(cm^2/mg), and observed SET and SEFI with a saturated x-section = 1.06 x 10^{-5} cm^2.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535 and JEDEC JEP163. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For static burn-in I, all inputs shall be connected to GND or low.

c. For static burn-in II, all inputs shall be connected to high through resistors to the supply voltage (V_{CC}).

d. Unless otherwise specified in the QM plan, for devices class V dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

e. For devices class V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

Case X

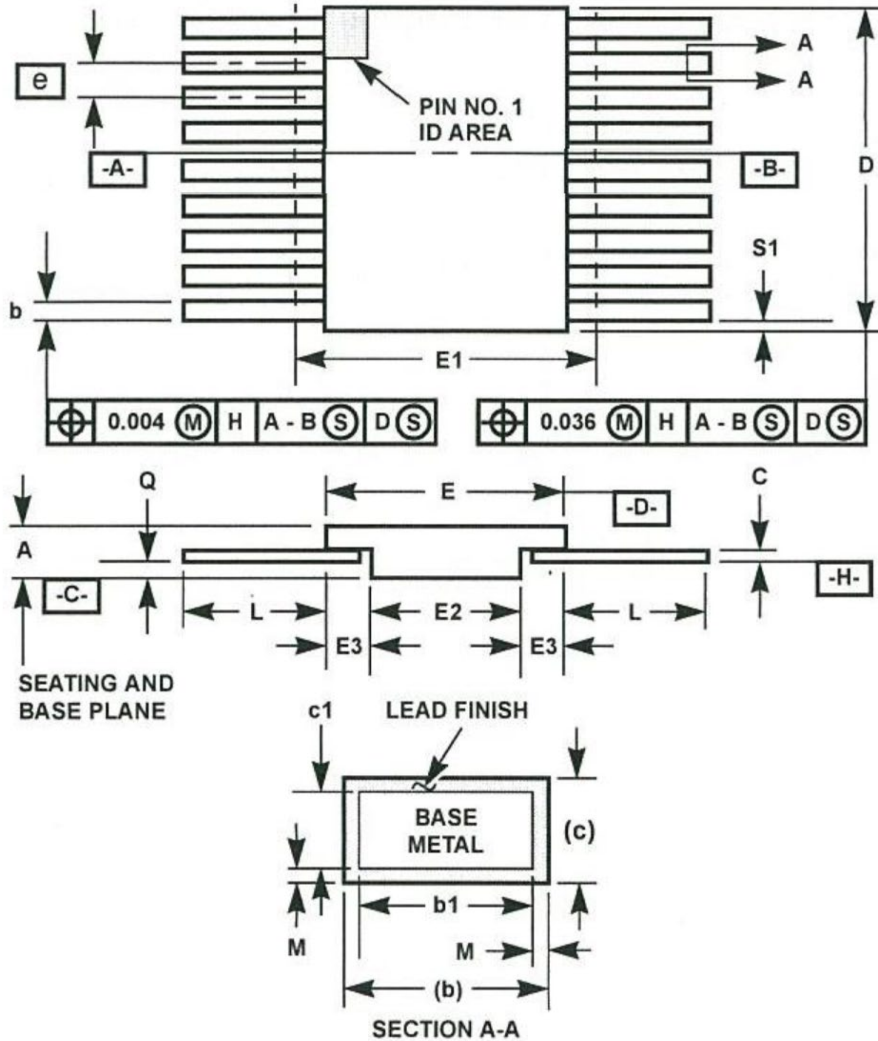


FIGURE 1. Case outline.

Case outline X - continued

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.045	.115	1.14	2.92	---
b	.015	.022	0.38	0.56	---
b1	.015	.019	0.38	0.48	---
c	.004	.009	0.10	0.23	---
c1	.004	.006	0.10	0.15	---
D	.430	.450	10.92	11.43	3
E	.320	.340	8.13	8.64	---
E1	---	.360	---	9.14	3
E2	.220	.240	5.59	6.10	---
E3	.030	---	0.76	---	7
e	.050 BSC		1.27 BSC		---
k	.008	.015	0.20	0.38	2
L	.280	.320	7.11	8.13	---
M	---	.0015	---	0.04	---
Q	.026	.045	0.66	1.14	8
S1	.000	---	0.00	---	---
N	18				

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by .0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
9. Controlling dimensions are inch, millimeter dimensions are given for reference only.

FIGURE 1. Case outline - continued.

Device types	01, 02
Case outline	X
Terminal number	Terminal symbol
1	VDD
2	UP
3	VM1
4	VM2
5	VM3
6	VM4
7	INIT
8	PGTMR
9	TDLY
10	GND
11	$\overline{\text{KILL}}$
12	DONE
13	EN4
14	EN3
15	EN2
16	EN1
17	VREF
18	VCC5
Package lid	Tied internally to terminal 10 (GND)

FIGURE 2. Terminal connections.

Terminal number	Description
V_{DD}	This is the supply for internal linear regulator of the device. The supply to V_{DD} should be locally bypassed using at least a 0.1 μF ceramic capacitor.
UP	This pin commands the device to sequence the power supplies up or down. This pin has an identical type structure as the VMX pins. This pin can be driven by a system controller or be used to sense a non sequenced power supply voltage to start the power up sequence.
VM1	These pins are the voltage monitor inputs. This is a comparator type input with a rising threshold of 600 mV and programmable hysteresis through current IHYS. Connect this pin to an external resistor divider between each sequenced power supply and GND. During power up sequencing, driving this pin above 600 mV indicates that the sequenced power supply has reached the desired power on voltage. During power down sequencing, a voltage below 600 mV indicates that the sequenced power supply has reached the desired power off voltage.
VM2	
VM3	
VM4	
INIT	Sequence INITIATE pin. When using the device in a standalone or the first in a cascade configuration connect this pin to UP. When not the first integrated circuit (IC) in a cascade configuration, this input is driven by DONE of the previous device. This pin has an identical type structure as the VMX pins. See Supplier Application Information for more information on this pin's configuration in cascaded applications.
PGTMR	A resistor connected between PGTMR to GND sets the time allowed for a power supply to reach a power good state after being enabled with ENx. Power Good timer is adjusted from 4 ms to 40 ms by a 10 kΩ to 100 kΩ resistor. Connect this pin to VCC5 to disable the power good timer.
TDLY	A resistor connected between TDLY and GND sets the rising and falling time delay between a supply ON/OFF signal (UP or VMx) and the enabling or disabling of (ENx) the next power supply in the sequence. Delay timer can be adjusted from 2 ms to 20 ms by a 10 kΩ to 100 kΩ resistor. Connect this pin to VCC5 if no assured delay is required between supplies being sequenced on or off.
GND	Connect this pin to the printed circuit board (PCB) ground plane.
$\overline{\text{KILL}}$	Open drain output indicating a fault condition. Disable all outputs simultaneously by pulling $\overline{\text{KILL}}$ low. After a fault clear, $\overline{\text{KILL}}$ must be high before subsequent UP driven high.
DONE	Open drain indicator that device has successfully sequenced on or off all the power supplies.
EN1	These pins are open drain outputs. Use an external pull-up resistor and connect to the enable pin of each power supply being sequenced.
EN2	
EN2	
EN4	
V_{REF}	Output of the internal 600 mV reference voltage. Bypass this pin to the PCB ground plane with a 0.22 μF ceramic capacitor located as close as possible to the pin.
VCC5	Output of the internal linear regulator and provides bias to all internal circuitry. Locally filter this pin to GND using a 0.1 μF ceramic capacitor as close as possible to the pin.
Package lid	Tied internally to terminal 10 (GND).

FIGURE 2. Terminal connections - continued.

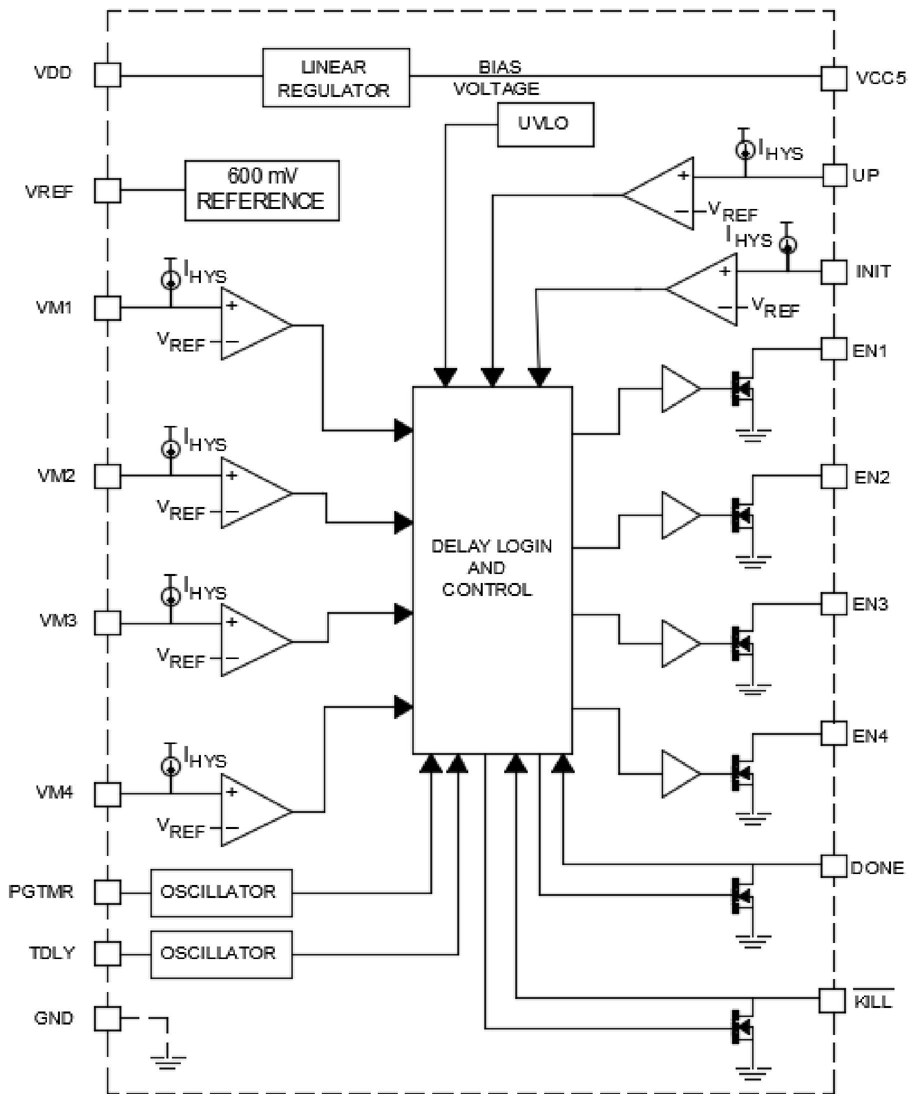


FIGURE 3. Functional block diagram.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Static burn-in (see 4.2.1) 3/ 4/	Not required	Required
Interim electrical parameters (see 4.2)	Not required	1, 9 1/ 2/
Dynamic burn-in (see 4.2.1) 3/ 5/	Required	Required
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1 ,2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and delta.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).
3/ The burn-in configuration, either static or dynamic burn-in test shall be performed per method 1015 with test condition A or B or C or D (see MIL-PRF-38535 and JEDEC JEP163)
4/ For device class V and Y (class level S): If the device operates in a static mode, then static burn-in I and/or II test shall be performed per method 1015 with test condition A or C (see MIL-PRF-38535 and JEDEC JEP163).
5/ For device class V and Y (class level S): If the device operates in a dynamic mode, then dynamic burn-in test shall be performed per method 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
+13.2 V Operating supply current	IDD_13	UP and INIT = 0.7 V, with EN and VM tied to 5 V	±500 uA
Output voltage	VCC5	V_{DD} = +13.2V I_{LOAD} = 45 mA	±250 mV
Reference voltage	V_{REF}		±3 mV
Comparator input leakage current	I_{LK}	$V_{up} = V_{vmx}$ = 0.5 V, measure UP, INIT, VM_X	±5 nA
Comparator rising threshold voltage	V_{th}	Measure UP, INIT, VM_X	±4.5 mV

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall be corresponding to the test defined in TABLE IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

c. Single event burn-out (SEB) observances.

d. Single event transient (SET) observances.

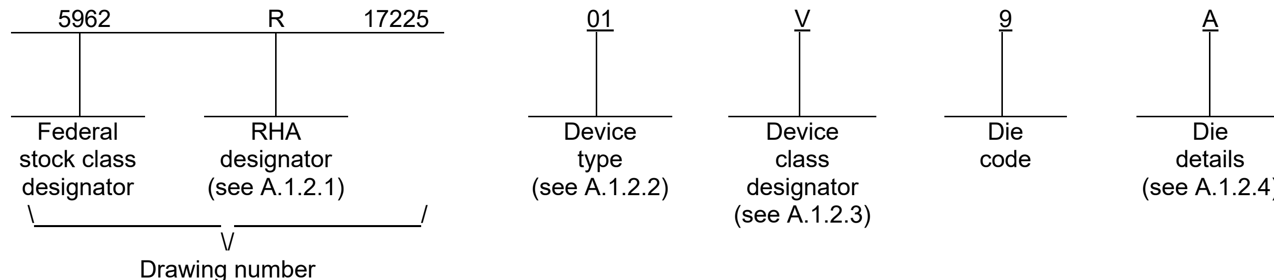
e. Single event functional interrupt (SEFI) observances.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-17225

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70321SEH	Radiation hardened, quad power supply sequencer
02	ISL73321SEH	Radiation hardened, quad power supply sequencer

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

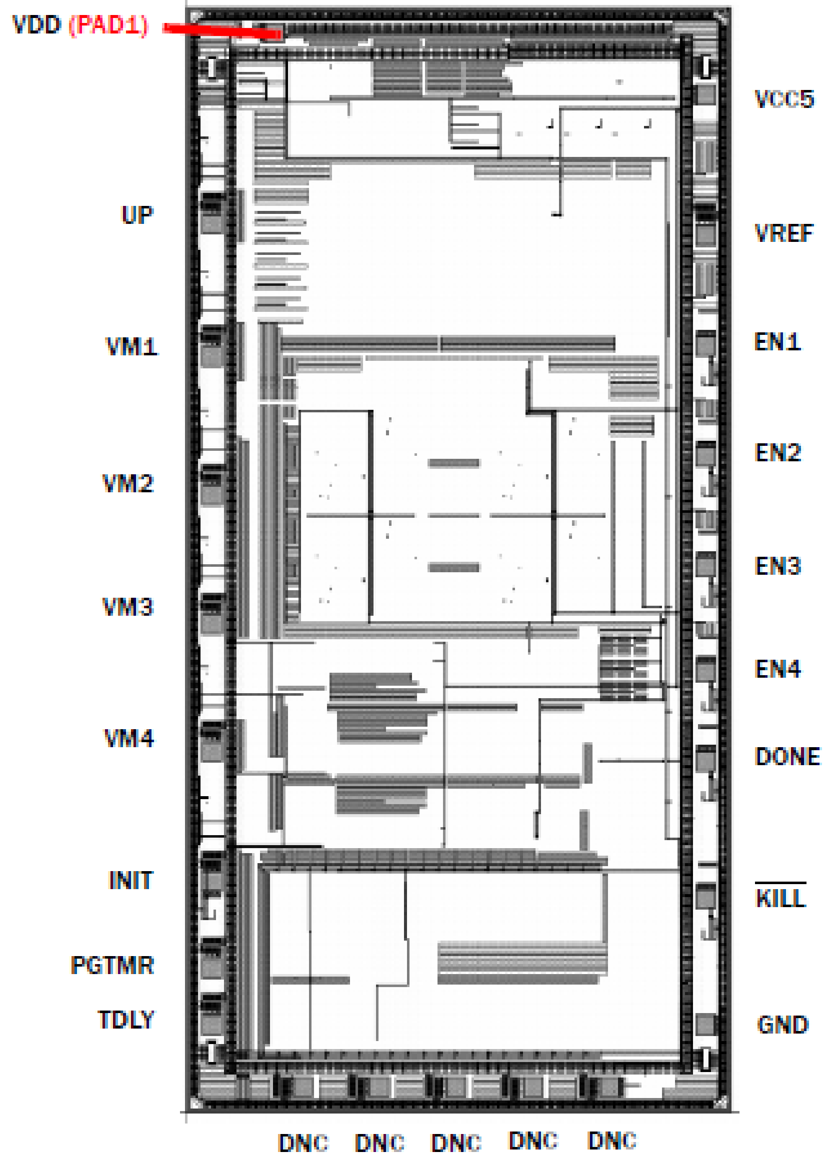


FIGURE A-1. Die bonding pad locations and electrical functions.

Pad Name	Pad Number	X (µm)	Y (µm)	dX (µm)	dY (µm)
V_{DD}	1	0	0	110	110
UP	2	-368	-1123.4	110	110
VM1	3	-368	-1900.8	110	110
VM2	4	-368	-2717.95	110	110
VM3	5	-368	-3476.25	110	110
VM4	6	-368	-4225.43	110	110
INIT	7	-368	-4987.95	110	110
PGTMR	8	-368	-5497.85	110	110
TDLY	9	-368	-5830	110	110
GND	10	2526	-5830	110	110
KILL	11	2526	-5088.8	110	110
DONE	12	2526	-4279.45	110	110
EN4	13	2526	-3754.45	110	110
EN3	14	2526	-3138.8	110	110
EN2	15	2526	-2488.8	110	110
EN1	16	2526	-1838.8	110	110
VREF	17	2526	-1188.8	110	110
V_{CC}	18	2526	-364	110	110

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size: 3300 μm x 6600 μm (130 mils x 260 mils)
Die thickness: 483 μm ± 25.4 μm (19 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5% / 0.5%)
Thickness: 2.7 μm ± 0.4 μm

Backside finish.
Silicon

Glassivation.
Type: Silicon oxide and silicon nitride
Thickness: 0.3 μm ± 0.03 μm to 1.2 μm ± 0.12 μm

Process.
0.6 μm BiCMOS junction isolated

Assembly related information.
Substrate potential: GND
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-09

Approved sources of supply for SMD 5962-17225 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1722501VXC	34371	ISL70321SEHVF
5962R1722501V9A	34371	ISL70321SEHVX
5962L1722502VXC	34371	ISL73321SEHVF
5962L1722502V9A	34371	ISL73321SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.