REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraph 4.4.4.1.1 Accelerated annealing test and make change to paragraph A.4.3.1. - ro	16-05-03	C. SAFFLE
B	Update drawing to latest MIL-PRF-38535 requirements. - jt	16-05-03	C. SAFFLE
C	Make change to the $I_{OUT(OFF)}$ subgroup 2 maximum limit with conditions of V_{IN} = 5.0 V and V_{OUT} = 0.5 V by deleting 0 nA and replacing with 30 nA as specified under Table IA. Make change to the $I_{OUT(ON)}$ subgroup 2 maximum limit with conditions of V_{IN} = V_{OUT} = 0.5 V by deleting 0 nA and replacing with 30 nA as specified under Table IA. - ro	22-12-05	J. ESCHMEYER

Revision Status of Sheets

REV	C	C	C	C	C	C	C	C	C	C	C	C										
SHEET	23	24	25	26	27	28	29	30	31	32	33	34										
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

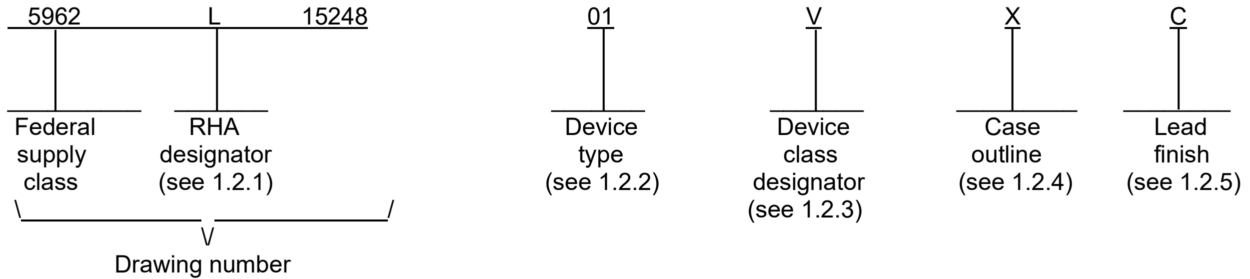
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RODNEY D. CHAMBERS CHECKED BY RAJESH PITHADIA APPROVED BY CHARLES F. SAFFLE DRAWING APPROVAL DATE 16-03-14	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime** MICROCIRCUIT, DIGITAL-LINEAR, BiCMOS, SINGLE 32-CHANNEL ANALOG MUX WITH OVERVOLTAGE PROTECTION, MONOLITHIC SILICON		
AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **67268**	**5962-15248**
		SHEET 1 OF 34		

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL71831SEH	Radiation hardened, dielectrically isolated (DI), BICMOS, single 32-channel analog MUX with high impedance analog Input overvoltage protection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Quad flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage between V_S and GND	7 V
V_{REF} to GND	7 V
Digital input overvoltage range	V_{REF} to GND
Maximum current through a selected switch	10 mA
Analog input overvoltage range (power on/off)	-0.4 V to 7 V
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-case (θ_{JC})	4°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	48°C/W

1.4 Recommended operating conditions.

Supply voltage (V_S)	3.0 V to 5.5 V
V_{REF}	3.0 V to 5.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available: low dose rate tests - dose rate ≤ 10 mrad(Si)/s:	50 krad(Si) 2/
Single event phenomena (SEP):	
No SEL occurs at effective linear energy threshold (LET)	60 MeV/(mg/cm^2) 3/ 4/
No SEB occurs at effective linear energy threshold (LET)	60 MeV/(mg/cm^2) 4/
Single event transients (SET) observed at an effective LET (see 4.4.4.3) (SET magnitude of ±20 mV at a cross section 3.1 X 10^{-5}cm^2)	≤ 60 MeV/(mg/cm^2) 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Device type 01 has been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krads(Si). Device type 01 is wafer acceptance tested to 75 krads(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krads(Si) level.

3/ Device type 01 use silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Pr ions at normal incidence, corresponding to a surface LET of 60 MeV/(mg/cm^2). The normal particle range into silicon for Pr ions after 30 mm of air is about 118 μm and the Bragg peak range is 53 μm, resulting in ion penetration well beyond the sensitive volume of the devices.

4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C V_S = 5 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Channel on resistance	R_{ON}	V_S = 4.5 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1, 2, 3	01		120	Ω
		M, D, P, L, V_S = 4.5 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1 3/			120	
R_{ON} match between channels	ΔR_{ON}	V_S = 4.5 V, V_{IN} = 0 V, 2.25 V, 4.5 V, I_{OUT} = 1 mA	1, 2, 3	01		5	Ω
		M, D, P, L, V_S = 4.5 V, V_{IN} = 0 V, 2.25 V, 4.5 V, I_{OUT} = 1 mA	1 3/			5	
R_{ON} flatness	ΔR_{ON-FL}	V_S = 4.5 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1, 2, 3	01		40	Ω
		M, D, P, L, V_S = 4.5 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1 3/			40	
Switch input off leakage	$I_{IN(OFF)}$	V_S = 5.5 V, V_{IN} = 5 V, all unused inputs and output equal = 0.5 V, see figure 5 2/	1, 2, 3	01	-30	30	nA
		M, D, P, L, V_S = 5.5 V, V_{IN} = 5 V, all unused inputs and output equal = 0.5 V, see figure 5 2/	1 3/		-30	30	
		V_S = 5.5 V, V_{IN} = 0.5 V, all unused inputs and output equal = 5 V, see figure 5 2/	1, 2, 3		-30	30	nA
		M, D, P, L, V_S = 5.5 V, V_{IN} = 0.5 V, all unused inputs and output equal = 5 V, see figure 5 2/	1 3/		-30	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = 5$ V, $V_{REF} = 3.3$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Switch input off over voltage	$I_{IN(OFF-OV)}$	$V_S = 5.5$ V, $V_{IN} = +7$ V, $V_{OUT} = 0$ V, unused inputs = 0 V, see figure 5	1, 3	01	-30	30	nA
			2		-30	120	
		M, D, P, L, $V_S = 5.5$ V, $V_{IN} = +7$ V, $V_{OUT} = 0$ V, unused inputs = 0 V, see figure 5	1 3/		-30	30	
Switch off leakage into the input of an unselected channel with supplies grounded	$I_{IN(PWR-OFF)}$	$V_{IN} = +7$ V, $V_{REF} = V_{EN} = V_A = \pm V_S = 0$ V, unused inputs = 0 V, see figure 5	1, 3	01	-20	20	nA
			2		-20	100	
		M, D, P, L $V_{IN} = +7$ V, $V_{REF} = V_{EN} = V_A = \pm V_S = 0$ V, unused inputs = 0 V, see figure 5	1 3/		-20	20	
Switch off leakage into the input of an unselected channel with supplies open	$I_{IN(PWR-OFF)}$	$V_{IN} = +7$ V, $V_{REF} = V_{EN} = V_A = \pm V_S = 0$ V, unused inputs = 0 V, see figure 5	1, 3	01	-20	20	nA
			2		-20	100	
		M, D, P, L, $V_{IN} = +7$ V, $V_{REF} = V_{EN} = V_A = \pm V_S = 0$ V, unused inputs = 0 V, see figure 5	1 3/		-20	20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C V_S = 5 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switch on leakage into the input of a selected channel (over voltage)	$I_{IN(ON-OV)}$	V_S = 5.5 V, V_{IN} = +7 V, V_{OUT} = OPEN, unused inputs = 0 V, see figure 5	1, 2, 3	01	2.75	5.5	µA
		M, D, P, L, V_S = 5.5 V, V_{IN} = +7 V, V_{OUT} = OPEN, unused inputs = 0 V, see figure 5	1 3/		2.75	5.5	
Switch off leakage into the output with the part disabled	$I_{OUT(OFF)}$	V_S = 5.5 V, V_{IN} = 0.5 V, V_{OUT} = 5.0 V, see figure 5 2/	1, 3	01	-30	30	nA
			2		0	200	
		M, D, P, L, V_S = 5.5 V, V_{IN} = 0.5 V, V_{OUT} = 5.0 V, see figure 5 2/	1 3/		-30	30	
		V_S = 5.5 V, V_{IN} = 5.0 V, V_{OUT} = 0.5 V, see figure 5 2/	1, 3		-30	30	
			2		-60	30	
		M, D, P, L, V_S = 5.5 V, V_{IN} = 5.0 V, V_{OUT} = 0.5 V, see figure 5 2/	1 3/		-30	30	
Switch on leakage into the input/output for a selected switch	$I_{OUT(ON)}$	V_S = 5.5 V, V_{IN} = V_{OUT} = 5.0 V, unused inputs = 0.5 V, see figure 5 2/	1, 3	01	-30	30	nA
			2		0	200	
		M, D, P, L, V_S = 5.5 V, V_{IN} = V_{OUT} = 5.0 V, unused inputs = 0.5 V, see figure 5 2/	1 3/		-30	30	
		V_S = 5.5 V, V_{IN} = V_{OUT} = 0.5 V, unused inputs = 5.0 V, see figure 5 2/	1, 3		-30	30	
			2		-60	30	
		M, D, P, L, V_S = 5.5 V, V_{IN} = V_{OUT} = 0.5 V, unused inputs = 5.0 V, see figure 5 2/	1 3/		-30	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ V_S = 5 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic input high/low voltage level	V_{IH}/V_{IL}	V_S = 5.5 V, V_{REF} = 3.3 V	1, 2, 3	01	1.3	1.6	V
		M, D, P, L, V_S = 5.5 V, V_{REF} = 3.3 V	1 3/		1.3	1.6	
Input current Into V_A and V_{EN}	I_{IH}/I_{IL}	V_S = 5.5 V, V_{REF} = V_{EN} = V_A = 3.3 V	1, 2, 3	01	-100	100	nA
		M, D, P, L, V_S = 5.5 V, V_{REF} = V_{EN} = V_A = 3.3 V	1 3/		-100	100	
Quiescent supply current	I_{SUPPLY}	V_S = V_{REF} = V_{EN} = 5.5 V, V_A = 0 V 2/	1,3	01		100	nA
			2			500	
		M, D, P, L, V_S = V_{REF} = V_{EN} = 5.5 V, V_A = 0 V 2/	1 3/			300	
Supply current in V_{REF}	I_{REF}	V_S = V_{REF} = V_{EN} = 5.5 V, V_A = 0 V 2/	1, 2, 3	01		200	nA
		M, D, P, L, V_S = V_{REF} = V_{EN} = 5.5 V, V_A = 0 V 2/	1 3/			200	
Capacitance: channel input	$C_{IN(OFF)}$	$+V_S$ = $-V_S$ = 0 V, f = 1 MHz, T_A = +25°C, see 4.4.1c	4	01		5	pF
Capacitance: channel output	$C_{OUT(OFF)}$	$+V_S$ = $-V_S$ = 0 V, f = 1 MHz, T_A = +25°C, see 4.4.1c	4	01		25	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_S = 5 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Off isolation	V_{ISO}	V_{EN} = V_{REF}, f = 1 kHz, R_L = OPEN, V_S = 1 V_{RMS}, T_A = +25°C, see 4.4.1c	4	01	60		dB
Crosstalk rejection	V_{CT}	V_{EN} = 0.8 V, f = 1 kHz, R_L = OPEN, V_S = 1 V_{RMS}, T_A = +25°C, see 4.4.1c	4	01	73		dB
Charge injection	V_{CTE}	C_L = 100 pF, V_{IN} = 0 V, see 4.4.1c	4	01		5	pC
Functional test		See 4.4.1d	7,8 A, 8B	01			
Transition time from address inputs to output	t_{TRANS}	C_L = 50 pF, R_L = 10 kΩ, V_S = 4.5 V	9, 10,11	01	10	70	ns
		M, D, P, L, C_L = 50 pF, R_L = 10 kΩ, V_S = 4.5 V	9 3/		10	70	
Break-before-make time delay	t_{BBM}	C_L = 50 pF, R_L = 100 Ω, V_S = 4.5 V, see figure 6	9, 10,11	01	5	40	ns
		M, D, P, L, C_L = 50 pF, R_L = 100 Ω, V_S = 4.5 V, see figure 6	9 3/		5	40	
Propagation delay time enable to I/O channels	$t_{ON(EN)}$	C_L = 50 pF, R_L = 1 kΩ, V_S = 4.5 V	9, 10,11	01		40	ns
		M, D, P, L, C_L = 50 pF, R_L = 1 kΩ, V_S = 4.5 V	9 3/			40	
Propagation delay time disable to I/O channels	$t_{OFF(EN)}$	C_L = 50 pF, R_L = 1 kΩ, V_S = 4.5 V	9, 10,11	01		50	ns
		M, D, P, L, C_L = 50 pF, R_L = 1 kΩ, V_S = 4.5 V	9 3/			50	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \le T_A \le +125°C$ V_S = 3.3 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Channel on resistance	R_{ON}	V_S = 3.0 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1,2,3	01		200	Ω
		M, D, P, L, V_S = 3.0 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1 3/			200	
R_{ON} match between channels	ΔR_{ON}	V_S = 3.0 V, V_{IN} = 0.5 V, 2.5 V, I_{OUT} = 1 mA	1,2,3	01		5	Ω
		M, D, P, L, V_S = 3.0 V, V_{IN} = 0.5 V, 2.5 V, I_{OUT} = 1 mA	1 3/			5	
R_{ON} flatness	ΔR_{ON-FL}	V_S = 3.0 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1,2,3	01		50	Ω
		M, D, P, L, V_S = 3.0 V, V_{IN} = 0 V to V_S, I_{OUT} = 1 mA	1 3/			50	
Switch input off leakage	$I_{IN(OFF)}$	V_S = 3.6 V, V_{IN} = 3.1 V, all unused inputs and output equal = 0.5 V, see figure 5 5/	1, 2, 3	01	-30	30	nA
		M, D, P, L, V_S = 3.6 V, V_{IN} = 3.1 V, all unused inputs and output equal = 0.5 V, see figure 5 5/	1 3/		-30	30	
		V_S = 3.6 V, V_{IN} = 0.5 V, all unused inputs and output equal = 3.1 V, see figure 5 5/	1, 2, 3		-30	30	
		M, D, P, L, V_S = 3.6 V, V_{IN} = 0.5 V, all unused inputs and output equal = 3.1 V, see figure 5 5/	1 3/		-30	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \leq T_A \leq +125°C$ V_S = 3.3 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limit Min	Limit Max	Unit
Switch input off over voltage	$I_{IN(OFF-OV)}$	V_S = 3.6 V, V_{IN} = +7 V, V_{OUT} = 0 V, unused inputs = 0 V, see figure 5	1, 3	01	-30	30	nA
			2		-30	100	
		M, D, P, L, V_S = 3.6 V, V_{IN} = +7 V, V_{OUT} = 0 V, unused inputs = 0 V, see figure 5	1 3/		-30	30	
Switch on leakage into the input of a selected channel (over voltage)	$I_{IN(ON-OV)}$	V_S = 3.6 V, V_{IN} = +7 V, V_{OUT} = OPEN, unused inputs = 0 V, see figure 5	1, 2, 3	01	1.8	3.6	μA
		M, D, P, L, V_S = 3.6 V, V_{IN} = +7 V, V_{OUT} = OPEN, unused inputs = 0 V, see figure 5	1 3/		1.8	3.6	
Switch off leakage into the output with the part disabled	$I_{OUT(OFF)}$	V_S = 3.6 V, V_{IN} = 0.5 V, V_{OUT} = 3.1 V, see figure 5 5/	1, 3	01	-30	30	nA
			2		0	120	
		M, D, P, L, V_S = 3.6 V, V_{IN} = 0.5 V, V_{OUT} = 3.1 V, see figure 5 5/	1 3/		-30	30	
		V_S = 3.6 V, V_{IN} = 3.1 V, V_{OUT} = 0.5 V, see figure 5 5/	1, 3		-30	30	
			2		0	30	
		M, D, P, L, V_S = 3.6 V, V_{IN} = 3.1 V, V_{OUT} = 0.5 V, see figure 5 5/	1 3/		-30	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \leq T_A \leq +125°C$ V_S = 3.3 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Switch on leakage into the input/output for a selected switch	$I_{OUT(ON)}$	V_S = 3.6 V, V_{IN} = V_{OUT} = 3.1 V, unused inputs = 0.5 V, see figure 5 5/	1, 3	01	-30	30	nA
			2		0	120	
		M, D, P, L, V_S = 3.6 V, V_{IN} = V_{OUT} = 3.1 V, unused inputs = 0.5 V, see figure 5 5/	1 3/		-30	30	
		V_S = 3.6 V, V_{IN} = V_{OUT} = 0.5 V, unused inputs = 3.1 V, see figure 5 5/	1, 3		-30	30	
			2		0	30	
		M, D, P, L, V_S = 3.6 V, V_{IN} = V_{OUT} = 0.5 V, unused inputs = 3.1 V, see figure 5 5/	1 3/		-30	30	
Quiescent supply current	I_{SUPPLY}	V_S = V_{REF} = V_{EN} = 3.6 V, V_A = 0 V 5/	1,3	01		100	nA
			2			300	
		M, D, P, L, V_S = V_{REF} = V_{EN} = 3.6 V, V_A = 0 V 5/	1 3/			300	
Supply current in V_{REF}	I_{REF}	V_S = V_{REF} = V_{EN} = 3.6 V, V_A = 0 V 5/	1,2,3	01		200	nA
		M, D, P, L, V_S = V_{REF} = V_{EN} = 3.6 V, V_A = 0 V 5/	1 3/			200	
Functional test		See 4.4.1d	7, 8A, 8B	01			
Transition time from address inputs to output	t_{TRANS}	C_L = 50 pF, R_L = 10 kΩ, V_S = 3.0 V	9, 10,11	01	10	100	ns
		M, D, P, L, C_L = 50 pF, R_L = 10 kΩ, V_S = 3.0 V	9 3/		10	100	
Break-before-make time delay	t_{BBM}	C_L = 50 pF, R_L = 100 Ω, V_S = 3.0 V, see figure 6	9, 10,11	01	5	50	ns
		M, D, P, L, C_L = 50 pF, R_L = 100 Ω, V_S = 3.0 V, see figure 6	9 3/		5	50	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \leq T_A \leq +125°C$ V_S = 3.3 V, V_{REF} = 3.3 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time enable to I/O channels	$t_{ON(EN)}$	C_L = 50 pF, R_L = 1 kΩ, V_S = 3.0 V	9, 10,11	01		60	ns
		M, D, P, L, C_L = 50 pF, R_L = 1 kΩ, V_S = 3.0 V	9 3/			60	
Propagation delay time disable to I/O channels	$t_{OFF(EN)}$	C_L = 50 pF, R_L = 1 kΩ, V_S = 3.0 V	9, 10,11	01		80	ns
		M, D, P, L, C_L = 50 pF, R_L = 1 kΩ, V_S = 3.0 V	9 3/			80	

1/ Unless otherwise specified, V_{AH} (logic level high) = 3.3 V dc, V_{AL} (logic level low) = 0 V dc, V_{EN} = 3.3 V, and V_{REF} = 3.3 V dc. V_S = 5.0 V dc.

2/ V_S = 5.5 V dc. V_{AH} (logic level high) = 3.3 V dc, V_{AL} (logic level low) = 0 V dc and V_{REF} = 3.3 V dc.

3/ RHA device type 01 supplied to this drawing will meet all levels M, D, P and L of irradiation for condition D. However, device type 01 is only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krads(Si). Device type 01 is wafer acceptance tested 75 krads(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krads(Si) level.
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ Unless otherwise specified, V_{AH} (logic level high) = 3.3 V dc, V_{AL} (logic level low) = 0 V dc, V_{EN} = 3.3 V, and V_{REF} = 3.3 V dc. V_S = 3.3 V dc.

5/ V_S = 3.6 V dc. V_{AH} (logic level high) = 3.3 V dc, V_{AL} (logic level low) = 0 V dc and V_{REF} = 3.3 V dc.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	Temperature (T_C)	Effective linear energy transfer (LET)
01	No SEL	125°C	60 MeV/(mg/cm^2) 3/ 4/
	No SEB	125°C	60 MeV/(mg/cm^2) 4/
	SET Observed	25°C	60 MeV/(mg/cm^2) 5/

1/ For SEP test conditions, see 4.4.4.5 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Device type 01 uses silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Pr ions at normal incidence, corresponding to a surface LET of 60 MeV/(mg/cm^2). The normal particle range into silicon for Pr ions after 30 mm of air is about 118 μm and the Bragg peak range is 53 μm, resulting in ion penetration well beyond the sensitive volume of the devices.

4/ SEL and SEB testing was performed at a supply voltage of V_S = 6.3 V, V_{REF} = 6.3 V.

5/ SET testing was performed at supply voltages of V_S = 3.0 V and V_S = 5.5 V. V_{REF} = 3 V for both supplies tested. SET magnitude of ±20 mV at a cross section 3.1 X 10^{-5}cm^2 was observed

Case outline X

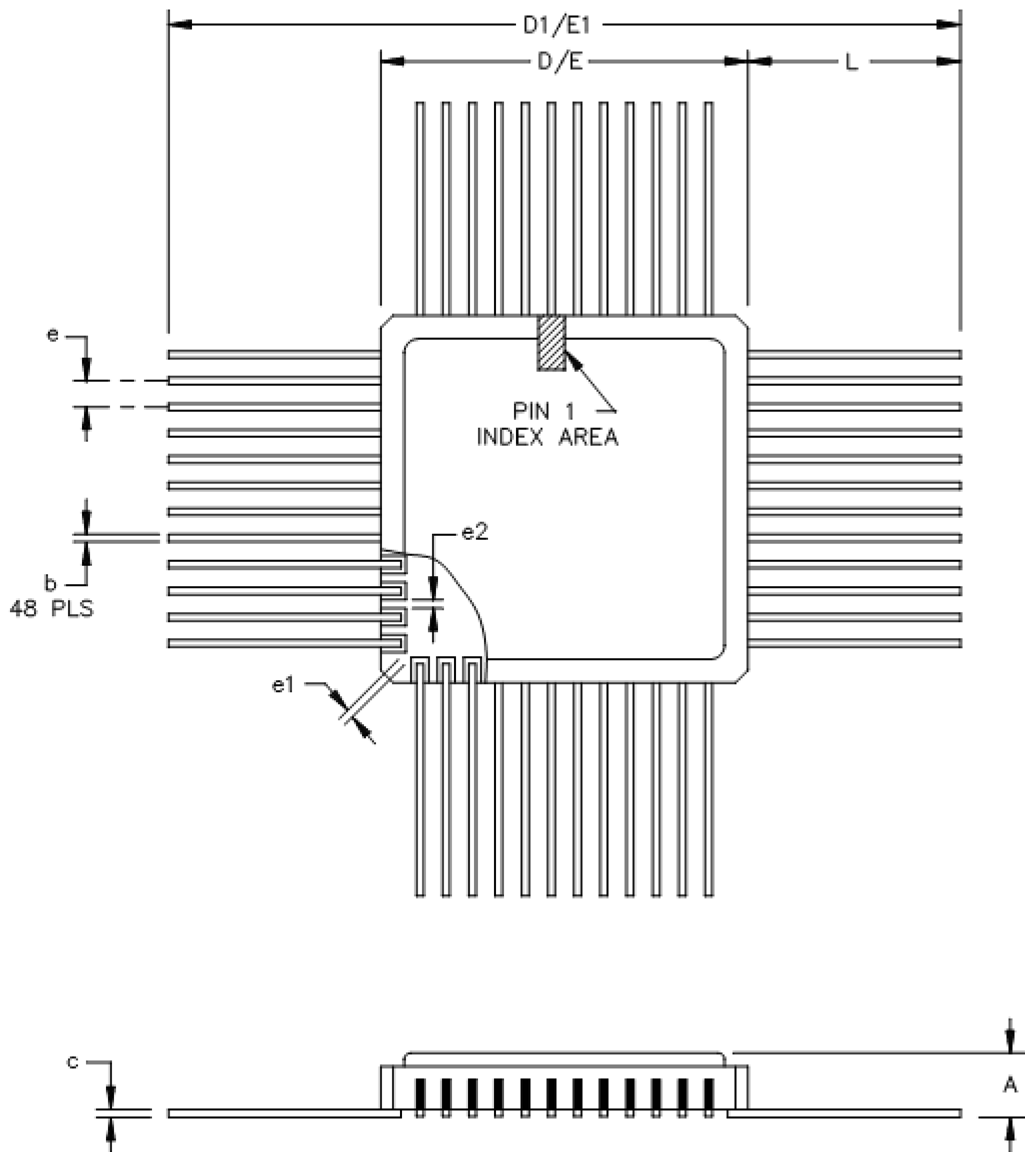


FIGURE 1. Case outline.

Case outline X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.076	0.099	1.93	2.51
b	0.008	0.015	0.20	0.38
C	0.009	0.016	0.23	0.41
D	0.555	0.572	14.10	14.53
D1	1.080	1.118	27.43	28.40
E	0.555	0.572	14.10	14.53
E1	1.080	1.118	27.43	28.40
e	0.040 BSC		1.02 BSC	
e1	0.015	---	0.38	---
e2	0.007	---	0.18	---
L	0.253	0.287	6.43	7.29

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.

FIGURE 1. Case outline - continued.

Device type	01			
Case outline	X			
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	OUT		25	A4
2	NC		26	NC
3	IN 16		27	NC
4	IN 15		28	$\overline{EN}$
5	IN 14		29	GND
6	IN 13		30	NC
7	IN 12		31	IN 17
8	IN 11		32	IN 18
9	IN 10		33	IN 19
10	IN 9		34	IN 20
11	IN 8		35	IN 21
12	IN 7		36	IN 22
13	IN 6		37	IN 23
14	IN 5		38	IN 24
15	IN 4		39	IN 25
16	IN 3		40	IN 26
17	IN 2		41	IN 27
18	IN 1		42	IN 28
19	V_S		43	IN 29
20	V_{REF}		44	IN 30
21	A0		45	IN 31
22	A1		46	IN 32
23	A3		47	NC
24	A3		48	NC
Package Lid	Tied internally to terminal 29 (GND)			

NC = No connection

FIGURE 2. Terminal connections.

Truth table						
A_4	A_3	A_2	A_1	A_0	$\overline{EN}$	On channel
X	X	X	X	X	H	None
L	L	L	L	L	L	1
L	L	L	L	H	L	2
L	L	L	H	L	L	3
L	L	L	H	H	L	4
L	L	H	L	L	L	5
L	L	H	L	H	L	6
L	L	H	H	L	L	7
L	L	H	H	H	L	8
L	H	L	L	L	L	9
L	H	L	L	H	L	10
L	H	L	H	L	L	11
L	H	L	H	H	L	12
L	H	H	L	L	L	13
L	H	H	L	H	L	14
L	H	H	H	L	L	15
L	H	H	H	H	L	16
H	L	L	L	L	L	17
H	L	L	L	H	L	18
H	L	L	H	L	L	19
H	L	L	H	H	L	20
H	L	H	L	L	L	21
H	L	H	L	H	L	22
H	L	H	H	L	L	23
H	L	H	H	H	L	24
H	H	L	L	L	L	25
H	H	L	L	H	L	26
H	H	L	H	L	L	27
H	H	L	H	H	L	28
H	H	H	L	L	L	29
H	H	H	L	H	L	30
H	H	H	H	L	L	31
H	H	H	H	H	L	32

FIGURE 3. Truth table.

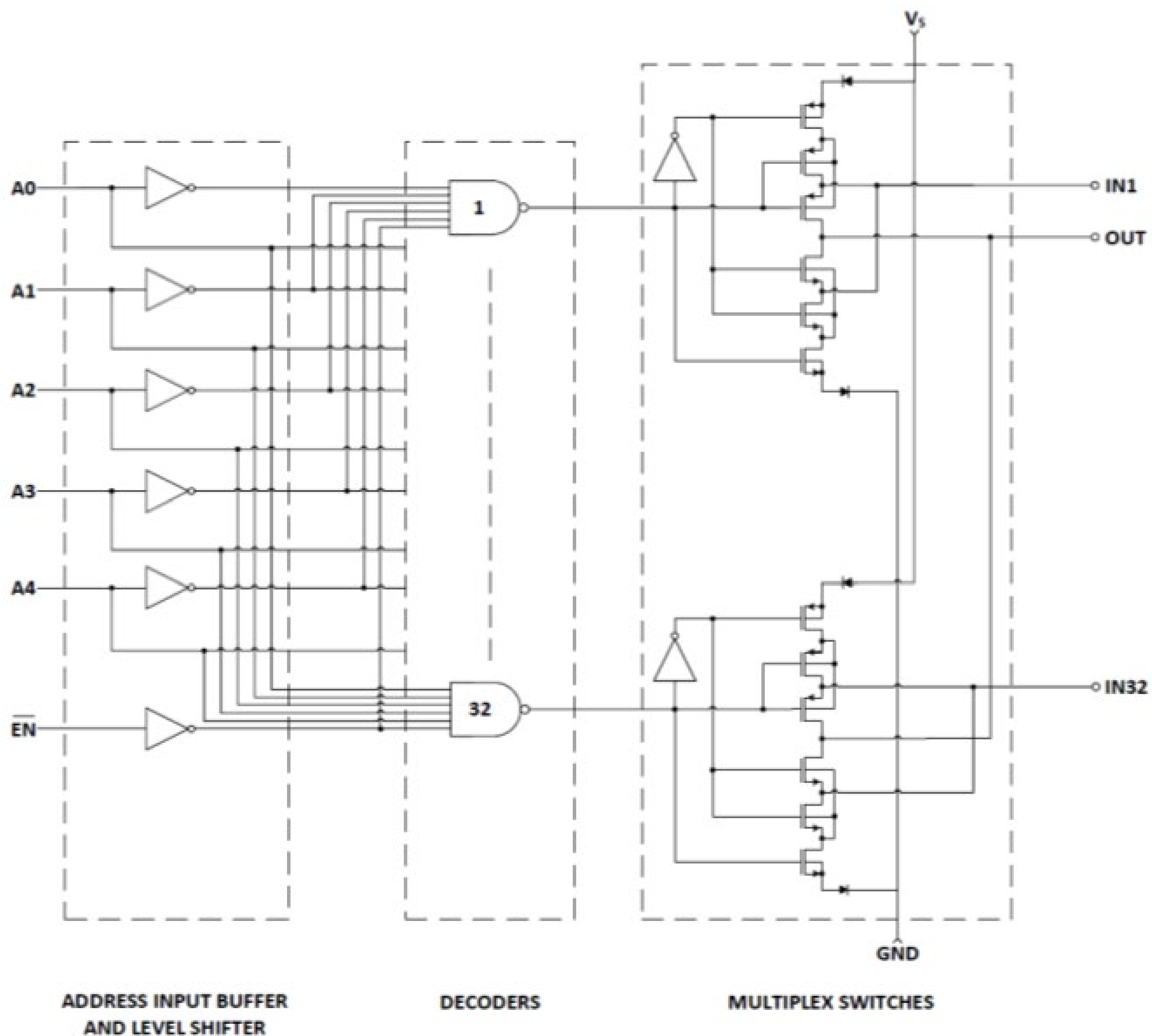
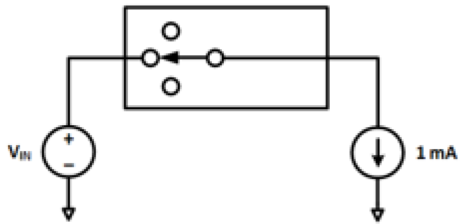
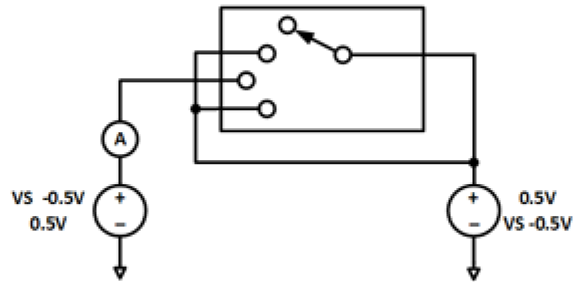
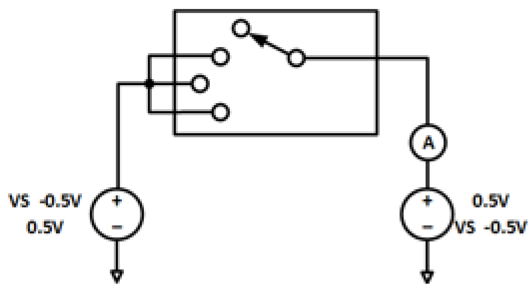
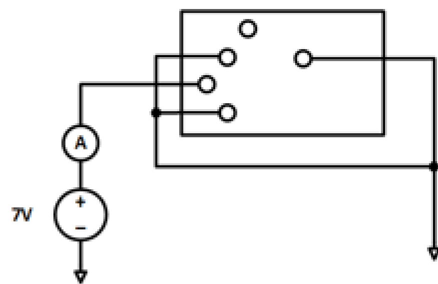


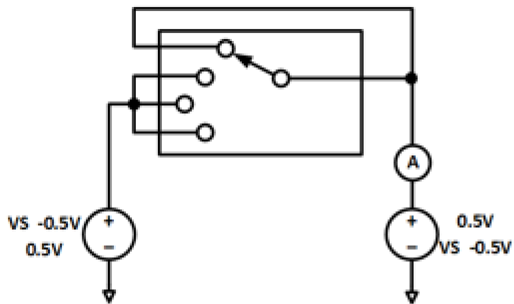
FIGURE 4. Logic diagram.











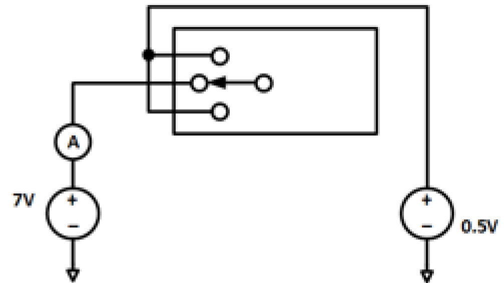
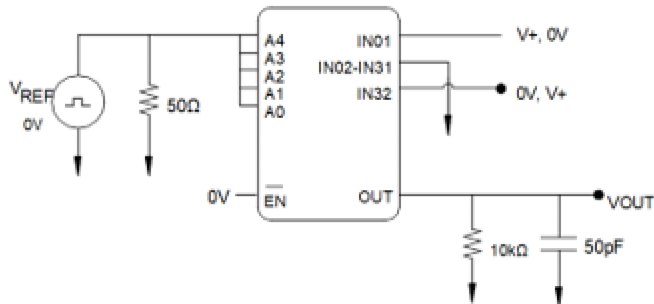
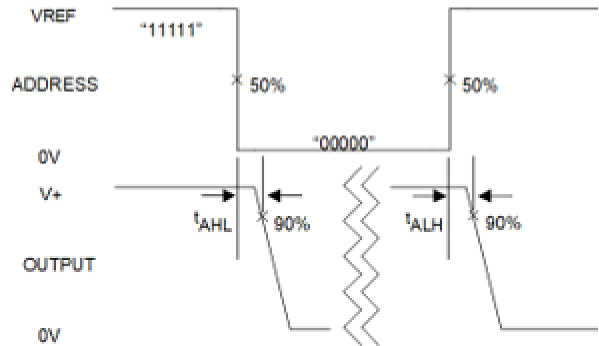


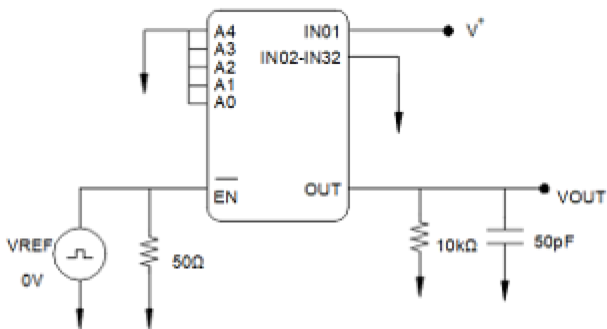
FIGURE 5. Test circuits for dc levels.

Address to output delay





Enable to output delay



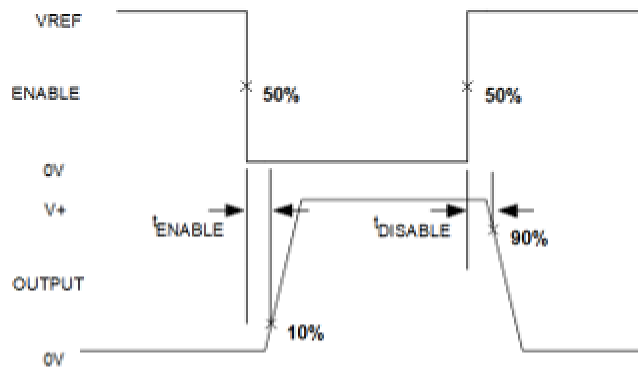
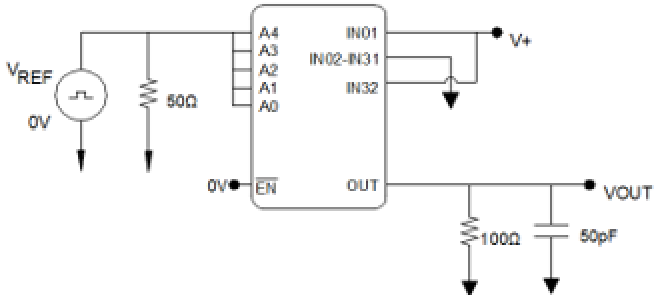
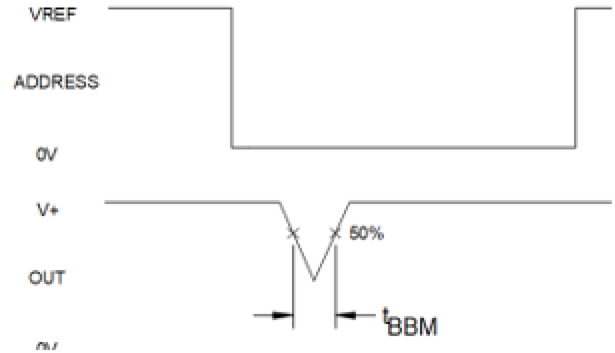


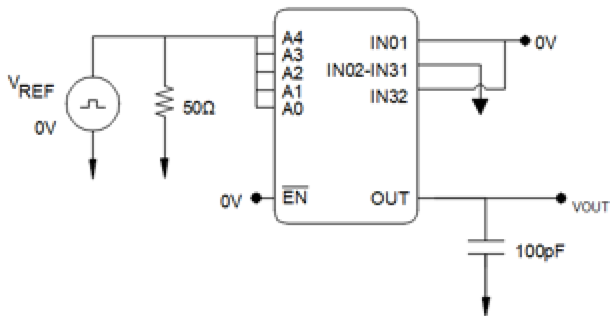
FIGURE 6. Test circuits and waveforms for ac levels.

Break before make delay





Charge injection



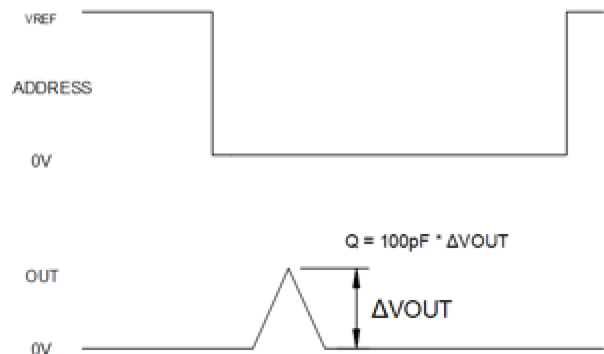


FIGURE 6. Test circuits and waveforms for ac levels – continued

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN(OFF)}$, $C_{OUT(OFF)}$, V_{CT}, V_{CTE}, and V_{ISO} measurements) should be measured for initial qualification and after any process or design changes which may affect input or output capacitance.

d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8A, 1/ 8B,9,10,11	1,2,3, 1/ 2/ 7,8A,8B,9, 10,11
Group A test requirements (see 4.4)	1,2,3,7,8A, 8B,9,10,11	1,2,3,7,8A, 8B,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,7,8A, 8B,9,10,11	1,2,3,4,7, 2/ 8A,8B,9,10,11
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1, 7, and Δ.

2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D, as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any process or design changes which may affect the RHA response of the device.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
Supply current +5.5 V, +3.6 V	I_{SUPPLY}	V_{ref} and V_{en} = V+	±60 nA
I reference current +5.5 V, +3.6 V	I_{REF}	V+ and V_{en} = V_{ref}	±70 nA
Switch on resistance	R_{ON}	V_S = +3.0 V, I_D = 1 mA	±20 Ω
Switch on resistance	R_{ON}	V_S = +4.5 V, I_D = 1 mA	±15 Ω
Input leakage current, address and enable pin(s)	I_{IH}/I_{IL}	Measure inputs sequentially, ground all unbiased pins	±20 nA
Switch off leakage into the source of an unselected channel	$I_{IN(OFF)}$	V_S = +5.5 V, V_{IN} = +5 V, Measure inputs sequentially	±5 nA
Switch off leakage into the drain with the part disabled	$I_{OUT(OFF)}$	V_S = +5.5 V, V_{OUT} = +5 V	±5 nA
Switch on leakage into the source/drain for a selected switch	$I_{OUT(ON)}$	V_S = +5.5 V, V_{IN} = V_{OUT} = +5 V	±5 nA
Switch off leakage into the source of an unselected channel	$I_{IN(OFF)}$	V_S = 5.5 V, V_{IN} = +.5 V measure inputs sequentially	±5 nA
Switch off leakage into the drain with the part disabled	$I_{OUT(OFF)}$	V_S = +5.5 V, V_{OUT} = +.5 V	±5 nA
Switch on leakage into the source/drain for a selected switch	$I_{OUT(ON)}$	V_S = +5.5 V, V_{IN} = V_{OUT} = +.5 V	±5 nA

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test conditions (SEP).

b. Occurrence of latchup (SEL).

c. Occurrence of single event burn-out (SEB).

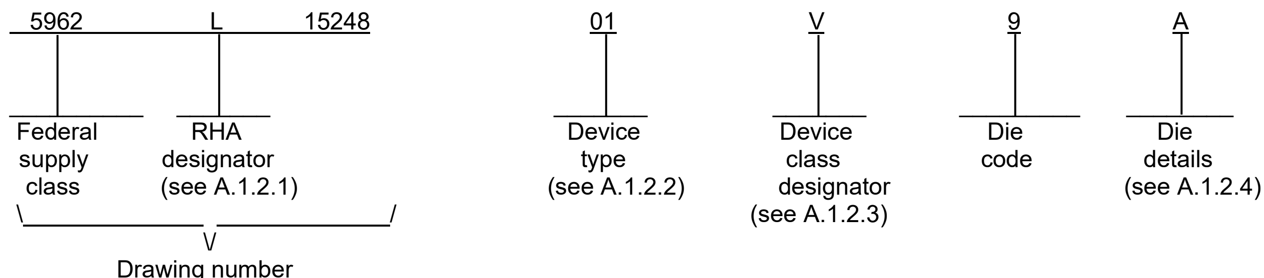
d. Observance of single event transient (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-15248

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type. This device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL71831SEH	Radiation hardened, dielectrically isolated (DI), BICMOS, single 32-channel analog MUX with high impedance analog input overvoltage protection

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

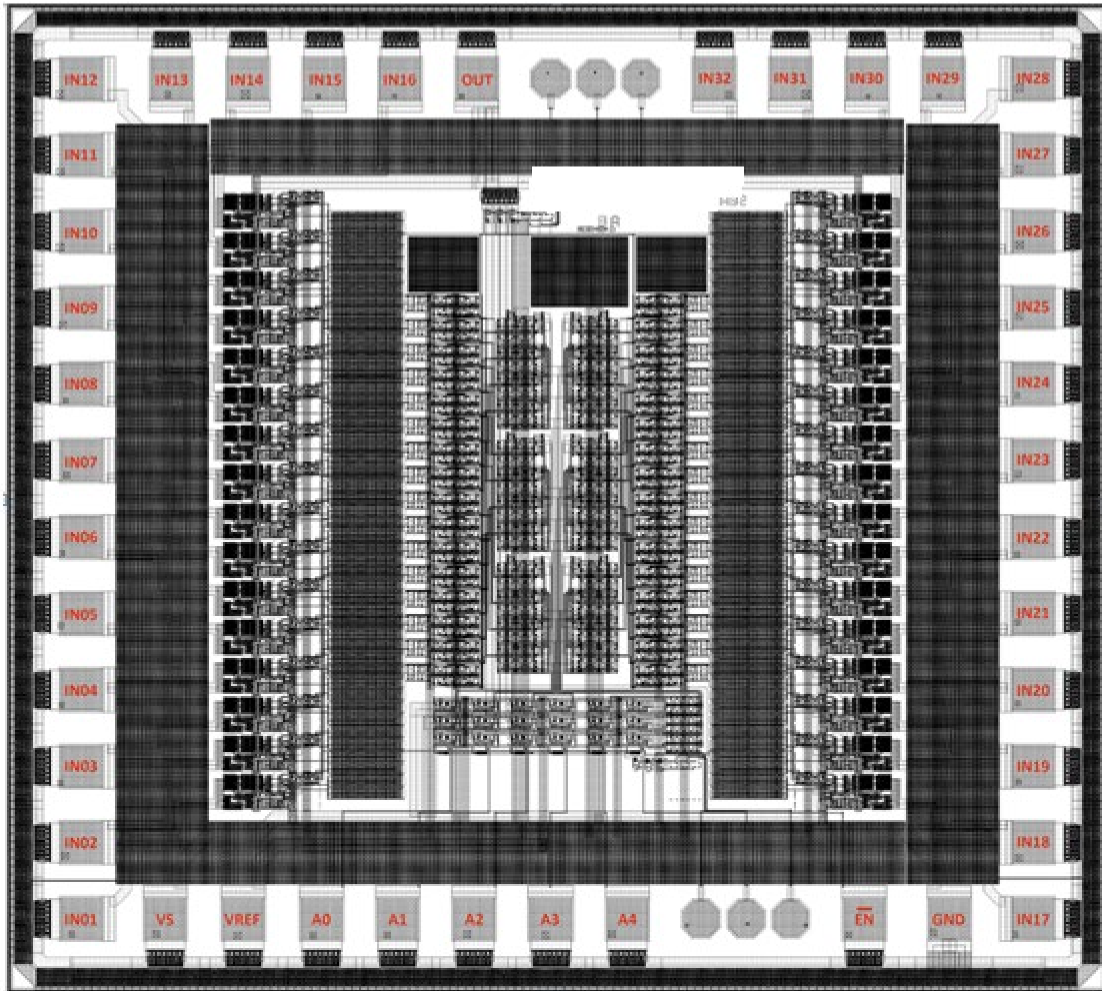
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-15248



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 3102 μm x 2800 μm (122 mils x 110 mils)

Die thickness: 483 microns ± 25.4 microns.

Interface materials.

Top metallization: 300Å TiN on 2.8μm AlCu, TiN removed from bond pads

Backside metallization: Silicon

Glassivation.

Type: Silicon Nitride on Oxide

Thickness: 12kÅ Silicon Nitride on 3kÅ Oxide

Substrate.

Bonded wafer dielectrically isolated.

Assembly related information.

Substrate potential: Floating

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-12-05

Approved sources of supply for SMD 5962-15248 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L1524801VXC	34371	ISL71831SEHVF
5962L1524801V9A	34371	ISL71831SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.