REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraph 4.4.4.1.1 Accelerated annealing test and make change to paragraph A.4.3.1.- ro	16-04-05	C. SAFFLE
B	Make change to the "V_{CC} to GND with / without ion beam" maximum limit from 4.5 V to 5.5 V as specified under paragraph 1.3. - ro	16-08-09	C. SAFFLE
C	Add device types 04, 05, and 06. Make changes to the SEL and SEB limits as specified under paragraph 1.5. Make limit changes under SEP table IB.- ro	17-01-18	C. SAFFLE
D	Add RHA device types 07, 08, 09, 10, 11 and 12. - ro	17-10-23	C. SAFFLE
E	Update document paragraphs to current requirements. - ro	23-02-01	J. ESCHMEYER

Revision Status of Sheets

REV	E	E	E	E	E	E	E	E	E	E	E											
SHEET	45	46	47	48	49	50	51	52	53	54	55											
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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DRAWING APPROVAL DATE
16-03-01

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

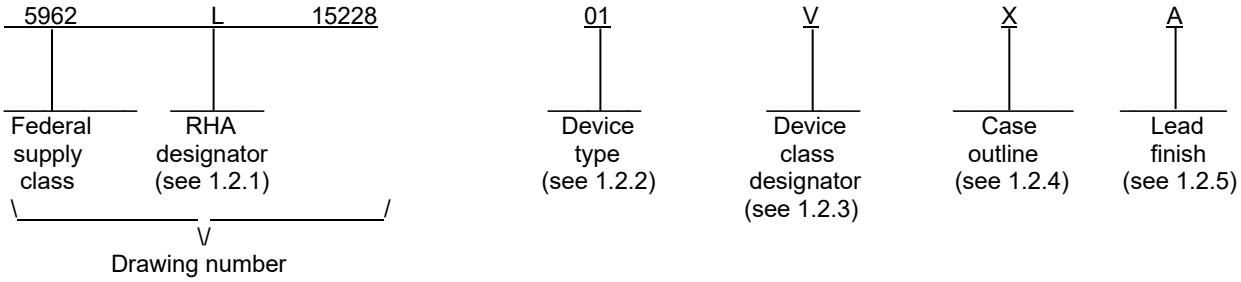
MICROCIRCUIT, LINEAR, 3.3 V CAN TRANSCEIVER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL E	SIZE A	CAGE CODE **67268**	**5962-15228**
		SHEET	1 OF 55	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL72026SEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
02	ISL72027SEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
03	ISL72028SEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output
04	ISL72026BSEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
05	ISL72027BSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
06	ISL72028BSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output
07	ISL72026ASEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
08	ISL72027ASEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
09	ISL72028ASEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output

1.2.2 Device type(s) - continued. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
10	ISL72026CSEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
11	ISL72027CSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
12	ISL72028CSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

V_{CC} to GND with / without ion beam	-0.3 V to 5.5 V
CANH, CANL, VREF (with / without ion beam)	±20 V
I/O voltages	
D, R, RS	-0.5 V to 7 V
Receiver output current	-10 mA to 10 mA
Output short circuit duration	Continuous
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-ambient (θ_{JA}) direct attach	39°C/W 2/
Thermal resistance, junction-to-case (θ_{JC}) direct attach	7°C/W 3/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (two buried 1 ounce copper planes) with “direct attach” features package base mounted to printed circuit board (PCB) thermal land with a 10 mil gap fill material having a k of 1 W/m-K. See manufacturer Tech Brief TB379.

3/ For θ_{JC}, the case temperature location is the center of the package underside.

1.4 Recommended operating conditions.

V_{CC} supply voltage	3.0 V to 3.6 V
Voltage on CAN I/O	-7 V to 12 V
V_{IH} D logic pin (D, LBK)	2 V to 5.5 V
V_{IL} D logic pin (D, LBK)	0 V to 0.8 V
I_{OH} driver (V_{OD} = 1.5 V, V_{CC} = 3.3 V)	-40 mA
I_{OH} receiver (V_{OH} = 2.4 V)	-4 mA
I_{OL} driver (V_{OD} = 1.5 V, V_{CC} = 3.3 V)	+40 mA
I_{OL} receiver	+4 mA
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available(low dose rate ≤ 10 mrad(Si)/s) :	
Device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	50 krad(Si) 4/ 5/
Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s):	
Device types 04, 05, 06, 10, 11, 12	100 krad(Si) 5/
Single event phenomena (SEP) :	
No SEL occurs at effective LET (see 4.4.4.2)	≤ 86 MeV/(mg/cm^2) 6/
No SEB occurs at surface LET (see 4.4.4.2)	≤ 86 MeV/(mg/cm^2) 6/
No SET observed at LET (see 4.4.4.2)	≤ 2.7 MeV/(mg/cm^2)
(Saturated cross section= 5 x 10^{-8} cm^2)	

_____

4/ Device types 01, 02, 03, 07, 08, 09 have been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device types 01, 02, 03, 07, 08, 09 are wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krad(Si) TID level.

5/ Device types 04, 05, 06, 10, 11, and 12 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krad(Si) and condition D to a maximum total dose of 75 krad(Si). The devices are marked at the high dose rate condition A to a TID level 100 krad(Si).

6/ Device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 12 use silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(mg/cm^2). The normal particle range into silicon for Au ions after 30 mm of air is about 115 μm and the Bragg peak range is 53 μm, resulting in ion penetration well beyond the sensitive volume of the devices.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Test circuits and waveforms. The test circuit and waveforms shall be as specified on figures 3 through 24.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics							
Dominant bus output voltage	VO(DOM)	D = 0 V, CANH, RS = GND, see figures 3, 4	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	2.25	VCC	V
		M, D, P, L, R, D = 0 V, CANH, RS = GND, see figures 3, 4	1 2/		2.25	VCC	
		D = 0 V, CANL, RS = GND, see figures 3, 4	1,2,3		0.1	1.25	
		M, D, P, L, R, D = 0 V, CANL, RS = GND, see figures 3, 4	1 2/		0.1	1.25	
Recessive bus output voltage	VO(REC)	D = 3 V, CANH, RS = GND, 60 Ω and no load, see figures 3, 4	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	1.8	2.7	V
		M, D, P, L, R, D = 3 V, CANH, RS = GND, 60 Ω and no load, see figures 3, 4	1 2/		1.8	2.7	
		D = 3 V, CANL, RS = GND, 60 Ω and no load, see figures 3, 4	1,2,3		1.8	2.8	
		M, D, P, L, R, D = 3 V, CANL, RS = GND, 60 Ω and no load, see figures 3, 4	1 2/		1.8	2.8	
Dominant output differential voltage	VOD(DOM)	D = 0 V, RS = GND, see figures 3, 4	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	1.5	3.0	V
		M, D, P, L, R, D = 0 V, RS = GND, see figures 3, 4	1 2/		1.5	3.0	
		D = 0 V, RS = GND, see figures 4, 5	1,2,3		1.2	3.0	
		M, D, P, L, R, D = 0 V, RS = GND, see figures 4, 5	1 2/		1.2	3.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics – continued.							
Recessive output differential voltage	$V_{OD(REC)}$	D = 3 V, RS = GND, see figures 3, 4	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	-120	12	mV
		M, D, P, L, R, D = 3 V, RS = GND, see figures 3, 4	1 2/		-120	12	
		D = 3 V, RS = GND, no load	1,2,3		-500	50	
		M, D, P, L, R, D = 3 V, RS = GND, no load	1 2/		-500	50	
Logic input high voltage (LBK)	V_{IH}	3/ 4/	1,2,3	01, 04, 07, 10	2.0	5.5	V
		M, D, P, L, R, 3/ 4/	1 2/ 4/		2.0	5.5	
Logic input low voltage (LBK)	V_{IL}	3/ 4/	1,2,3	01, 04, 07, 10	0	0.8	V
		M, D, P, L, R, 3/ 4/	1 2/ 4/		0	0.8	
Logic input high voltage (D)	V_{IH}	3/	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	2.0	5.5	V
		M, D, P, L, R, 3/	1 2/		2.0	5.5	
Logic input low voltage (D)	V_{IL}	3/	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	0	0.8	V
		M, D, P, L, R 3/	1 2/		0	0.8	
Logic high level input current (LBK)	I_{IH}	LBK = 2.0 V 4/	1,2,3	01, 04, 07, 10	-30	30	µA
		M, D, P, L, R, LBK = 2.0 V 4/	1 2/ 4/		-30	30	
Logic high level input current (D)	I_{IH}	D = 2.0 V	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	-30	30	µA
		M, D, P, L, R, D = 2.0 V	1 2/		-30	30	
Logic low level input current (LBK)	I_{IL}	LBK = 0.8 V 4/	1,2,3	01, 04, 07, 10	-30	30	µA
		M, D, P, L, R, LBK = 0.8 V 4/	1 4/		-30	30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics – continued.							
Logic low level input current (D)	I_{IL}	D = 0.8 V	1,2,3	01, 02, 03, 04, 05, 06,	-30	30	µA
		M, D, P, L, R, D = 0.8 V	1 2/	07, 08, 09, 10, 11, 12	-30	30	
RS input voltage for listen mode	$V_{IN(RS)}$		1,2,3	01, 02, 03, 04, 05, 06,	0.75 V_{CC}	5.5	V
		M, D, P, L, R	1 2/	07, 08, 09, 10, 11, 12	0.75 V_{CC}	5.5	
Output short circuit current	I_{OSC}	VCANH = -7 V, CANL = open, see figures 6, 7	1,2,3	01, 02, 03, 04, 05, 06,	-250		mA
		M, D, P, L, R, VCANH = -7 V, CANL = open, see figures 6, 7	1 2/	07, 08, 09, 10, 11, 12	-250		
		VCANH = +12 V, CANL = open, see figures 6, 7	1,2,3			1	
		M, D, P, L, R, VCANH = +12 V, CANL = open, see figures 6, 7	1 2/			1	
		VCANL = -7 V, CANH = open, see figures 6, 7	1,2,3		-1		
		M, D, P, L, R, VCANL = -7 V, CANH = open, see figures 6, 7	1 2/		-1		
		VCANL = +12 V, CANH = open, see figures 6, 7	1,2,3			250	
		M, D, P, L, R, VCANL = +12 V, CANH = open, see figures 6, 7	1 2/			250	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics							
Input threshold voltage (rising) (LBK)	VTHR	LBK = 0 V, 4/ RS = GND, 10 kΩ, 50 kΩ, (recessive to dominant), see figures 8, 9, 10, and 11	1,2,3	01, 04, 07, 10		900	mV
		M, D, P, L, R, LBK = 0 V, 4/ RS = GND, 10 kΩ, 50 kΩ, (recessive to dominant), see figures 8, 9, 10, and 11	1 2/ 4/			900	
Input threshold voltage (rising)	VTHR	RS = GND, 10 kΩ, 50 kΩ, (recessive to dominant), see figures 8, 9, 10, and 11	1,2,3	02, 03, 05, 06 08, 09, 11, 12		900	mV
		M, D, P, L, R, RS = GND, 10 kΩ, 50 kΩ, (recessive to dominant), see figures 8, 9, 10, and 11	1 2/			900	
Input threshold voltage (falling) (LBK)	VTHF	LBK = 0 V, 4/ RS = GND, 10 kΩ, 50 kΩ, (dominant to recessive), see figures 8, 9, 10, and 11	1,2,3	01, 04, 07, 10	500		mV
		M, D, P, L, R, LBK = 0 V, 4/ RS = GND, 10 kΩ, 50 kΩ, (dominant to recessive), see figures 8, 9, 10, and 11	1 2/ 4/		500		
Input threshold voltage (falling)	VTHF	RS = GND, 10 kΩ, 50 kΩ, (dominant to recessive), see figures 8, 9, 10, and 11	1,2,3	02, 03, 05, 06, 08, 09 11, 12	500		mV
		M, D, P, L, R, RS = GND, 10 kΩ, 50 kΩ, (dominant to recessive), see figures 8, 9, 10, and 11	1 2/		500		
Input hysteresis	VHYS	(VTHR - VTHF), RS = GND, 10 kΩ, 50 kΩ, see figures 8, 9, 10, and 11	1,2,3	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	40		mV
		M, D, P, L, R, (VTHR - VTHF), RS = GND, 10 kΩ, 50 kΩ, see figures 8, 9, 10, and 11	1 2/		40		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics - continued.							
Listen mode input threshold voltage (rising)	VTHRLM	RS = V_{CC}, (recessive to dominant), see figures 8, 9, and 10	1,2,3	01, 02, 04, 05		1150	mV
		M, D, P, L, R, RS = V_{CC}, (recessive to dominant), see figures 8, 9, and 10	1 2/			1150	
		RS = V_{CC}, (recessive to dominant), see figures 8, 9, and 10	1,2,3	07, 08, 10, 11		900	
		M, D, P, L, R, RS = V_{CC}, (recessive to dominant), see figures 8, 9, and 10	1 2/			900	
Listen mode input threshold voltage (falling)	VTHFLM	RS = V_{CC}, (dominant to recessive), see figures 8, 9, and 10	1,2,3	01, 02, 04, 05	525		mV
		M, D, P, L, R, RS = V_{CC}, (dominant to recessive), see figures 8, 9, and 10	1 2/		525		
		RS = V_{CC}, (dominant to recessive), see figures 8, 9, and 10	1,2,3	07, 08, 10, 11	325		
		M, D, P, L, R, RS = V_{CC}, (dominant to recessive), see figures 8, 9, and 10	1 2/		325		
Listen mode input hysteresis	VHYSLM	(VTHR - VTHF), RS =V_{CC}, see figures 8, 9, and 10	1,2,3	01, 02, 04, 05	50		mV
		M, D, P, L, R, (VTHR - VTHF), RS =V_{CC}, see figures 8, 9, and 10	1 2/		50		
		(VTHR - VTHF), RS =V_{CC}, see figures 8, 9, and 10	1,2,3	07, 08, 10, 11	40		
		M, D, P, L, R, (VTHR - VTHF), RS =V_{CC}, see figures 8, 9, and 10	1 2/		40		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics - continued.							
Receiver output high voltage	V_{OH}	I_O = -4 mA	1,2,3	01, 02, 03, 04, 05, 06,	2.4		V
		M, D, P, L, R, I_O = -4 mA	1 2/	07, 08, 09, 10, 11, 12	2.4		
Receiver output low voltage	V_{OL}	I_O = +4 mA	1,2,3	01, 02, 03, 04, 05, 06,		0.4	V
		M, D, P, L, R, I_O = +4 mA	1 2/	07, 08, 09, 10, 11, 12		0.4	
Input current for CAN bus (LBK)	ICAN	CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1,2,3	01, 04		500	µA
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1 2/ 4/			500	
		CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1,2,3	07, 10		600	
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1 2/ 4/			600	
		CANH or CANL at 12 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1,2,3	01, 04		250	
		M, D, P, L, R, CANH or CANL at 12 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1 2/ 4/			250	
		CANH or CANL at 12 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1,2,3	07, 10		275	
		M, D, P, L, R, CANH or CANL at 12 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1 2/ 4/			275	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteri stics - continued.							
Input current for CAN bus (LBK)	ICAN	CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1,2,3	01, 04	-400		µA
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1 2/ 4/		-400		
		CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1,2,3	07, 10	-500		
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, LBK = RS = GND 4/	1 2/ 4/		-500		
		CANH or CANL at -7 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1,2,3	01, 04	-150		
		M, D, P, L, R, CANH or CANL at -7 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1 2/ 4/		-150		
		CANH or CANL at -7 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1,2,3	07, 10	-175		
		M, D, P, L, R, CANH or CANL at -7 V, 4/ D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, LBK = RS = GND	1 2/ 4/		-175		
Input current for CAN bus	ICAN	CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, RS = GND	1,2,3	02, 03, 05, 06		500	µA
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, RS = GND	1 2/			500	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteri stics - conti nued.							
Input current for CAN bus	ICAN	CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, RS = GND	1,2,3	08, 09, 11, 12		600	µA
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, other bus pin at 0 V, RS = GND	1 2/			600	
		CANH or CANL at 12 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1,2,3	02, 03, 05, 06		250	
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1 2/			250	
		CANH or CANL at 12 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1,2,3	08, 09, 11, 12		275	
		M, D, P, L, R, CANH or CANL at 12 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1 2/			275	
		CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, RS = GND	1,2,3	02, 03, 05, 06	-400		
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, RS = GND	1 2/		-400		
		CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, RS = GND	1,2,3	08, 09, 11, 12	-500		
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, other bus pin at 0 V, RS = GND	1 2/		-500		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteri stics - conti nued.							
Input current for CAN bus	ICAN	CANH or CANL at -7 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1,2,3	02, 03, 05, 06	-150		µA
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1 2/		-150		
		CANH or CANL at -7 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1,2,3	08, 09, 11, 12	-175		
		M, D, P, L, R, CANH or CANL at -7 V, D = 3 V, V_{CC} = 0 V, other bus pin at 0 V, RS = GND	1 2/		-175		
Input resistance (CANH or CANL) (LBK)	RIN	Input to GND, D = 3 V, LBK = RS = GND	4,5,6	01, 04, 07, 10	20	50	kΩ
		M, D, P, L, R, Input to GND, D = 3 V, LBK = RS = GND	4 2/ 4/		20	50	
Input resistance (CANH or CANL)	RIN	Input to GND, D = 3 V, RS = GND	4,5,6	02, 03, 05, 06, 08, 09, 11, 12	20	50	kΩ
		M, D, P, L, R, Input to GND, D = 3 V, RS = GND	4 2/		20	50	
Differential input resistance (LBK)	RIND	Input to GND, D = 3 V, LBK = RS = GND	4,5,6	01, 04, 07, 10	40	100	kΩ
		M, Input to GND, D = 3 V, LBK = RS = GND D, P, L, R,	4 2/ 4/		40	100	
Differential input resistance	RIND	Input to GND, D = 3 V, RS = GND	4,5,6	02, 03, 05, 06, 08, 09, 11, 12	40	100	kΩ
		M, D, P, L, R, Input to GND, D = 3 V, RS = GND	4 2/		40	100	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteri stics - conti nued.							
Supply current							
Supply current, listen mode (LBK)	ICC(L)	RS = D = VCC, LBK = 0 V 4/	1,2,3	01, 04,		2	mA
		M, D, P, L, R, RS = D = VCC, LBK = 0 V 4/	1 2/ 4/	07, 10		2	
Supply current, listen mode	ICC(L)	RS = D = V_{CC}	1,2,3	02, 05,		2	mA
		M, D, P, L, R, RS = D = V_{CC}	1 2/	08, 11		2	
Supply current, low power shutdown mode	ICC(LPS)	RS = D = V_{CC} 4/	1,2,3	03, 06,		50	µA
		M, D, P, L, R, RS = D = V_{CC} 4/	1 4/	09, 12		50	
Supply current, dominant (LBK)	ICC(DOM)	D = LBK = RS = GND, 4/ no load	1,2,3	01, 04, 07, 10		7	mA
		M, D, P, L, R, D = LBK = RS = GND, 4/ no load	1 2/ 4/			7	
Supply current, dominant	ICC(DOM)	D = RS = GND, no load	1,2,3	02, 03, 05, 06,		7	mA
		M, D, P, L, R, D = RS = GND, no load	1 2/	08, 09, 11, 12		7	
Supply current, recessive (LBK)	ICC(REC)	D = V_{CC}, LBK = RS = GND, no load 4/	1,2,3	01, 04, 07, 10		5	mA
		M, D, P, L, R, D = V_{CC}, LBK = RS = GND, no load 4/	1 2/ 4/			5	
Supply current, recessive	ICC(REC)	D = V_{CC}, RS = GND, no load	1,2,3	02, 03, 05, 06,		5	mA
		M, D, P, L, R, D = V_{CC}, RS = GND, no load	1 2/	08, 09, 11, 12		5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Cold sparing bus current							
CANH leakage current	IL(CANH)	V_{CC} =0.2 V, RS = GND, CANH = -7 V or 12 V, CANL = float, D = V_{CC}	1,2,3	01, 02, 03, 04, 05, 06, 07, 08,	-25	25	µA
		M, D, P, L, R, V_{CC} =0.2 V, RS = GND, CANH = -7 V or 12 V, CANL = float, D = V_{CC}	1 2/	09, 10, 11, 12	-25	25	
CANL leakage current	IL(CANL)	V_{CC} =0.2 V, RS = GND, CANL = -7 V or 12 V, CANH = float, D = V_{CC}	1,2,3	01, 02, 03, 04, 05, 06, 07, 08,	-25	25	µA
		M, D, P, L, R, V_{CC} =0.2 V, RS = GND, CANL = -7 V or 12 V, CANH = float, D = V_{CC}	1 2/	09, 10, 11, 12	-25	25	
VREF leakage current	IL(VREF)	V_{CC} =0.2 V, VREF= -7 V or 12 V, D = V_{CC}	1,2,3	02, 03, 05, 06, 08, 09,	-25	25	µA
		M, D, P, L, R, V_{CC} =0.2 V, VREF= -7 V or 12 V, D = V_{CC}	1 2/	11, 12	-25	25	
Driver switching characteristics							
Propagation delay low to high	tPDLH1	RS = GND, see figures 12, 13	9,10,11	01, 02, 03, 04,		150	ns
		M, D, P, L, R, RS = GND, see figures 12, 13	9 2/	05, 06		150	
		RS = GND, see figures 12, 13	9,10,11	07, 08,		160	
		M, D, P, L, R, RS = GND, see figures 12, 13	9 2/	09, 10, 11, 12		160	
	tPDLH2	RS = 10 kΩ, see figures 12, 13	9,10,11	01, 02,		850	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13	9 2/	03, 04, 05, 06		850	
		RS = 10 kΩ, see figures 12, 13	9,10,11	07, 08,		550	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13	9 2/	09, 10, 11, 12		550	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics – continued.							
Propagation delay low to high	t_{PDLH3}	RS = 50 kΩ, see figures 12, 13	9,10,11	01, 02,		1400	ns
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13	9 2/	03, 04, 05, 06		1400	
		RS = 50 kΩ, see figures 12, 13	9,10,11	07, 08,		800	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13	9 2/	09, 10, 11, 12		800	
Propagation delay high to low	t_{PDHL1}	RS = GND, see figures 12, 13	9,10,11	01, 02,		155	ns
		M, D, P, L, R, RS = GND, see figures 12, 13	9 2/	03, 04, 05, 06		155	
		RS = GND, see figures 12, 13	9,10,11	07, 08,		180	
		M, D, P, L, R RS = GND, see figures 12, 13	9 2/	09, 10, 11, 12		180	
	t_{PDHL2}	RS = 10 kΩ, see figures 12, 13	9,10,11	01, 02,		800	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13	9 2/	03, 04, 05, 06		800	
		RS = 10 kΩ, see figures 12, 13	9,10,11	07, 08,		600	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13	9 2/	09, 10, 11, 12		600	
	t_{PDHL3}	RS = 50 kΩ, see figures 12, 13	9,10,11	01, 02,		1300	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13	9 2/	03, 04, 05, 06		1300	
		RS = 50 kΩ, see figures 12, 13	9,10,11	07, 08,		900	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13	9 2/	09, 10, 11, 12		900	
Output skew	t_{SKEW1}	RS = GND, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	01, 02, 03, 04,		50	ns
		M, D, P, L, R, RS = GND, see figures 12, 13, (|tPHL - tPLH|)	9 2/	05, 06		50	
		RS = GND, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	07, 08, 09, 10,		65	
		M, D, P, L, R RS = GND, see figures 12, 13, (|tPHL - tPLH|)	9 2/	11, 12		65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ TA ≤ +125°C VCC = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristic s – continued.							
Output skew	tSKEW2	RS = 10 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	01, 02, 03, 04, 05, 06		510	ns
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9 2/			510	
		RS = 10 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	07, 08, 09, 10, 11, 12		275	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9 2/			275	
	tSKEW3	RS = 50 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	01, 02, 03, 04, 05, 06		800	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9 2/			800	
		RS = 50 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9,10,11	07, 08, 09, 10, 11, 12		400	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13, (|tPHL - tPLH|)	9 2/			400	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristiics – continued.							
Output rise time	tr1	RS = GND, see figures 12, 13, (driver fastest speed)	9,10,11	01, 02, 03, 04,	20	100	ns
		M, D, P, L, R, RS = GND, see figures 12, 13, (driver fastest speed)	9 2/	05, 06	20	100	
		RS = GND, see figures 12, 13, (driver fastest speed)	9,10,11	07, 08, 09, 10,	15	85	
		M, D, P, L, R, RS = GND, see figures 12, 13, (driver fastest speed)	9 2/	11, 12	15	85	
	tr2	RS = 10 kΩ, see figures 12, 13, (medium speed)	9,10,11	01, 02, 03, 04,	200	780	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (medium speed)	9 2/	05, 06	200	780	
		RS = 10 kΩ, see figures 12, 13, (medium speed)	9,10,11	07, 08, 09, 10,	125	550	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (medium speed)	9 2/	11, 12	125	550	
	tr3	RS = 50 kΩ , see figures 12, 13, (slowest speed)	9,10,11	01, 02, 03, 04,	400	1400	
		M, D, P, L, R, RS = 50 kΩ , see figures 12, 13, (slowest speed)	9 2/	05, 06	400	1400	
		RS = 50 kΩ , see figures 12, 13, (slowest speed)	9,10,11	07, 08, 09, 10,	200	800	
		M, D, P, L, R, RS = 50 kΩ , see figures 12, 13, (slowest speed)	9 2/	11, 12	200	800	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ TA ≤ +125°C VCC = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics – continued.							
Output fall time	tf1	RS = GND, see figures 12, 13, (driver fastest speed)	9,10,11	01, 02, 03, 04, 05, 06	10	75	ns
		M, D, P, L, R, RS = GND, see figures 12, 13, (driver fastest speed)	9 2/		10	75	
		RS = GND, see figures 12, 13, (driver fastest speed)	9,10,11	07, 08, 09, 10, 11, 12	10	65	
		M, D, P, L, R, RS = GND, see figures 12, 13, (driver fastest speed)	9 2/		10	65	
	tr2	RS = 10 kΩ, see figures 12, 13, (medium speed)	9,10,11	01, 02, 03, 04, 05, 06	175	500	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (medium speed)	9 2/		175	500	
		RS = 10 kΩ, see figures 12, 13, (medium speed)	9,10,11	07, 08, 09, 10, 11, 12	100	425	
		M, D, P, L, R, RS = 10 kΩ, see figures 12, 13, (medium speed)	9 2/		100	425	
Output fall time	tf3	RS = 50 kΩ, see figures 12, 13, (slowest speed)	9,10,11	01, 02, 03, 04, 05, 06	300	1000	ns
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13, (slowest speed)	9 2/		300	1000	
		RS = 50 kΩ, see figures 12, 13, (slowest speed)	9,10,11	07, 08, 09, 10, 11, 12	175	600	
		M, D, P, L, R, RS = 50 kΩ, see figures 12, 13, (slowest speed)	9 2/		175	600	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics – continued.							
Total loop delay, driver input to receiver output, recessive to dominant	t(LOOP1)	RS = GND, see figures 14, 15	9,10,11	01, 04		210	ns
		RS = GND, see figures 16, 17		02, 03, 05, 06		210	
		M, D, P, L, R, RS = GND, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		210	
		RS = GND, see figures 14, 15	9,10,11	07, 10		225	
		RS = GND, see figures 16, 17		08, 09, 11, 12		225	
		M, D, P, L, R, RS = GND, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		225	
		RS = 10 kΩ, see figures 14, 15	9,10,11	01, 04		875	
		RS = 10 kΩ, see figures 16, 17		02, 03, 05, 06		875	
		M, D, P, L, R, RS = GND, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		875	
		RS = 10 kΩ, see figures 14, 15	9,10,11	07, 10		600	
		RS = 10 kΩ, see figures 16, 17		08, 09, 11, 12		600	
		M, D, P, L, R, RS = 10 kΩ, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		600	
Total loop delay, driver input to receiver output, recessive to dominant	t(LOOP1)	RS = 50 kΩ, see figures 14, 15	9,10,11	01, 04		1400	ns
		RS = 50 kΩ, see figures 16, 17		02, 03, 05, 06		1400	
		M, D, P, L, R, RS = 50 kΩ, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		1400	
		RS = 50 kΩ, see figures 14, 15	9,10,11	07, 10		800	
		RS = 50 kΩ, see figures 16, 17		08, 09, 11, 12		800	
		M, D, P, L, R, RS = 50 kΩ, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		800	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0V to 3.6V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristic s - continued .							
Total loop delay, driver input to receiver output, dominant to recessive	t(LOOP2)	RS = GND, see figures 14, 15	9,10,11	01, 04		270	ns
		RS = GND, see figures 16, 17		02, 03, 05, 06		270	
		M, D, P, L, R, RS = GND, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		270	
		RS = GND, see figures 14, 15	9,10,11	07, 10		285	
		RS = GND, see figures 16, 17		08, 09, 11, 12		285	
		M, D, P, L, R, RS = GND, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		285	
		RS = 10 kΩ, see figures 14, 15	9,10,11	01, 04		825	
		RS = 10 kΩ, see figures 16, 17		02, 03, 05, 06		825	
		M, D, P, L, R, RS = 10 kΩ, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		825	
		RS = 10 kΩ, see figures 14, 15	9,10,11	07, 10		700	
		RS = 10 kΩ, see figures 16, 17		08, 09, 11, 12		700	
		M, D, P, L, R, RS = 10 kΩ, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		700	
Total loop delay, driver input to receiver output, dominant to recessive	t(LOOP2)	RS = 50 kΩ, see figures 14, 15	9,10,11	01, 04		1300	ns
		RS = 50 kΩ, see figures 16, 17		02, 03, 05, 06		1300	
		M, D, P, L, R, RS = 50 kΩ, see figures 16, 17	9 2/	01, 02, 03, 04, 05, 06		1300	
		RS = 50 kΩ, see figures 14, 15	9,10,11	07, 10		950	
		RS = 50 kΩ, see figures 16, 17		08, 09, 11, 12		950	
		M, D, P, L, R, RS = 50 kΩ, see figures 16, 17	9 2/	07, 08, 09, 10, 11, 12		950	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ TA ≤ +125°C VCC = 3.0V to 3.6V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics – continued.							
Listen to valid dominant time	tL-DOM	See figures 18, 20	9,10,11	01, 02, 04, 05,		15	µs
		M, D, P, L, R, See figures 18, 20	9 2/	07, 08, 10, 11		15	
Low power shutdown valid dominant time	tLPS-DOM	See figures 21, 22 4/	9,10,11	03, 06,		15	µs
		M, D, P, L, R, See figures 21, 22 4/	9 2/ 4/	09, 12		15	
Receiver switching characteristics							
Propagation delay low to high	tPLH	See figures 8, 9, 10	1,2,3	01, 02, 03, 04, 05, 06,		110	ns
		M, D, P, L, R, See figures 8, 9, 10	1 2/	07, 08, 09, 10, 11, 12		110	
Propagation delay high to low	tPHL	See figures 8, 9, 10	1,2,3	01, 02, 03, 04, 05, 06,		110	ns
		M, D, P, L, R, See figures 8, 9, 10	1 2/	07, 08, 09, 10, 11, 12		110	
Rx skew	tSKEW1	See figures 8, 9, 10, |(tPHL - tPLH)|	1,2,3	01, 02, 03, 04, 05, 06,		35	ns
		M, D, P, L, R, See figures 8, 9, 10, |(tPHL - tPLH)|	1 2/	07, 08, 09, 10, 11, 12		35	
LBK delay I/O to Rx output	tLBK	See figures 23, 24 4/	1,2,3	01, 04		75	ns
		M, D, P, L, R, See figures 23, 24 4/	1 2/ 4/			75	
		See figures 23, 24 4/	1,2,3	07, 10		90	
		M, D, P, L, R, See figures 23, 24 4/	1 2/ 4/			90	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = 3.0 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{REF} / RS pin characteristics							
V_{REF} pin voltage	V_{REF}	5 µA < IREF < 5 µA	1,2,3	02, 03, 05, 06, 08, 09, 11, 12	0.45 x V_{CC}	0.55 x V_{CC}	V
		M, D, P, L, R, 5 µA < IREF < 5 µA	1 2/		0.45 x V_{CC}	0.55 x V_{CC}	
		50 µA < IREF < 50 µA	1,2,3		0.4x V_{CC}	0.6x V_{CC}	
		M, D, P, L, R, 50 µA < IREF < 50 µA	1 2/		0.4x V_{CC}	0.6x V_{CC}	
RS input current, high	IRSH	RS = 0.75 X V_{CC}	1,2,3	01,02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	-10		µA
		M, D, P, L, R, RS = 0.75 X V_{CC}	1		-10		
RS input current, low	IRSL	RS = GND	1,2,3	01,02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	-450	0	µA

1/ Unless otherwise specified, V_{CC} = 3.0 V to 3.6 V.

2/ RHA device types 01, 02, 03, 07, 08, and 09 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device types 01, 02, 03, 07, 08, and 09 are only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total dose of 75 krad(Si). Device types 01, 02, 03, 07, 08, and 09 are wafer acceptance tested 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krad(Si) level.
RHA device types 04, 05, 06, 10, 11, and 12 supplied to this drawing will meet all levels M, D, P, L and R of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device types 04, 05, 06, 10, 11, and 12 are only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A to TID level 100 krad(Si) and condition D to TID level 75 krad(Si) (see 1.5 herein).
Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Parameter included in functional testing.

4/ Performed during the 100% screening operations in production over the full operating temperature range. Not performed as part of TCI Group C and Group E. Radiation characterization testing performed as part of initial release and after any major changes in design.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Temperature (T_C)	Bus voltage (VCANH, VCANL)	Supply voltage (V_{CC})	Linear energy transfer (LET) 4/
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	No SEL	125°C	±20 V	5.5 V	86 MeV/(mg/cm^2)
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	No SEB	25°C	±20 V	5.5 V	86 MeV/(mg/cm^2)
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	No SET	25°C	Floating	3.0 V	2.7 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer's SEE test report for more information.

4/ Device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 12 use silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Au ions at normal incidence, corresponding to a surface LET of 86 MeV/(mg/cm^2). The normal particle range into silicon for Au ions after 30 mm of air is about 115 μm and the Bragg peak range is 53 μm, resulting ion penetration well beyond the sensitive volume of the devices.

Case outline X

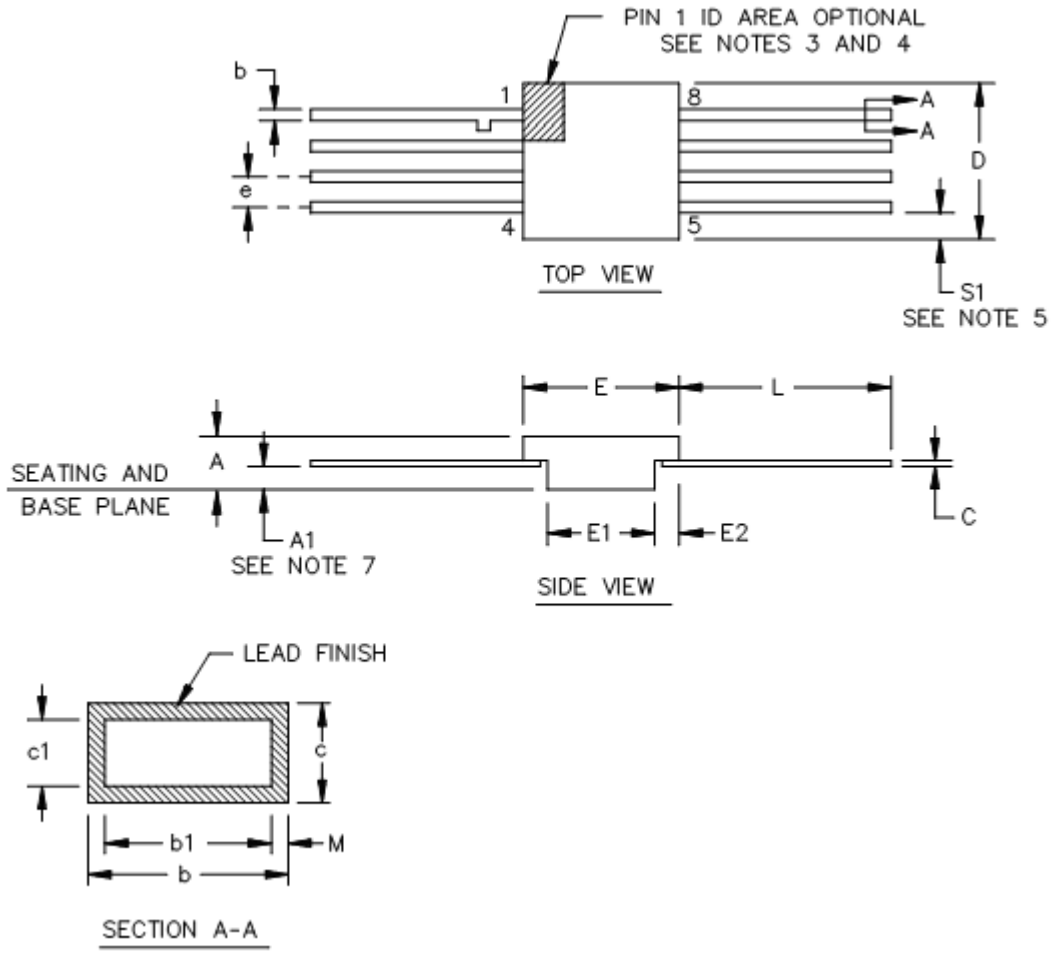


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-15228**
		REVISION LEVEL **E**	SHEET **27**

Case outline X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.087	.110	2.21	2.79
A1	.026	.036	0.66	0.92
b	.015	.022	0.38	0.56
c	.004	.009	0.10	0.23
D	.245	.265	6.22	6.73
E	.245	.265	6.22	6.75
E1	.170	.180	4.32	4.57
E2	0.03		0.76	
e	.050 BSC		1.27 BSC	
L	.325	.370	8.26	9.40

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as pin one identification mark. Alternately, a tab may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
4. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, When solder dip or tin plate lead finish is applied.
5. Measure dimension at all four corners.
6. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the packages to cover the leads.
7. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outline – continued..

Device types	01, 04, 07, 10	02, 05, 08, 11	03, 06, 09, 12
Case outline	X	X	X
Terminal number	Terminal symbol		
1	D	D	D
2	GND	GND	GND
3	V_{CC}	V_{CC}	V_{CC}
4	R	R	R
5	LBK	VREF	VREF
6	CANL	CANL	CANL
7	CANH	CANH	CANH
8	RS	RS	RS
Package lid	Tied internally to terminal 2 (GND)	Tied internally to terminal 2 (GND)	Tied internally to terminal 2 (GND)

Terminal symbol	Description
D	CAN driver digital input. The bus states are LOW = dominant and HIGH = recessive.
GND	Ground pin of the device.
V_{CC}	Supply pin of the device. The typical voltage for the device is 3.3 V.
R	CAN data receiver output for the device. The bus states are LOW = dominant and HIGH = recessive.
RS	A resistor to GND from this pin controls the rise and fall time of the CAN output waveform. Drive RS HIGH to put into listen mode.
CANL	CAN bus line for low level output
CANH	CAN bus line for high level output
LBK	A high on this pin places CANH & CANL pins in a high impedance state. The rest of the circuit remains active so that the TX and Rx can loopback diagnostic information. Internal tied low.
VREF	$V_{CC}/2$ reference output for split mode termination.
Package lid	Tied internally to terminal 2 (GND)

FIGURE 2. Terminal connections.

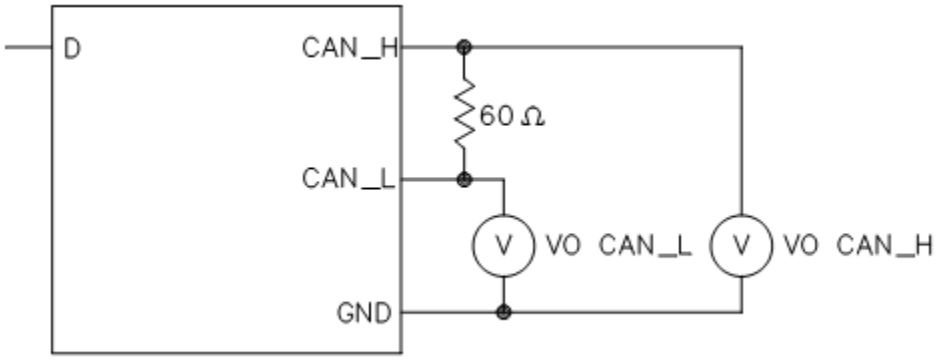


FIGURE 3. Driver test circuit.

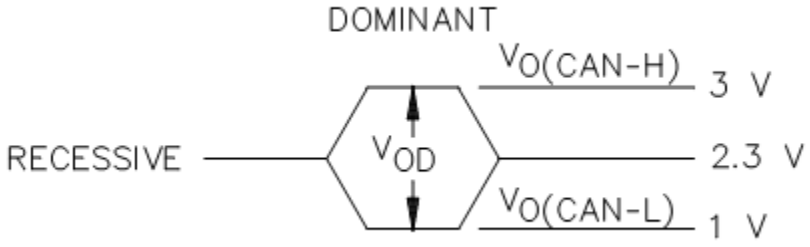


FIGURE 4. Driver bus voltage definitions.

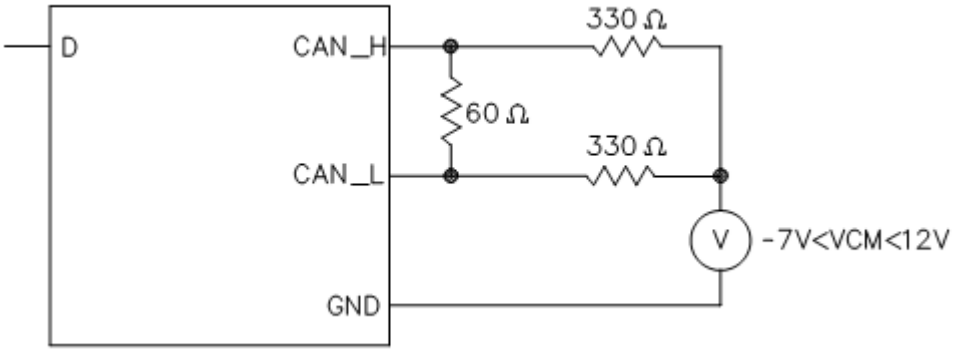


FIGURE 5. Driver common mode circuit.

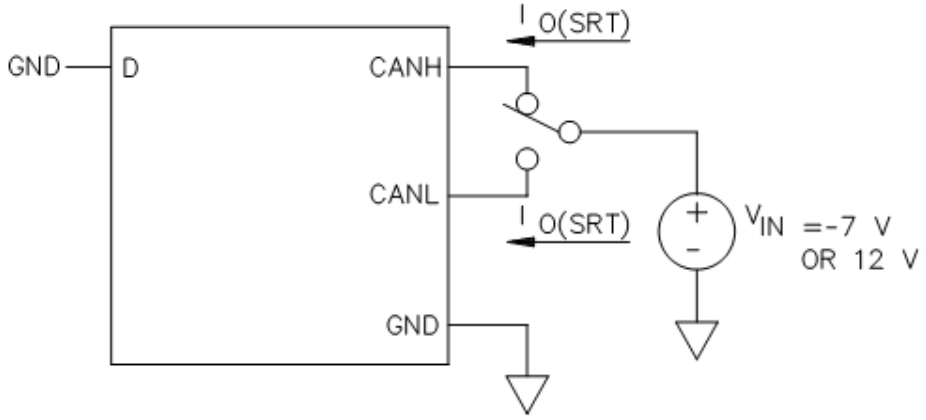


FIGURE 6. Output short circuit current circuit.

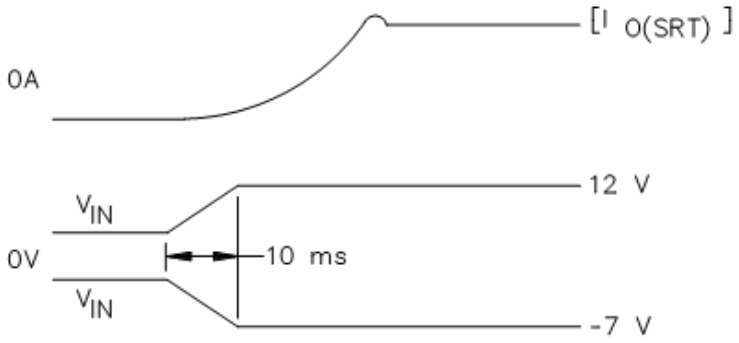


FIGURE 7. Output short circuit current waveforms.

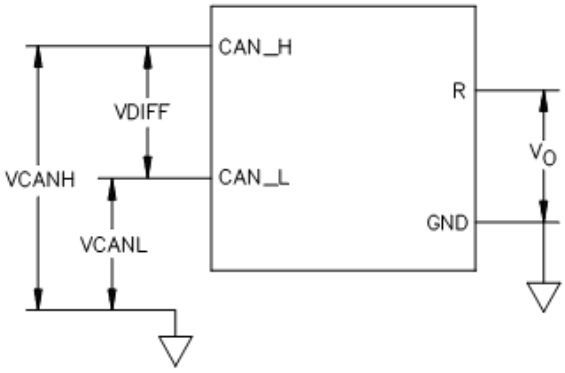


FIGURE 8. Receiver voltage definitions.

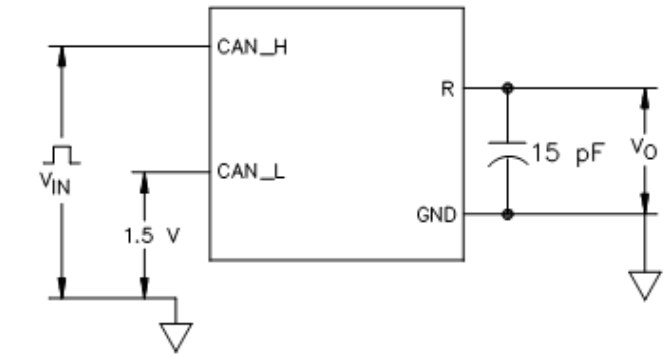


FIGURE 9. Receiver test circuit.

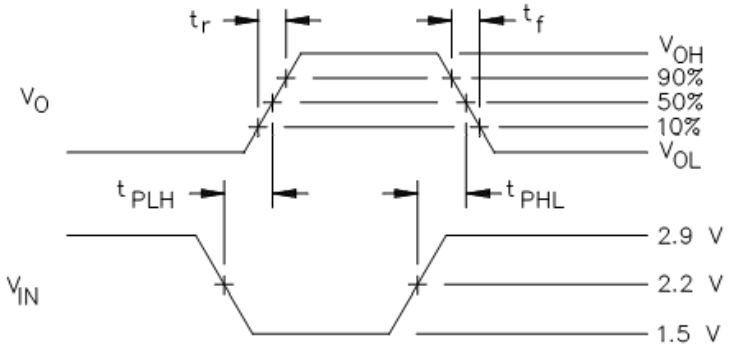
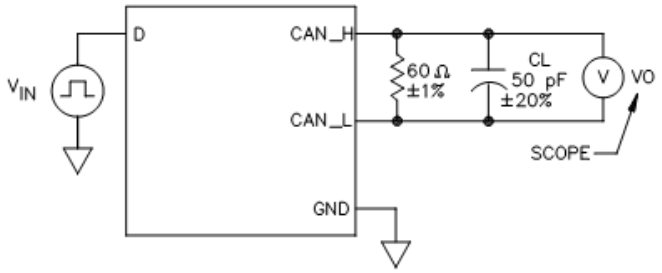


FIGURE 10. Receiver test measurement points.

Input		Output	Measured
VCANH	VCANL	R	VDIFF
-6.1 V	-7 V	L	900 mV
12 V	11.1 V	L	900 mV
-1 V	-7 V	L	6 V
12 V	6 V	L	6 V
-6.5 V	-7 V	H	500 mV
12 V	11.5 V	H	500 mV
-7 V	-1 V	H	6 V
6 V	12 V	H	6 V
Open	Open	H	X

FIGURE 11. Differential input voltage threshold test.



VIN = 125 kHz, 0 V to VCC, duty cycle 50%, tr = tf ≤ 6 ns, Zo = 50 Ω.
CL includes fixture and instrumentation capacitance.

FIGURE 12. Driver timing test circuit.

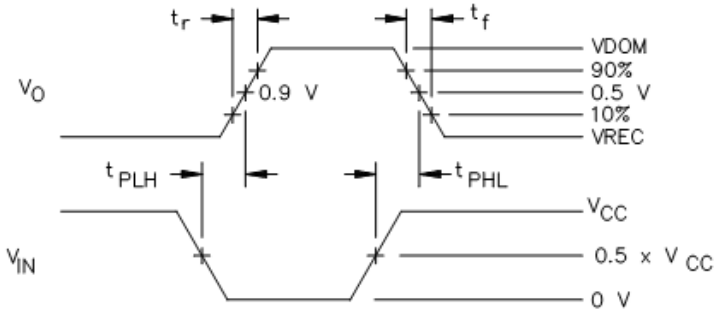


FIGURE 13. Driver timing measurement points .

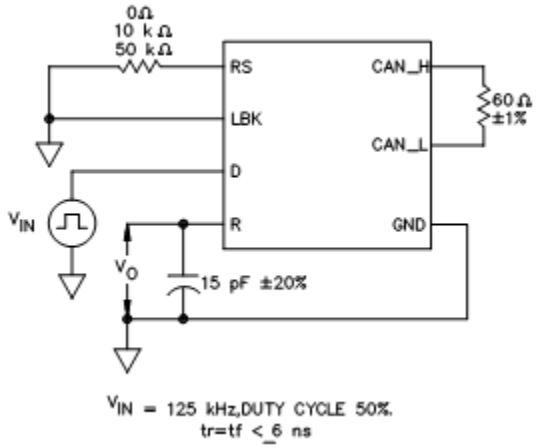


FIGURE 14. Total loop delay test circuit.

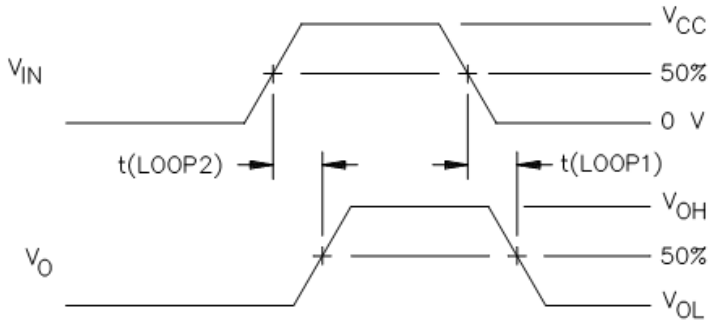
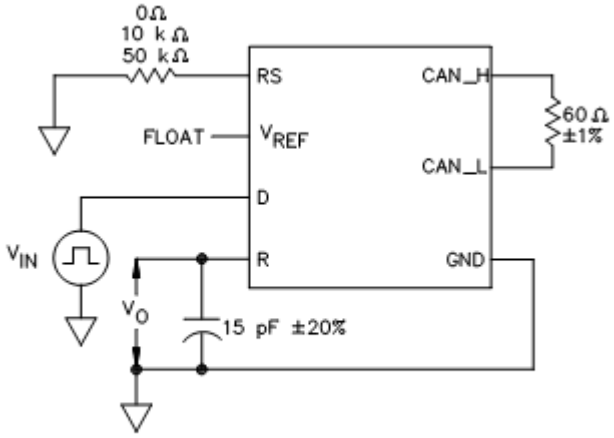


FIGURE 15. Total loop delay test measurement points.



V_{IN} = 125 kHz, duty cycle 50%, $t_r = t_f \leq 6$ ns.

FIGURE 16. Total loop delay test circuit.

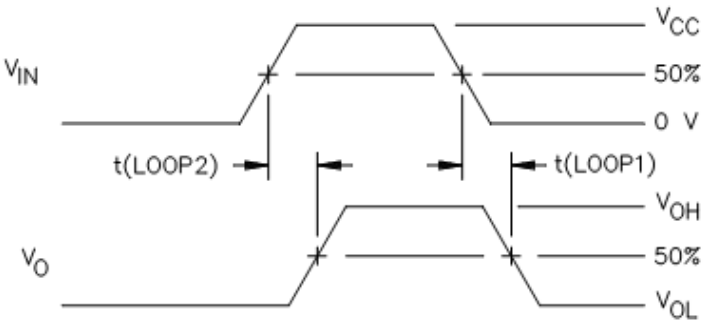
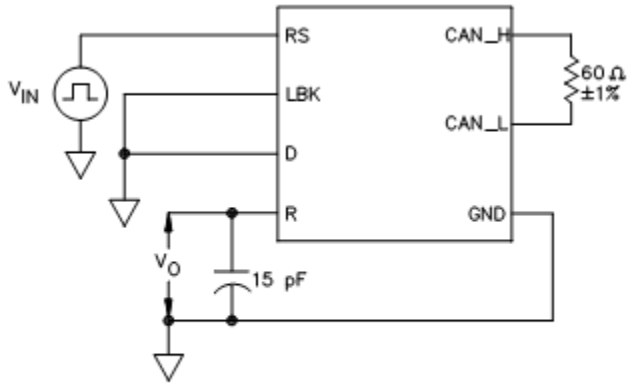
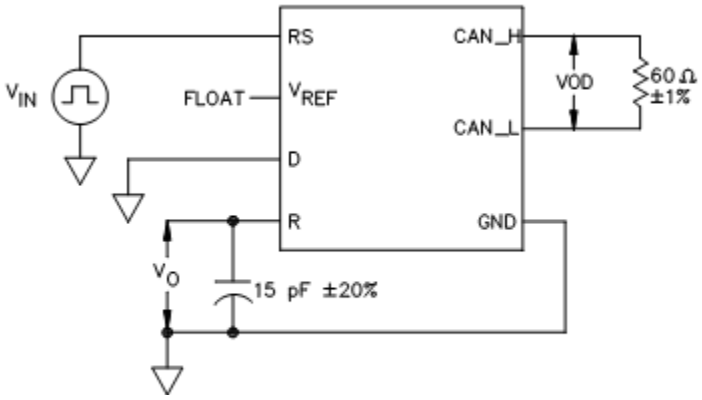


FIGURE 17. Total loop delay test measurement points.



V_{IN} = 125 kHz, duty cycle 50%, $t_r = t_f \leq 6$ ns.

FIGURE 18. Listen to valid dominant time circuit.



V_{IN} = 125 kHz, 0 V to V_S, duty cycle 50%, $t_r = t_f \leq 6$ ns.

FIGURE 19. Listen to valid dominate time circuit.

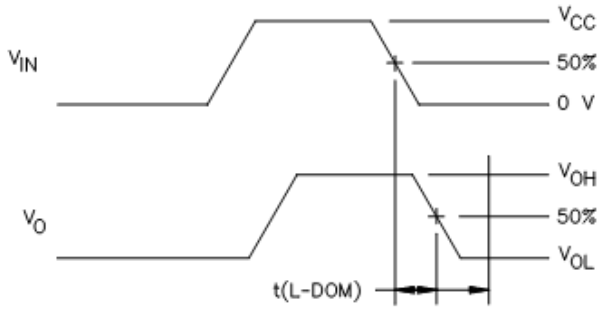
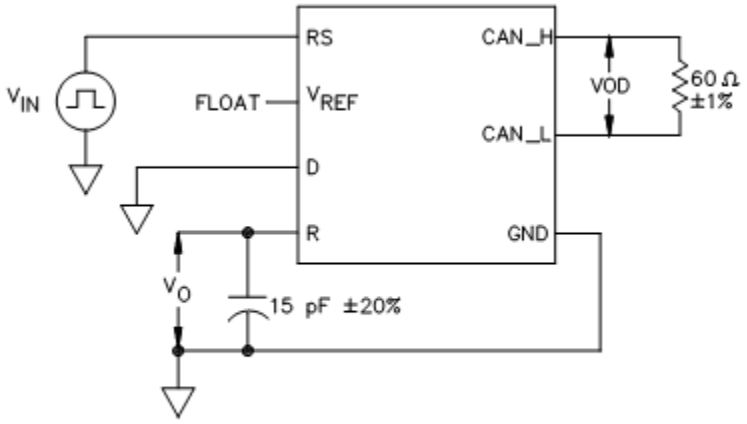


FIGURE 20. Listen to valid dominate time measurement points.



V_{IN} = 125 kHz, 0 V to V_S, duty cycle 50%, $t_r = t_f \leq 6$ ns.

FIGURE 21. Low power shutdown to dominate time circuit.

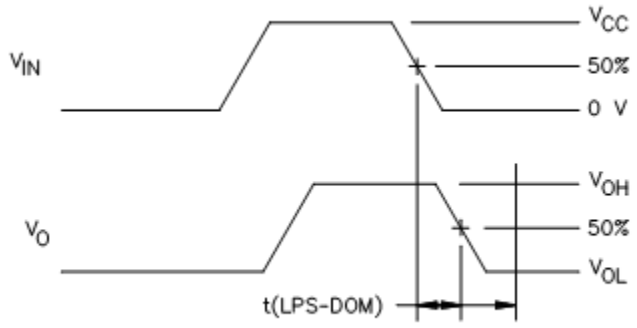
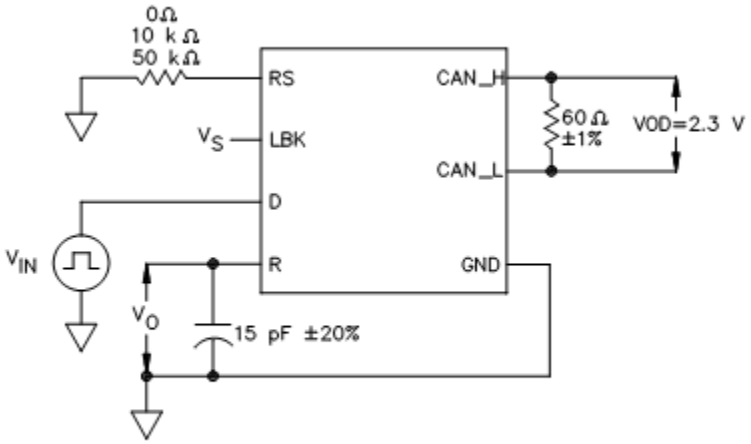


FIGURE 22. Low power shutdown to time measurement points.



V_{IN} = 125 kHz, 0 V to V_S, duty cycle 50%, $t_r = t_f \leq 6$ ns.

FIGURE 23. Loop back delay to dominant time test circuit.

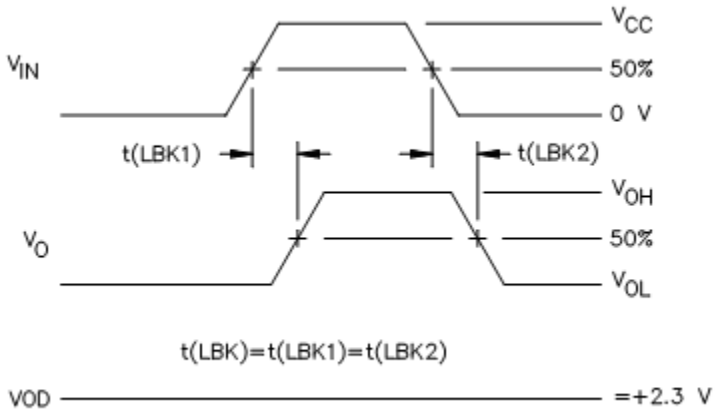


FIGURE 24. Loop back delay to dominant measurement points.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 1/ 5, 6, 9, 10, 11	1, 2, 3, 1/ 2/ 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 2/ 5, 6, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1, 9, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions V_{CC} = 3.0 V and 3.6 V	Device types	Limit
D logic input leakage	I_{IH}	D = 2.0 V	All	±3.0 µA
D logic input leakage	I_{IL}	D = 0.8 V	All	±3.0 µA
Supply current dominant	ICC(DOM)	D = LBK = RS = 0 V, no load	All	±1.0 mA
Supply current recessive	ICC(REC)	D = V_{CC}, LBK = RS = 0 V, no load	All	±0.75 µA
Receiver output high voltage	V_{OH}	I_O = -4 mA	All	±0.10 V
Receiver output low voltage	V_{OL}	I_O = +4 mA	All	±0.10 V
Dominant bus output voltage	VO(DOM)	D = 0 V, CANH = RS = 0 V	All	±0.10 V
Dominant bus output voltage	VO(DOM)	D = 0 V, CANL = RS = 0 V	All	±0.10 V
Recessive bus output voltage	VO(REC)	D = 3 V, CANH = RS = 0 V, 60 Ω, no load	All	±0.10 V
Recessive bus output voltage	VO(REC)	D = 3 V, CANL = RS = 0 V, 60 Ω, no load	All	±0.10 V

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019, condition D for device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, and condition A for device types 04, 05, 06 and 10, 11, 12 as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any process or design changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latchup (SEL).

c. Number of transients (SET).

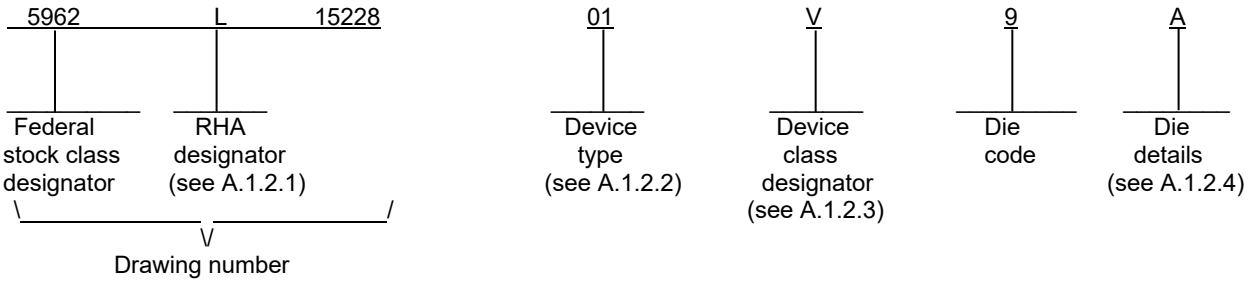
d. Occurrence of burn-out (SEB).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-15228

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL72026SEH	3.3 V can transceiver, 1 Mbps, listen mode, loopback
02	ISL72027SEH	3.3 V can transceiver, 1 Mbps, listen mode, split termination output
03	ISL72028SEH	3.3 V can transceiver, 1 Mbps, low power shutdown, split termination output
04	ISL72026BSEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
05	ISL72027BSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
06	ISL72028BSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output
07	ISL72026ASEH	3.3 V can transceiver, 1 Mbps, listen mode, loopback
08	ISL72027ASEH	3.3 V can transceiver, 1 Mbps, listen mode, split termination output

A.1.2.2 Device type(s) - continued. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
09	ISL72028ASEH	3.3 V can transceiver, 1 Mbps, low power shutdown, split termination output
10	ISL72026CSEH	Radiation hardened, 3.3 V can transceiver, 1 Mbps, listen mode, loopback
11	ISL72027CSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, listen mode, split termination output
12	ISL72028CSEH	Radiation hardened, 3.3 V can transceiver, 1Mbps, low power shutdown, split termination output

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 04, 07, 10	A-1
02, 05, 08, 11	A-2
03, 06, 09, 12	A-3

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 04, 07, 10	A-1
02, 05, 08, 11	A-2
03, 06, 09, 12	A-3

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 04, 07, 10	A-1
02, 05, 08, 11	A-2
03, 06, 09, 12	A-3

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 04, 07, 10	A-1
02, 05, 08, 11	A-2
03, 06, 09, 12	A-3

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

Device types 01, 04, 07, 10

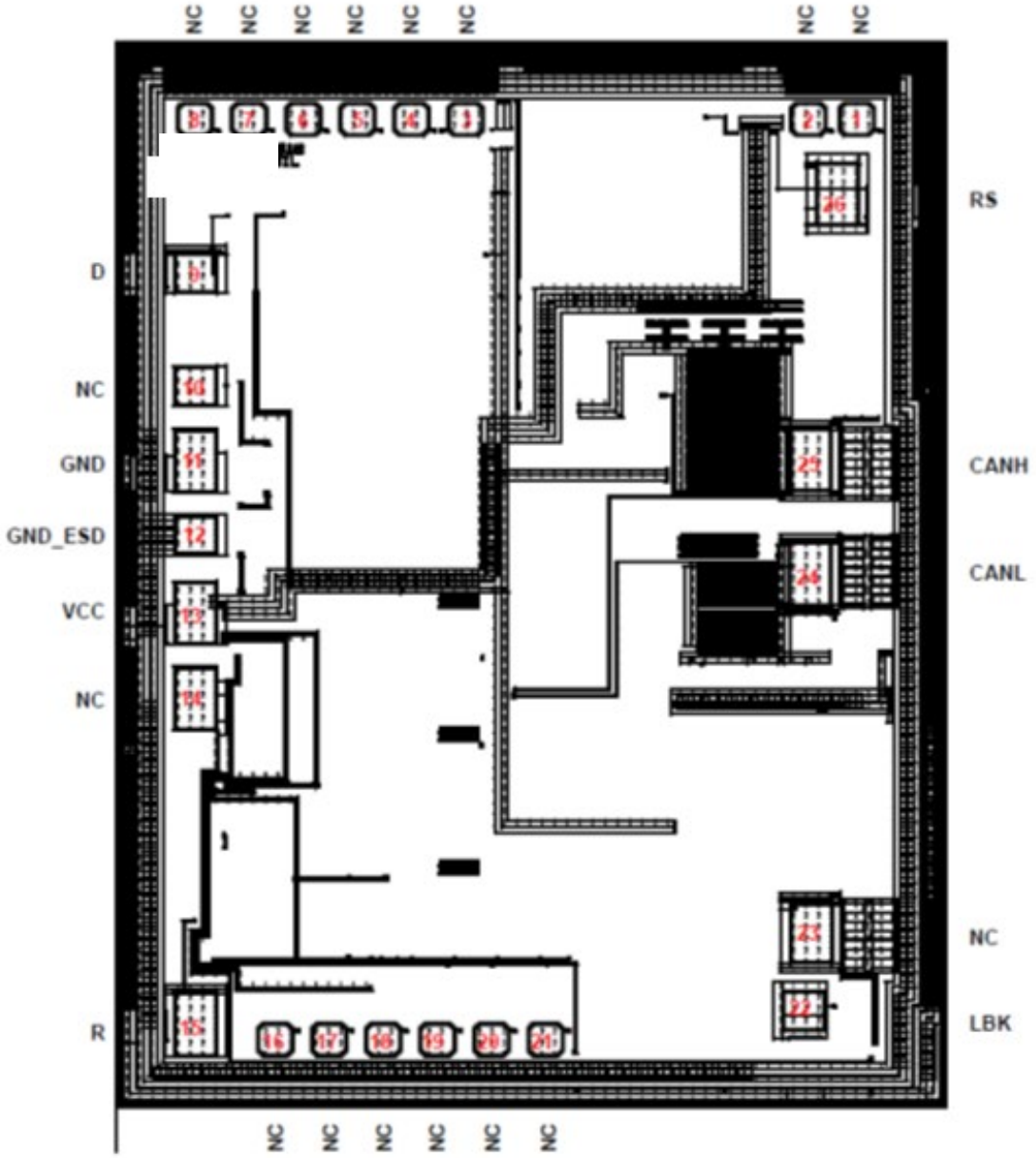


FIGURE A-1. Die bonding pad locations and electrical functions.

Device types 01, 04, 07, 10

Die layout X - Y coordinates

Pad number	Pad name	X (µm)	Y (µm)	X	Y
1	NC	90.0	90.0	901.4	1365.6
2	NC	90.0	90.0	767.4	1365.6
3	NC	90.0	90.0	-183.23	1365.6
4	NC	90.0	90.0	-333.25	1365.6
5	NC	90.0	90.0	-483.25	1365.6
6	NC	90.0	90.0	-633.25	1365.6
7	NC	90.0	90.0	-783.25	1365.6
8	NC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	NC	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	VCC	110.0	180.0	-931.1	-115.05
14	NC	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	NC	90.0	90.0	-711.1	-1394.95
17	NC	90.0	90.0	-561.1	-1394.95
18	NC	90.0	90.0	-411.1	-1394.95
19	NC	90.0	90.0	-261.1	-1394.95
20	NC	90.0	90.0	-111.1	-1394.95
21	NC	90.0	90.0	38.9	-1394.95
22	LBK	110.0	110.0	756.9	-1307.3
23	NC	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

NOTE: Origin of coordinates is the center of the die. NC = No connect

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

Device types 01, 04, 07, 10

Die physical dimensions.

Die size: 2413 microns x 3322 microns.
Die thickness: 305 microns ± 25 microns.

Interface materials.

Top metallization: 300 Å TiN on 2.8 microns AlCu
In bond pads, TiN has been removed.
Backside metallization: Silicon

Glassivation.

Type: 12 kÅ silicon nitride on 3 kÅ oxide

Substrate: P6SOI: Bonded wafer dielectrically isolated BiCMOS.

Assembly related information.

Substrate potential: Floating
Special assembly instructions: Tie GND (pad 11) and GND_ESD (pad 12) both together and to GND.
All pads identified as NC shall not be connected and shall remain floating.

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

Device types 02, 05, 08, 11

FIGURE A-2. Die bonding pad locations and electrical functions.

Device types 02, 05, 08, 11

Die layout X - Y coordinates

Pad number	Pad name	X (µm)	Y (µm)	X	Y
1	NC	90.0	90.0	901.4	1365.6
2	NC	90.0	90.0	767.4	1365.6
3	NC	90.0	90.0	-183.23	1365.6
4	NC	90.0	90.0	-333.25	1365.6
5	NC	90.0	90.0	-483.25	1365.6
6	NC	90.0	90.0	-633.25	1365.6
7	NC	90.0	90.0	-783.25	1365.6
8	NC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	NC	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	V_{CC}	110.0	180.0	-931.1	-115.05
14	VCC_VREF	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	NC	90.0	90.0	-711.1	-1394.95
17	NC	90.0	90.0	-561.1	-1394.95
18	NC	90.0	90.0	-411.1	-1394.95
19	NC	90.0	90.0	-261.1	-1394.95
20	NC	90.0	90.0	-111.1	-1394.95
21	NC	90.0	90.0	38.9	-1394.95
22	NC	110.0	110.0	756.9	-1307.3
23	V_{REF}	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

NOTE: Origin of coordinates is the ce nter of the die. NC = No connect

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

Device types 02, 05, 08, 11

Die physical dimensions.

Die size: 2413 microns x 3322 microns.
Die thickness: 305 microns ± 25 microns.

Interface materials.

Top metallization: 300 Å TiN on 2.8 microns AlCu
In bond pads, TiN has been removed.
Backside metallization: Silicon

Glassivation.

Type: 12 kÅ silicon nitride on 3 kÅ oxide

Substrate: P6SOI: Bonded wafer dielectrically isolated BiCMOS.

Assembly related information.

Substrate potential: Floating
Special assembly instructions: Tie GND (pad 11) and GND_ESD (pad 12) both together and to GND.
Tie V_{CC} (pad 13) and VCC_VREF (pad 14) both together and to V_{CC}.
All pads identified as NC shall not be connected and shall remain floating.

FIGURE A-2. Die bonding pad locations and electrical functions – continued.

Device types 03, 06, 09, 12

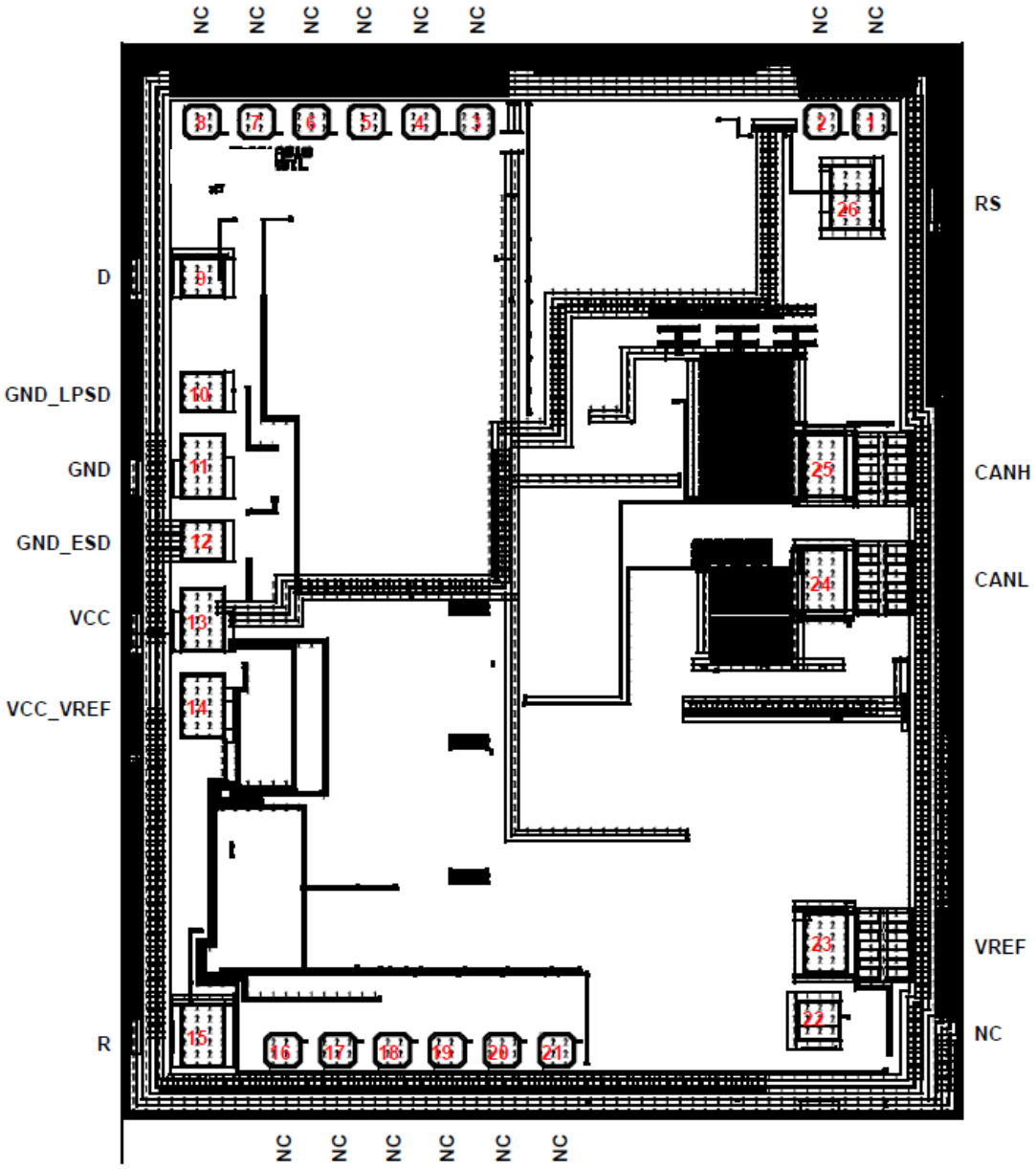


FIGURE A-3. Die bonding pad locations and electrical functions.

Device types 03, 06, 09, 12

Die layout X - Y coordinates

Pad number	Pad name	X (µm)	Y (µm)	X	Y
1	NC	90.0	90.0	901.4	1365.6
2	NC	90.0	90.0	767.4	1365.6
3	NC	90.0	90.0	-183.23	1365.6
4	NC	90.0	90.0	-333.25	1365.6
5	NC	90.0	90.0	-483.25	1365.6
6	NC	90.0	90.0	-633.25	1365.6
7	NC	90.0	90.0	-783.25	1365.6
8	NC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	GND_LSPD	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	V_{CC}	110.0	180.0	-931.1	-115.05
14	VCC_VREF	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	NC	90.0	90.0	-711.1	-1394.95
17	NC	90.0	90.0	-561.1	-1394.95
18	NC	90.0	90.0	-411.1	-1394.95
19	NC	90.0	90.0	-261.1	-1394.95
20	NC	90.0	90.0	-111.1	-1394.95
21	NC	90.0	90.0	38.9	-1394.95
22	NC	110.0	110.0	756.9	-1307.3
23	V_{REF}	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

NOTE: Origin of coordinates is the center of the die. NC = No connect

FIGURE A-3. Die bonding pad locations and electrical functions - continued.

Device types 03, 06, 09, 12

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2413 microns x 3322 microns.
Die thickness: 305 microns ± 25 microns.

Interface materials.
Top metallization: 300 Å TiN on 2.8 microns AlCu
In bond pads, TiN has been removed.
Backside metallization: Silicon

Glassivation.
Type: 12 kÅ silicon nitride on 3 kÅ oxide

Substrate: P6SOI: Bonded wafer dielectrically isolated BiCMOS.

Assembly related information.
Substrate potential: Floating
Special assembly instructions: Tie GND_LPSD (pad 10) and GND (pad 11) and GND_ESD (pad 12) all together and to GND.
Tie V_{CC} (pad 13) and VCC_VREF (pad 14) both together and to V_{CC}.
All pads identified as NC shall not be connected and shall remain floating.

FIGURE A-3. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-02-01

Approved sources of supply for SMD 5962-15228 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L1522801VXC	34371	ISL72026SEHVF
5962L1522801V9A	34371	ISL72026SEHVX
5962L1522802VXC	34371	ISL72027SEHVF
5962L1522802V9A	34371	ISL72027SEHVX
5962L1522803VXC	34371	ISL72028SEHVF
5962L1522803V9A	34371	ISL72028SEHVX
5962R1522804VXC	34371	ISL72026BSEHVF
5962R1522804V9A	34371	ISL72026BSEHVX
5962R1522805VXC	34371	ISL72027BSEHVF
5962R1522805V9A	34371	ISL72027BSEHVX
5962R1522806VXC	34371	ISL72028BSEHVF
5962R1522806V9A	34371	ISL72028BSEHVX
5962L1522807VXC	34371	ISL72026ASEHVF
5962L1522807V9A	34371	ISL72026ASEHVX
5962L1522808VXC	34371	ISL72027ASEHVF
5962L1522808V9A	34371	ISL72027ASEHVX
5962L1522809VXC	34371	ISL72028ASEHVF
5962L1522809V9A	34371	ISL72028ASEHVX
5962R1522810VXC	34371	ISL72026CSEHVF
5962R1522810V9A	34371	ISL72026CSEHVX

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1522811VXC	34371	ISL72027CSEHVF
5962R1522811V9A	34371	ISL72027CSEHVX
5962R1522812VXC	34371	ISL72028CSEHVF
5962R1522812V9A	34371	ISL72028CSEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406