REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to footnote 3/ as specified under paragraph 1.3. Make change to footnote 3/ as specified under TABLE IB. - ro	15-02-10	C. SAFFLE
B	Add device type 02. Make change to the PVINx, AV_{DD}, DV_{DD} voltage under paragraph 1.4. Make clarifications to LX, PVIN, and PGND terminal symbols under FIGURE 2 by deleting "x" and assigning actual numbers.- ro	16-04-01	C. SAFFLE
C	Make correction to the Standby supply current test condition column by deleting "GND" with "1" in all four places in TABLE IA. - ro	19-10-29	J. ESCHMEYER

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
14-03-13

REVISION LEVEL
C

MICROCIRCUIT, LINEAR, SYNCHRONOUS BUCK REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-14203**

SHEET 1 OF 31

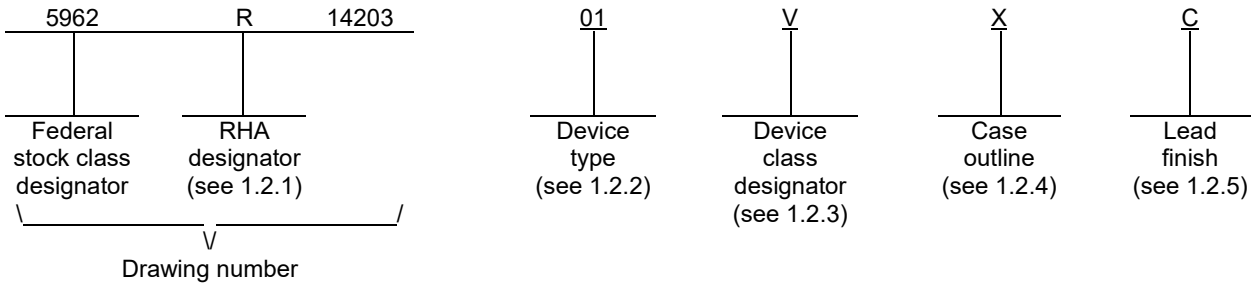
DSCC FORM 2233
APR 97

5962-E011-20

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70003SEH	Radiation hardened 3 V to 13.2 V, 6 A, synchronous buck regulator
02	ISL70003ASEH	Radiation hardened 3 V to 13.2 V, 9 A, synchronous buck regulator with enhanced high current load regulation

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	64	Quad flat pack
Y	See figure 1	64	Quad flat pack with heat sink

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Switch node connections (LXx), Power supply inputs (PVINx)	PGNDx – 0.3 V to PGNDx + 16 V
LXx, PVINx	PGNDx – 0.3 V to PGNDx + 14.7 V 2/
LXx, PVINx	PGNDx – 0.3 V to PGNDx + 13.7 V 3/
Analog voltage supply (AV_{DD}) – Analog ground (AGND), Digital voltage supply (DV_{DD}) – Digital ground (DGND)	PVINx – PGNDx ± 0.3 V
Analog output reference (V_{REFA})	GNDA – 0.3 V to GNDA + 5.5 V
Digital output reference (V_{REFD}), Output reference (VREF_OUTS)	GNDD – 0.3 V to GNDD + 5.5 V
Signal pins	GNDA – 0.3 V to V_{REFA} + 0.3 V 4/
Digital control pins	GNDD – 0.3 V to V_{REFD} + 0.3 V 5/
Soft start input (SS)	DGND – 0.3 V to DGND + 2.5 V
Power good output (PGOOD)	GNDD – 0.3 V to DVDD
Resistor to V_{IN} (RT) / capacitor to GND (CT)	GNDD – 0.3 V to DVDD
Power dissipation (P_D):	
Case outline X:	
T_A = +25°C	3.67 W
T_A = +125°C	0.73 W
T_C = +25°C	83.3 W
T_C = +125°C	16.6 W
Case outline Y:	
T_A = +25°C	7.34 W
T_A = +125°C	1.46 W
T_C = +25°C	178.5 W
T_C = +125°C	35.6 W
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+260°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-ambient (θ_{JA}) :	
Case outline X	34°C/W 6/
Case outline Y	17°C/W 7/
Thermal resistance, junction-to-case (θ_{JC}) :	
Case outline X	1.5°C/W 8/
Case outline Y	0.7°C/W 9/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For operation in a heavy ion environment at LET = 86.4 MeV/mg/cm^2 at T_C = +125°C and sourcing 7 A load current.

3/ For operation in a heavy ion environment at LET = 86.4 MeV/mg/cm^2 at T_C = +125°C and with a negative inductor valley current.

4/ POR_VIN, FB, NI, VERR, OCSETA, OCSETB, BUFOUT, BUFIN-, BUFIN+, IMON and REF pins.

5/ FSEL, EN, SYNC, SEL1, SEL2, and DE pins.

6/ θ_{JA} is measured in free air with the component mounted on a low effective thermal conductivity test board.

7/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features.

8/ For θ_{JC}, the case temperature location is the center of the package underside.

9/ For θ_{JC}, the case temperature location is the center of the exposed metal heatsink on the package underside.

1.4 Recommended operating conditions.

PVINx, AV_{DD}, DV_{DD}	3.0 V to 13.2 V
Operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 10/
Maximum total dose available (dose rate ≤ 0.01 rads(Si)/s)	50 krads(Si) 10/

Single event phenomena (SEP):

No SEL observed at effective linear energy transfer (LET) (see 4.4.4.4)	≤ 86 MeV/(mg/cm^2) 11/
No SEB observed at effective LET (fluence = 6.0 x 10^7 ions/cm^2)	< 86 MeV/(mg/cm^2) 11/
No SET observed resulting in > ± 6% ΔV_{OUT} with 3 V input and 1.8 V output at effective LET	< 86 MeV/(mg/cm^2) 11/
No SET observed resulting in > ± 3% ΔV_{OUT} with 13.2 V input and 3.3 V output at effective LET	< 86 MeV/(mg/cm^2) 11/
No SEFI observed with 13.2 V input and 3.3 V output at linear energy transfer (LET)	≤ 86 MeV/(mg/cm^2) 11/
No SEFI observed with 5.5 V input and 1.8 V output at linear energy transfer (LET)	≤ 86 MeV/(mg/cm^2) 11/
No SEFI observed with 3 V input and 1.8 V output at linear energy transfer (LET)	≤ 60 MeV/(mg/cm^2) 11/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

10/ The device types 01 and 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

11/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP/SEE characteristics but, are not production tested unless specified by the customer through the purchase order or contract. For more information on destructive SEE (SEB/SEGR) test results, customers are requested to contact manufacturer.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and .

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply section.							
Operating supply current	IOP	PVINx = 13.2 V, FSEL = 1	1,2,3	01, 02		125	mA
		PVINx = 13.2 V, FSEL = 0				125	
		PVINx = 3.0 V, FSEL = 1				60	
		PVINx = 3.0 V, FSEL = 0				60	
Standby supply current	ISBY	PVINx = 13.2 V, FSEL = 1, SEL1 = SEL2 = 1	1,2,3	01, 02		30	mA
		PVINx = 13.2 V, FSEL = 0, SEL1 = SEL2 = 1				30	
		PVINx = 3.0 V, FSEL = 1, SEL1 = SEL2 = 1				15	
		PVINx = 3.0 V, FSEL = 0, SEL1 = SEL2 = 1				15	
Shutdown supply current	ISDN	PVINx = 13.2 V, EN = GND	1,2,3	01, 02		3	mA
		PVINx = 3.0 V, EN = GND				1	
Linear regulators.							
Output voltage	VO	AV_{DD}, DV_{DD} = 13.2 V	1,2,3	01, 02	4.5	5.5	V
Current limit	CL	AV_{DD}, DV_{DD} = 13.2 V	1,2,3	01, 02	50	190	mA
Power-on reset (POR).							
POR pin input voltage	PORThr		1,2,3	01, 02	0.56	0.64	V
POR sink current	PORIsk		1,2,3	01, 02	9.6	14.4	µA
Enable.							
Enable V_{IH} voltage	EnVIH		1,2,3	01, 02	2		V
Enable V_{IL} voltage	EnVIL		1,2,3	01, 02		0.8	V
Enable (EN) leakage	EnIIH	EN = 4.5 V	1,2,3	01, 02		10	µA
Select phase.							
SEL 1,2 V_{IH} voltage	SELVIH		1,2,3	01, 02	2		V
SEL 1,2 V_{IL} voltage	SELVIL		1,2,3	01, 02		0.8	V
SEL 1,2 leakage current	SELIIH	SEL1,2 = V_{REFD}	1,2,3	01, 02		10	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse width modulator (PWM) control logic.							
Switching frequency	OSC	FSEL = 1	9,10,11	01, 02	255	345	kHz
		FSEL = 0			425	575	
Minimum on time 3/	t_{ON}	SS = GND	9,10,11	01, 02		320	ns
Minimum on time 3/	t_{ON1}		9,10,11	01, 02		220	ns
Minimum off time 3/	t_{OFF}		9,10,11	01, 02		270	ns
External synchronization frequency range	OSCsyn	FSEL = 1, PVINx = 3.0 V	9,10,11	01, 02		345	kHz
		FSEL = 0, PVINx = 3.0 V				575	
SYNC V_{IH} voltage	$SYNV_{IH}$		1,2,3	01, 02	2		V
SYNC V_{IL} voltage	$SYNV_{IL}$		1,2,3	01, 02		0.8	V
Synchronization input leakage current	$SYNI_{IH}$	SYNC = VREFD	1,2,3	01, 02		4	µA
Soft start.							
Soft-start source current	ISSRC	SS = GND	1,2,3	01, 02	20	27	µA
Soft-start discharge on-resistance	SSRES		1,2,3	01, 02		6	Ω
Reference voltage.							
Reference voltage tolerance	$V_{REF} + V_{IO}$	V_{REF} + Error amplifier V_{IO}	1,2,3	01, 02	0.594	0.606	V
Error amplifier.							
Maximum output voltage	EAO	V_{IN} = 5.5 V	1,2,3	01, 02	3.5		V
Feedback (FB) input leakage current	EAFB	VFB = 0.6 V, PVINx = 13.2 V	1,2,3	01, 02		250	nA
Offset voltage	V_{IO}		1,2,3	01, 02	-3	3	mV
Power blocks.							
Upper device rDS(ON)	URON	PVINx = 3.0 V	4,5,6	01, 02	170	700	mΩ
		PVINx = 5.5 V			120	600	
Lower device rDS(ON)	LRON	PVINx = 3.0 V	4,5,6	01, 02	90	455	mΩ
		PVINx = 5.5 V			60	425	
LXx output leakage	LX_{LKG}	EN = LXx = GND, single LXx output	1,2,3	01, 02		3	µA
		EN = GND, LXx = PVINx, single LXx output				3	
Deadtime 3/	t_{DEAD}	Within a single power block or between power blocks	9,10,11	01, 02	4		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power-good signal.							
Rising threshold	PGOOVTH	VFB as a % of V_{REF}	1,2,3	01, 02	107	115	%
Rising hysteresis	PGOOVHYS	VFB as a % of V_{REF}	1,2,3	01, 02	2	5	%
Falling threshold	PGOUVTH	VFB as a % of V_{REF}	1,2,3	01, 02	85	93	%
Falling hysteresis	PGOUVHYS	VFB as a % of V_{REF}	1,2,3	01, 02	2	5	%
Power-good drive	PGDRV	PVIN = 3 V, PGOOD = 0.4 V, EN = GND	1,2,3	01, 02	7.2		mA
Power-good leakage	PGLKG	PVIN = PGOOD = 13.2 V	1,2,3	01, 02		1	µA
Protection features.							
Undervoltage protection.							
Undervoltage trip threshold	UVTRIP	VFB as a % of V_{REF}, test mode	1,2,3	01, 02	71	79	%
Undervoltage recovery threshold	UVREC	VFB as a % of V_{REF}, test mode	1,2,3	01, 02	86	94	%
Overcurrent protection.							
Overcurrent accuracy	OCACC	ROCSETA,B = 6 kΩ (IOC = 0.6A/LX) V_{IN} = 12 V	1,2,3	01, 02	0.43	0.77	A/LX
Buffer amplifier.							
Source current capability	BUFISC		1,2,3	01, 02		20	mA
Sink current capability	BUFISK		1,2,3	01, 02	250		µA
Offset voltage	BUFVIO		1,2,3	01, 02	-4	4	mV
IMON current monitor.							
IMON Sense Time	IMONST		9,10,11	01, 02	145	300	ns
IMON Gain Accuracy	IMONGA	I_{LOAD} = 1 A/LXx, LXx off time > 300 ns	1,2,3	01, 02	86	114	µA

1/ Unless otherwise specified, $V_{IN} = AV_{DD} = DV_{DD} = PVINx = EN = 3$ V - 13.2 V; GND = AGND = DGND = PGNDx = GNDx = 0 V; POR_VIN = FB = 0.65 V; SYNC = LXx = open circuit; PGOOD is pulled up to VREFD with a 3 kΩ resistor; REF is bypassed to GND with a 220 nF capacitor; SS is bypassed to GND with a 100 nF capacitor; I_{OUT} = 0 A.

2/ RHA devices supplied to this drawing meet levels M, D, P, L, and R of irradiation for condition A and levels M, D, P, and L for condition D. However, devices are only tested at the R level in accordance with MIL-STD-883, method 1019, condition A and the L level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).
When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

3/ Limits established by characterization or analysis and are not production tested or characterized over radiation.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP/SEE	Temperature (T_C)	V_{IN}	Effective linear energy transfer (LET)	Fluence / cross section
01, 02	No SEL	+125°C	14.7 V	≤ 86 MeV/(mg/cm^2)	3/
	No SEB	+125°C	14.7 V	≤ 86 MeV/(mg/cm^2)	4/
	No SEB	+125°C	13.7 V	≤ 86 MeV/(mg/cm^2)	5/
	SET observed	+25°C	13.2 V	= 86 MeV/(mg/cm^2)	6/
	SET observed	+25°C	3.0 V	= 86 MeV/(mg/cm^2)	7/
	No SEFI	+25°C	13.2 V	= 86 MeV/(mg/cm^2)	Cross section: $< 1.30 \times 10^{-8}$ cm^2 8/
	No SEFI	+25°C	5.5 V	= 86 MeV/(mg/cm^2)	Cross section: $< 2.50 \times 10^{-8}$ cm^2 9/
	SEFI	+25°C	3.0 V	= 86 MeV/(mg/cm^2)	Cross section: $= 5.50 \times 10^{-7}$ cm^2 10/
	No SEFI	+25°C	3.0 V	= 60 MeV/(mg/cm^2)	Cross section: $< 2.5 \times 10^{-8}$ cm^2 11/

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.
2/ All test conditions using a minimum of 4 units unless otherwise noted.
3/ V_{OUT} = 3.3 V, I_{OUT} = 7 A, fluence = 2 X10^7 ions/cm^2.
V_{OUT} = 3.3 V, no negative valley current, fluence = 2 X10^7 ions/cm^2.
4/ V_{OUT} = 3.3 V, I_{OUT} = 7 A, fluence = 2 X10^7 ions/cm^2.
5/ V_{OUT} = 3.3 V, I_{OUT} = -4 A, fluence = 2 X10^7 ions/cm^2.
6/ V_{OUT} = 3.3 V, I_{OUT} = 3 A/part, fluence = 4.0 X10^7 ions/cm^2. SET no more than 1 LX pulse perturbation before correction, with a $\Delta V_{OUT} < 3\%$.
7/ V_{OUT} = 1.8 V, I_{OUT} = 3 A/part, fluence = 4.0 X10^7 ions/cm^2. SET no more than 1 LX pulse perturbation before correction, with a $\Delta V_{OUT} < 6\%$.
8/ No SEFI events observed at surface LET = 86 MeV/mg/cm^2, V_{OUT} = 3.3 V, I_{OUT} = 3 A/part, V_{IN} = 13.2 V and cross section $< 1.30 \times 10^{-8}$cm^2 . (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)
9/ No SEFI events observed at surface LET = 86 MeV/mg/cm^2, V_{OUT} = 1.8 V, I_{OUT} = 3 A/part, V_{IN} = 5.5 V and cross section $< 2.50 \times 10^{-8}$ions/cm^2 . (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)
10/ SEFI events observed at surface LET = 86 MeV/mg/cm^2, V_{OUT} = 1.8 V, I_{OUT} = 3 A/part, V_{IN} = 3.0 V and cross section = 5.50×10^{-7}ions/cm^2 . (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)
11/ No SEFI events observed at surface LET = 60 MeV/mg/cm^2, V_{OUT} = 1.8 V, I_{OUT} = 3 A/part, V_{IN} = 3.0 V and cross section $< 2.5 \times 10^{-8}$ ions/cm^2 . (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)

Case X

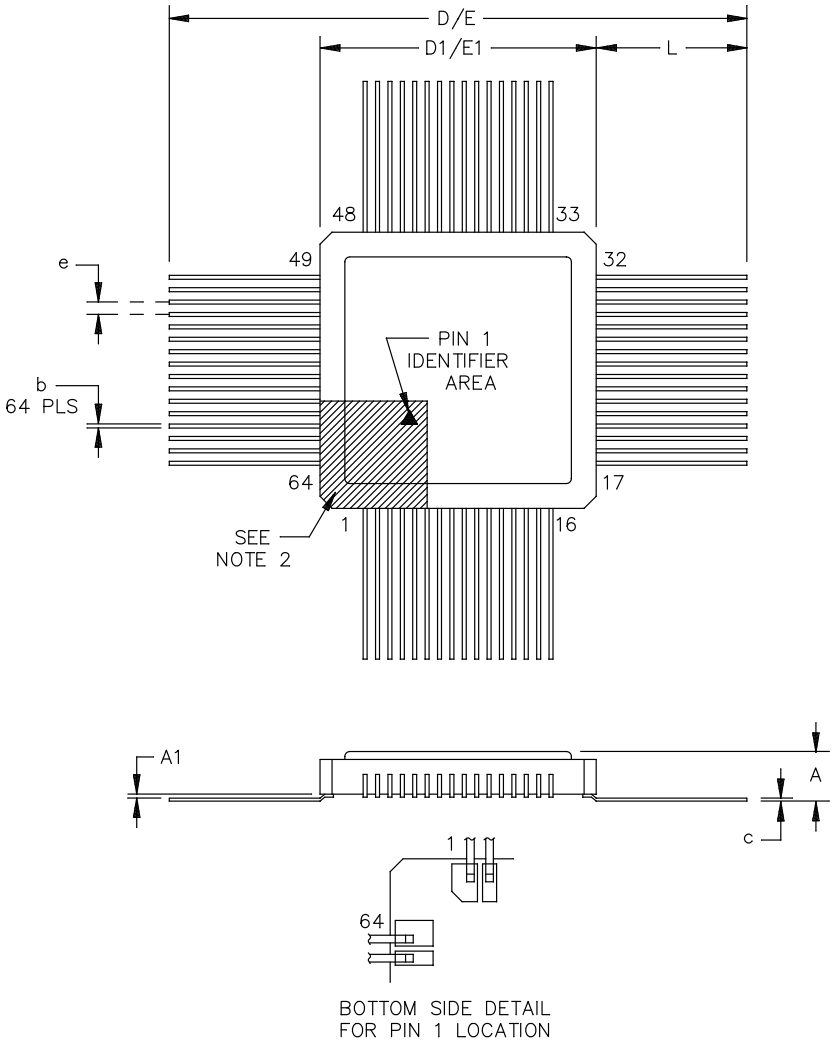


FIGURE 1. Case outlines.

Case X – continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.075	0.105	1.91	2.67	
A1	0.008 REF		0.20 REF		
b	0.006	0.010	0.15	0.25	
c	0.005	0.0075	0.125	0.188	
D	1.080	1.118	27.43	28.40	
D1	0.547	0.567	13.90	14.40	
E	1.080	1.118	27.43	28.40	
E1	0.547	0.567	13.90	14.40	
e	0.025 BSC		0.635 BSC		
L	0.255	0.290	6.48	7.37	
N	64		64		

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Pin 1 identifier location. Pin 1 is the bottom left pin.

FIGURE 1. Case outlines – continued.

Case Y

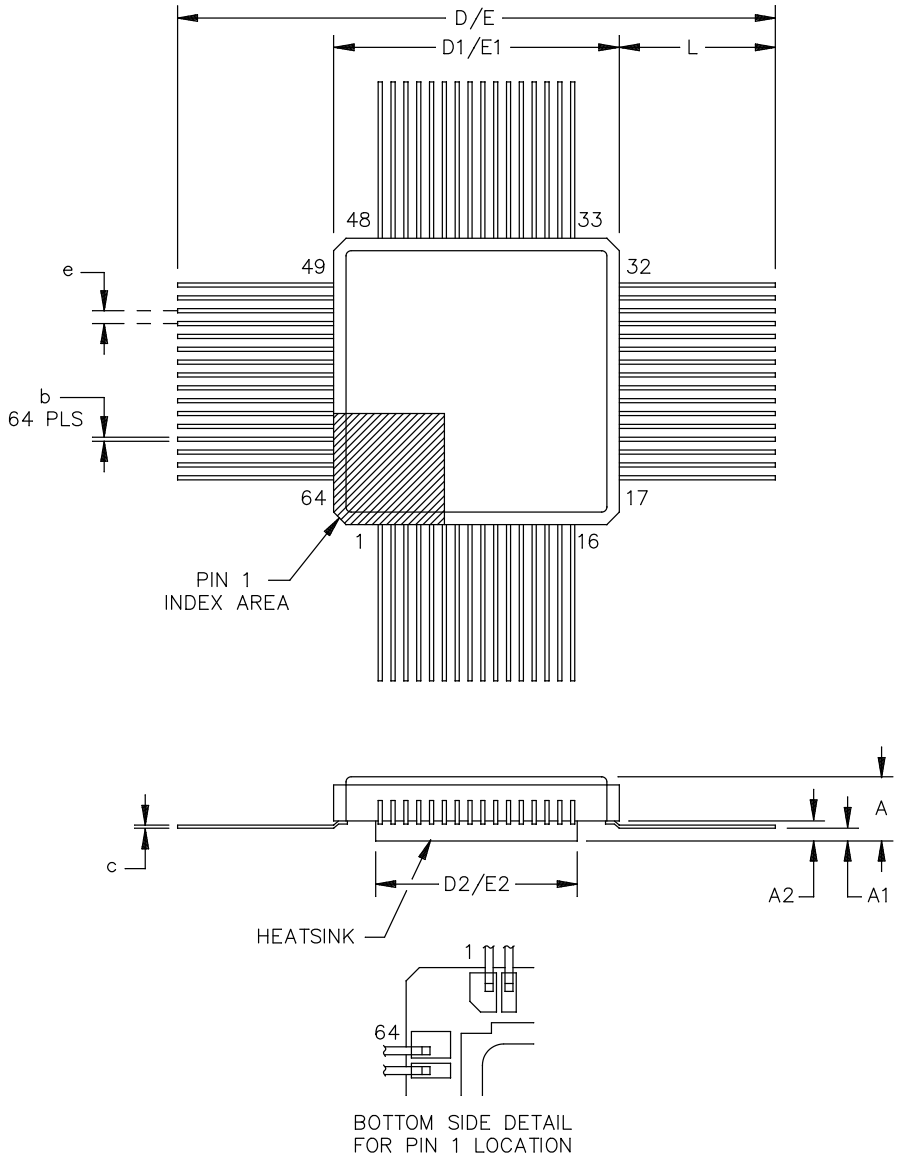


FIGURE 1. Case outlines – continued.

Case Y – continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.111	0.135	2.82	3.43	
A1	0.026	---	0.66	---	2
A2	0.048 REF		1.22 REF		
b	0.006	0.010	0.15	0.25	
c	0.005	0.0075	0.125	0.188	
D/E	1.080	1.118	27.43	28.40	
D1/E1	0.547	0.567	13.90	14.40	
D2/E2	0.395	0.405	10.03	10.29	
e	0.025 BSC		0.635 BSC		
L	0.255	0.290	6.48	7.37	
N	64		64		

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.

FIGURE 1. Case outlines – continued.

Device types	01, 02		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NI	17	GND
2	FB	18	GND
3	VERR	19	GND
4	POR_VIN	20	GND
5	V_{REFA}	21	GND
6	AV_{DD}	22	PGOOD
7	AGND	23	PVIN10
8	DGND	24	LX10
9	VREF_OUTS	25	PGND10
10	DV_{DD}	26	PGND9
11	V_{REFD}	27	LX9
12	ENABLE	28	PVIN9
13	RT/CT	29	SEL1
14	FSEL	30	SEL2
15	SYNC	31	DE
16	SS	32	PVIN8

FIGURE 2. Terminal connections.

Device types	01, 02		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
33	LX8	49	PVIN3
34	PGND8	50	NC/HS
35	PGND7	51	IMON
36	LX7	52	SGND
37	PVIN7	53	PVIN2
38	PVIN6	54	LX2
39	LX6	55	PGND2
40	PGND6	56	PGND1
41	PGND5	57	LX1
42	LX5	58	PVIN1
43	PVIN5	59	OCSETA
44	PVIN4	60	OCSETB
45	LX4	61	BUFIN+
46	PGND4	62	BUFIN-
47	PGND3	63	BUFOUT
48	LX3	64	REF

FIGURE 2. Terminal connections - continued.

Terminal symbol	Description
NI	This pin is the non-inverting input to the internal error amplifier. Connect this pin to the REF pin for normal applications or the BUFOUT pin for DDR memory power applications.
FB	This pin is the inverting input to the internal error amplifier. An external type III compensation network should be connected between this pin and the VERR pin.
VERR	This pin is the output of the internal error amplifier. An external compensation network should be connected between this pin and the FB pin.
POR_VIN	This pin is the power-on reset input to the integrated circuit. This is a comparator-type input with a rising threshold of 0.6 V and programmable hysteresis. Driving this pin above 0.6 V enables the integrated circuit. Bypass this pin to AGND with a 10 nF ceramic capacitor to mitigate SEE.
V_{REFA}	This pin is the output of the internal linear regulator and the bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 0.47 μF ceramic capacitor as close as possible to the integrated circuit.
AV_{DD}	This pin provides the supply for internal linear regulator of the device. The supply to AV_{DD} should be locally bypassed using a ceramic capacitor. Tie AV_{DD} to the PVINx pins.
AGND	This pin is the analog ground associated with the internal analog control circuitry. Connect this pin directly to the printed circuit board (PCB) ground plane.
DGND	This pin is the ground associated with the internal digital control circuitry. Connect this pin directly to the PCB ground plane.
VREF_OUTS	This pin is the output of the internal linear regulator and the supply input to the internal reference circuit. Locally filter this pin to AGND using a 0.47 μF ceramic capacitor as close as possible to the integrated circuit.
DV_{DD}	This pin provides the supply for internal linear regulator of the device. The supply to DV_{DD} should be locally bypassed using a ceramic capacitor. Tie DV_{DD} to the PVINx pin.
V_{REFD}	This pin is the output of the internal linear regulator and the bias supply input to the internal digital control circuitry. Locally filter this pin to DGND using a 0.47 μF ceramic capacitor as close as possible to the integrated circuit.
ENABLE	This pin is a logic-level enable input. Pulling this pin low powers down the chip by placing it into a very low power sleep mode
RT/CT	A resistor to V_{IN} and a capacitor to GND provide feed-forward to keep a constant modulator gain of 4.8 as V_{IN} varies.
FSEL	This pin is the oscillator frequency select input. Tie this pin to 5 V to select a 300 kHz nominal oscillator frequency. Tie this pin to the PCB ground plane to select a 500 kHz nominal oscillator frequency.
SYNC	This pin is the frequency synchronization input to the integrated circuit. This pin should be tied GND to free-run from the internal oscillator or connected to an external clock for external frequency synchronization.
SS	This pin is the soft-start input. Connect a ceramic capacitor from this pin to the PCB ground plane to set the soft-start ramp time in accordance with Equation 1: $t_{SS} C_{SS} V\times REF I = / SS$ (Equation 1) where: t_{SS} = soft-start output ramp time C_{SS} = soft-start capacitance V_{REF} = reference voltage (0.6 V normally) I_{SS} = soft-start charging current (23 μA normally) Soft-start time is adjustable from approximately 2 ms to 200 ms. The range of the soft-start capacitor should be 82 nF to 8.2 μF, inclusive.

FIGURE 2. Terminal connections - continued.

Terminal symbol	Description
GND	Connect this pin to the PCB ground plane
PGOOD	This pin is the power-good output. This pin is an open-drain logic output that is pulled to DGND when the output voltage is outside a ±11% normal regulation window. This pin can be pulled up to any voltage from 0 V to 13.2 V, independent of the supply voltage. A nominal 1 kΩ to 10 kΩ pull-up resistor is recommended. Bypass this pin to the PCB ground plane with a 10 nF ceramic capacitor to mitigate SEE.
PVINx (x = 1 to 10)	These pins are the power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3 V to 13.2 V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the integrated circuit.
SEL1	This pin is a logic-level disable input working in conjunction with SEL2. These pins form a two-bit logic input that set the number of active power blocks. This allows the device to be tailored to any load the application requires and achieve the highest possible efficiency.
SEL2	This pin is a logic-level disable input. Pulling this pin low inhibits pulses on the LXx outputs. See description of pin 29, SEL1, for more information.
DE	The DE pin enables or disables diode emulation. When it is HIGH, diode emulation is allowed. Otherwise, continuous conduction mode is forced.
LXx (x = 1 to 10)	These pins are the switch node connections to the internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous metal oxide semiconductor field effect transistor (MOSFET) power switches.
NC/HS	This is a no connect pin that is not connected to anything internally. For case outline Y (heatsink option) this pin is electrically connected to the heat sink on the underside of the package. Connect this pin and/or the heat sink to a thermal plane.
IMON	IMON is a current source output that is proportional to the sensed current through the regulator. Tie it to GND if not used.
SGND	This pin is connected to an internal metal trace that serves as a noise shield. Connect this pin to the PCB ground plane.
PGNDx (x = 1 to 10)	These pins are the power grounds associated with the corresponding internal power blocks. Connect these pins directly to the PCB ground plane. These pins should also connect to the negative terminals of the input and output capacitors. The package lid is internally connected to PGNDx.
OCSETA	This pin is the redundant output overcurrent set input. Connect a resistor from this pin to the PCB ground plane to set the output overcurrent threshold.
OSCETB	This pin is the primary output overcurrent set input. Connect a resistor from this pin to the PCB ground plane to set the output overcurrent threshold.
BUFIN+	This pin is the input to the internal unity gain buffer amplifier. For DDR memory power applications connect the VTT voltage to this pin.

FIGURE 2. Terminal connections - continued.

Terminal symbol	Description
BUFIN-	This pin is the inverting input to the buffer amplifier. For DDR power memory applications connect BUFOUT to this pin. Bypass this pin to the PCB ground plane with a 0.1 μF ceramic capacitor.
BUFOUT	This pin is the output of the buffer amplifier. For DDR power applications connect this pin to the reference input of the DDR memory. The buffer needs a minimum of 1.0 μF load capacitor for stability
REF	This pin is the output of the internal reference voltage. Bypass this pin to the PCB ground plane with a 220 nF ceramic capacitor located as close as possible to the integrated circuit. The bypass capacitor is needed to mitigate SEE.
HEATSINK	The heatsink is connected to device pin 50 (NC) and is electrically isolated. The heatsink should be connected to a thermal chassis of any potential for optimal thermal relief.
PACKAGE LID	For case outlines X and Y, the lid is connected to the PGNDx pins.

FIGURE 2. Terminal connections - continued.

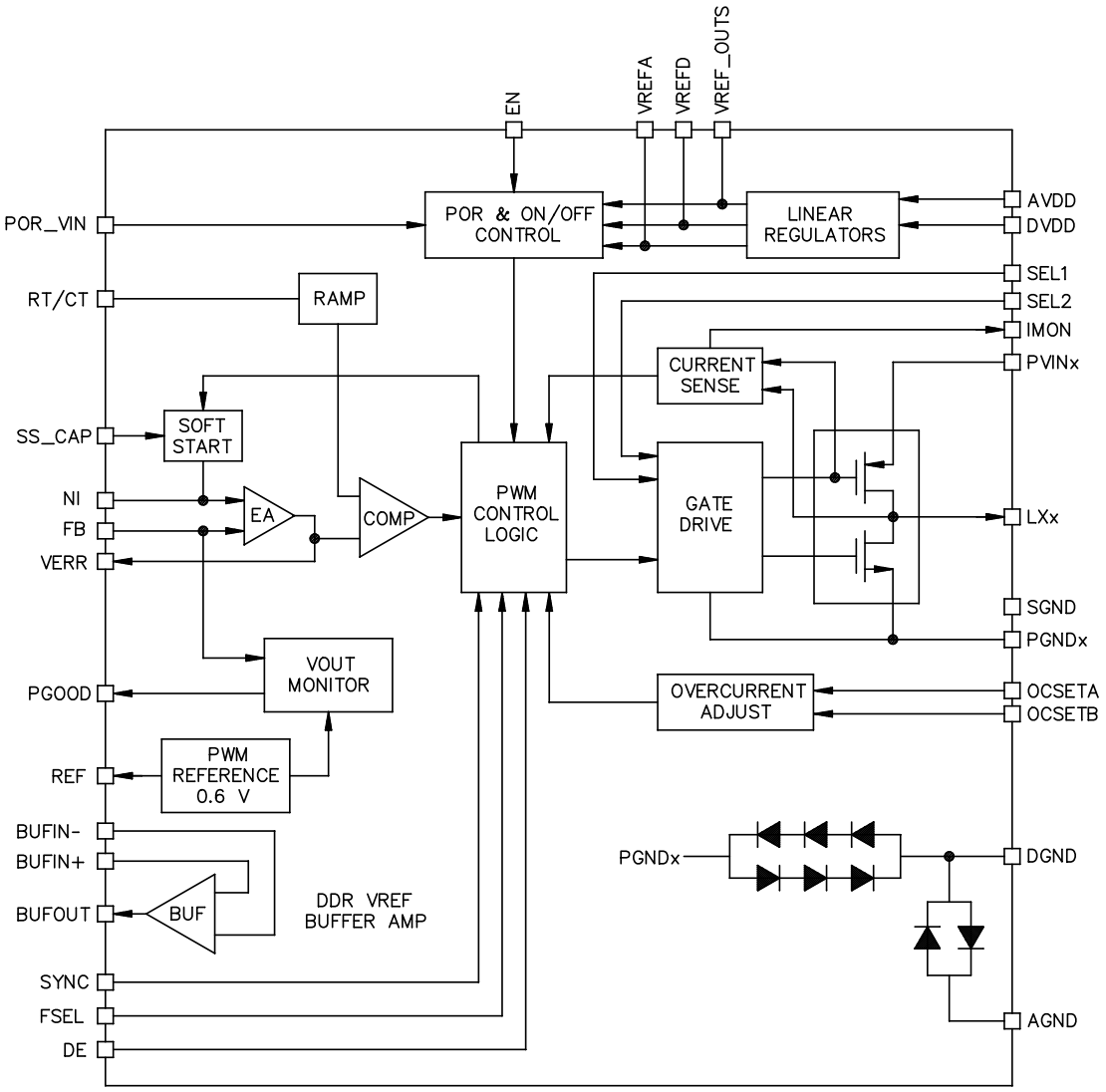


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3, 1/ 2/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and Δ.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Delta limits		Units
		Min	Max	
Shutdown supply current 13.2 V	ISDN	-0.5	+0.5	mA
Shutdown supply current 3.0 V	ISDN	-0.2	+0.2	mA
V_{REF} + error amplifier V_{IO} 13.2 V	V_{REF} + V_{IO}	-2.0	+2.0	mV
V_{REF} + error amplifier V_{IO} 3.0 V	V_{REF} + V_{IO}	-2.0	+2.0	mV
Switching frequency 500 kHz 3.0 V	OSC	-40	+40	kHz
Switching frequency 500 kHz 13.2 V	OSC	-40	+40	kHz
Switching frequency 300 kHz 3.0 V	OSC	-25	+25	kHz
Switching frequency 300 kHz 13.2 V	OSC	-25	+25	kHz
Soft-start source current 3.0 V	ISSRC	-2.5	+2.5	µA
Soft-start source current 13.2 V	ISSRC	-2.5	+2.5	µA

1/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, conditions A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be 25°C for SET. The test temperature shall be 125°C for SEB and SEL.

f. Bias conditions shall be as specified in table IB.

g. For SEL, SEB, SET, and SEFI test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Occurrence of latchup (SEL).

d. Occurrence of burnouts (SEB).

e. Number of transients (SET).

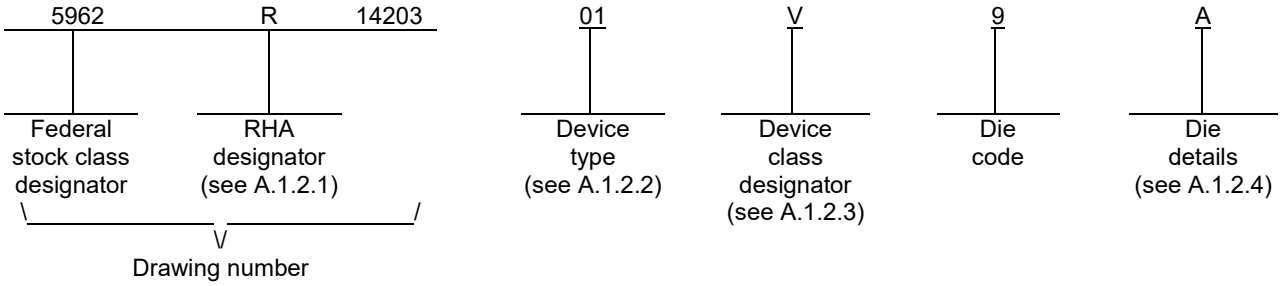
f. Number of single event functional interrupts (SEFI).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-14203

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70003SEH	Radiation hardened 3 V to 13.2 V, 6 A synchronous buck regulator
02	ISL70003ASEH	Radiation hardened 3 V to 13.2 V, 9 A synchronous buck regulator with ..enhanced high current load regulation

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

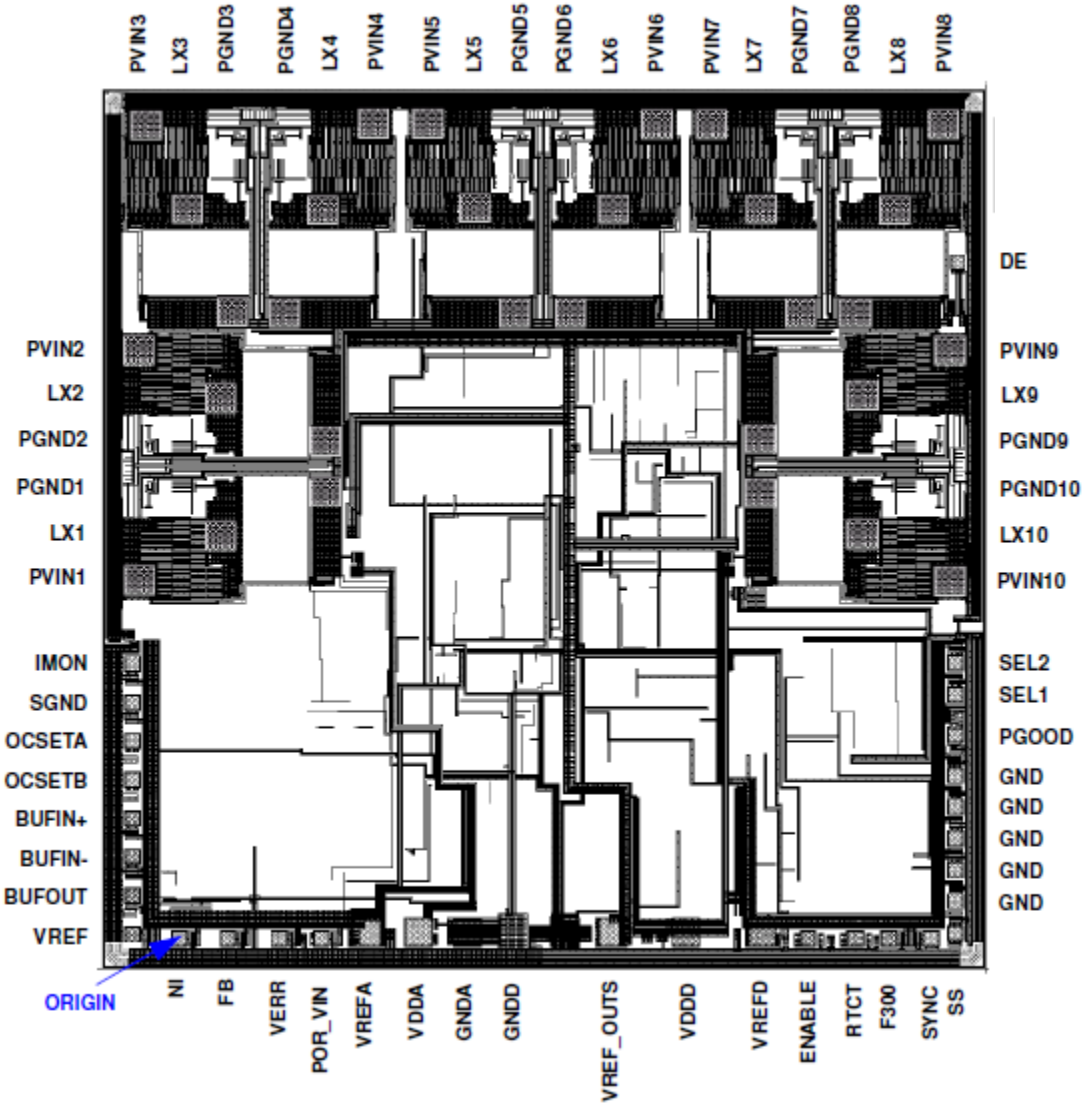


FIGURE A-1. Die bonding pad locations and electrical functions.

Pad name	Pad number	Center pad location X (μm)	Center pad location Y (μm)	Pad size dx (μm)	Pad size dy (μm)	Bond wire size (mils)
NI	1	0	0	135	135	1.5
FB	2	452	0	135	135	1.5
VERR	3	929	0	135	135	1.5
POR_VIN	4	1371	0	135	135	1.5
V_{REFA}	5	1854	58	254	254	3
AV_{DD}	6	2577	60	254	254	3
AGND	7	3104	60	254	254	3
DGND	8	3589	60	254	254	3
VREF_OUTS	9	4035	60	254	254	3
DV_{DD}	10	4713	60	254	254	3
V_{REFD}	11	5420	60	254	254	3
ENABLE	12	5846	0	135	135	1.5
RTCT	13	6274	0	135	135	1.5
F300	14	6579	0	135	135	1.5
SYNC	15	6976	0	135	135	1.5
SS CAP	16	7201	51	135	135	1.5
TDI	17	7201	345	135	135	1.5
ZAP	18	7201	639	135	135	1.5
TD0	19	7201	934	135	135	1.5
TST TRIM	20	7201	1228	135	135	1.5
TCLK	21	7201	1522	135	135	1.5
PGOOD	22	7201	1902	135	135	1.5
SEL1	23	7201	2275	135	135	1.5
SEL2	24	7201	2569	135	135	1.5
PVIN10	25	7140	3285	254	254	3

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Pad name	Pad number	Center pad location X (μm)	Center pad location Y (μm)	Pad size dx (μm)	Pad size dy (μm)	Bond wire size (mils)
LX10	26	6350	3771	254	254	3
PGND10	27	5387	4179	254	254	3
PGND9	28	5387	4625	254	254	3
LX9	29	6350	5033	254	254	3
PVIN9	30	7140	5518	254	254	3
DEON	31	7220	6303	135	135	1.5
PVIN8	32	7140	7578	254	254	3
LX8	33	6655	6788	254	254	3
PGND8	34	6247	5825	254	254	3
PGND7	35	5801	5825	254	254	3
LX7	36	5393	6788	254	254	3
PVIN7	37	4908	7578	254	254	3
PVIN6	38	4497	7578	254	254	3
LX6	39	4011	6788	254	254	3
PGND6	40	3603	5825	254	254	3
PGND5	41	3157	5825	254	254	3
LX5	42	2749	6788	254	254	3
PVIN5	43	2264	7578	254	254	3
PVIN4	44	1853	7578	254	254	3
LX4	45	1367	6788	254	254	3
PGND4	46	960	5825	254	254	3
PGND3	47	514	5825	254	254	3
LX3	48	106	6788	254	254	3
PVIN3	49	-379	7578	254	254	3
PVIN2	50	-379	5518	254	254	3

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Pad name	Pad number	Center pad location X (μm)	Center pad location Y (μm)	Pad size dx (μm)	Pad size dy (μm)	Bond wire size (mils)
LX2	51	411	5033	254	254	3
PGND2	52	1374	4625	254	254	3
PGND1	53	1374	4179	254	254	3
LX1	54	411	3771	254	254	3
PVIN1	55	-379	3285	254	254	3
IMON	56	-438	2561	135	135	1.5
SGND	57	-438	2201	135	135	1.5
OCSETA	58	-438	1841	135	135	1.5
OCSETB	59	-438	1481	135	135	1.5
BUF IN +	60	-438	1121	135	135	1.5
BUF IN -	61	-438	761	135	135	1.5
BUF OUT	62	-438	401	135	135	1.5
VREF	63	-438	41	135	135	1.5

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 8300 μm x 8300 μm (327 mils x 327 mils)
Die thickness: 300 μm ± 25.4 μm (12.0 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (0.5%)
Thickness: 2.7 μm ± 0.4 μm
Backside metallization: None

Glassivation.
Type: Silicon dioxide and silicon nitride
Thickness: 0.3 μm ±0.03 μm and 1.2 μm ±0.12 μm

Substrate: 0.6 μM BiCMOS junction isolated

Assembly related information.
Substrate potential: Ground
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-10-29

Approved sources of supply for SMD 5962-14203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1420301VXC	3/	ISL70003SEHVF
5962R1420301VYC	3/	ISL70003SEHVFE
5962R1420301V9A	3/	ISL70003SEHVX
5962R1420302VYC	34371	ISL70003ASEHVFE
5962R1420302V9A	34371	ISL70003ASEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406