REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - rrp	19-02-04	C. SAFFLE
B	Make correction to the Input bias current test, under the condition column with V_{CM} = -V_S, delete +V_S and replace -V_S as specified under Table I. - ro	20-05-07	J. ESCHMEYER
C	Make correction to PSRR test condition limits and Group A subgroups limit columns within V_S = ±2.5 V section as specified under Table IA. - ro	22-06-13	J. ESCHMEYER
D	Make updates on pages 3 and 16 to part radiation performance characteristics to reflect results of neutron testing performed by vendor CAGE 34371. - cgh	25-07-14	J. ESCHMEYER

Revision Status of Sheets

REV	D																					
SHEET	23																					
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RICK OFFICER CHECKED BY RAJESH PITHADIA APPROVED BY CHARLES F. SAFFLE DRAWING APPROVAL DATE 14-11-24	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime** MICROCIRCUIT, LINEAR, 19 MHz, 40 V, LOW POWER, DUAL OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

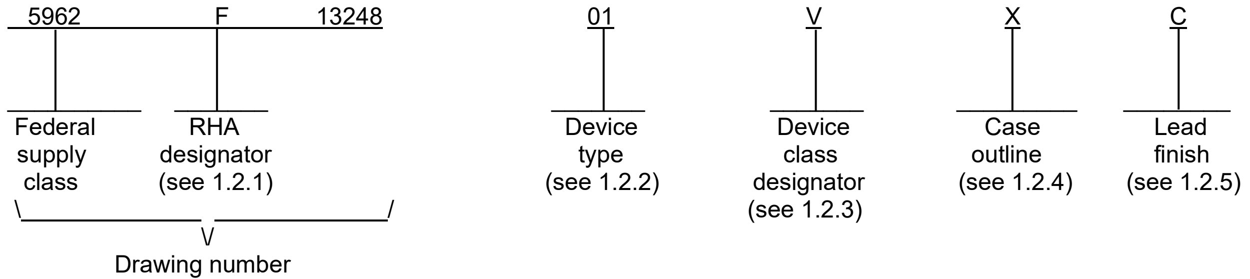
AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-13248**
		SHEET 1 OF 23		

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70244SEH	Radiation hardened, 19 MHz, 40 V, low power, dual operational amplifier
02	ISL73244SEH	Radiation hardened, 19 MHz, 40 V, low power, dual operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device type	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Device type	Descriptive designator	Terminals	Package style
X	CDFP3-F10	10	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Maximum supply voltage .... 42 V
Maximum supply voltage .... 38 V 2/
Maximum differential input current .... 20 mA
Maximum differential input voltage .... 42 V or ([$-V_S$ - 0.5] V to [$+V_S$ + 0.5] V)
Minimum/maximum input voltage .... 42 V or ([$-V_S$ - 0.5] V to [$+V_S$ + 0.5] V)
Maximum/minimum current for input voltage ($> +V_S$ or $< -V_S$) .... ±20 mA
Electrostatic discharge (ESD) ratings:
Human body model (HBM).. 2 kV
Machine model (MM) .... 200 V
Charged device model (CDM) .... 750 V
Maximum junction temperature range (T_J)... +150°C
Storage temperature range (T_{STG}) .... -65°C to +150°C
Thermal resistance, junction to case (θ_{JC}) .... 10°C/W 3/
Thermal resistance, junction to ambient (θ_{JA}) .... 44°C/W 4/

1.4 Recommended operating conditions.

Single supply voltage (V_S) .... [2.7 V ± 10%] to 39.6 V
Split rail supply voltage (V_S) .... ±1.35 V to ±19.8 V
Ambient operating temperature range (T_A) .... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s):
Device type 01 .... 300 krad(Si) 5/
Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):
Device type 01 and 02 .... 50 krad(Si) 5/ 6/
Single event phenomenon (SEP):
No Single event latch-up (SEL) occurs at effective LET (see 4.4.4.2) .... ≤ 86 MeV/(mg/cm^2) 7/
No Single event burnout (SEB) occurs at effective LET (see 4.4.4.2) .... ≤ 86 MeV/(mg/cm^2) 7/
Single event transient (SET) observed that resulted in a recovery
time not exceeding 5 µs with effective LET (see 4.4.4.2) .... 60 MeV/(mg/cm^2) 7/
Neutron irradiation Displacement Damage (DD) test (1 MeV equivalent)............ 2 x 10^{12} neutron/cm^2 7/

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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Tested in a heavy ion environment at LET = 86.4 MeV/(mg/cm^2) at 125°C (T_C) for single event burnout.

3/ For θ_{JC}, the “case temperature” location is the center of the package underside.

4/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.

5/ For device type 01, total irradiation dose (TID) is performed at high dose rate and low dose rate condition A and condition D as specified in MIL-STD-883, method 1019. Radiation end point limits for the noted parameters are guaranteed only for condition A to a maximum TID level of 300 krad(Si), and condition D to a maximum TID level of 50 krad(Si).

6/ For device type 02, total irradiation dose (TID) is performed at low dose rate condition D as specified in MIL-STD-883, method 1019. Radiation end point limits for the noted parameters are guaranteed only for condition D to a maximum TID level of 50 krad(Si).

7/ For SEE and Neutron displacement damage test, devices are characterized at initial qualification and after any design or process changes which may affect the SEP or Neutron electrical parametric limit. However, when specified in the purchase order or contract, SEP and Neutron test shall be performed during production lot test. See manufacturer’s SEE or neutron test report for more information.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 19.8$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	V_{OS}	V_{CM} = 0 V	1	01, 02	-400	400	µV
		V_{CM} = $+V_S$ to $-V_S$	1, 2, 3		-500	500	
		V_{CM} = $+V_S$ to $-V_S$, M, D, P, L, R, F 2/	1		-500	500	
Input offset channel to channel match	ΔV_{OS}	V_{CM} = $+V_S$	1, 2, 3	01, 02		800	µV
		V_{CM} = $+V_S$, M, D, P, L, R, F 2/	1				
		V_{CM} = $-V_S$	1, 2, 3			800	
		V_{CM} = $-V_S$, M, D, P, L, R, F 2/	1				
Input bias current	I_B	V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V)	1, 2, 3	01, 02	-500	500	nA
		V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V), M, D, P, L, R, F 2/	1		-500	500	
		V_{CM} = $-V_S$, ($-V_S$ + 0.5 V)	1, 2, 3		-650	650	
		V_{CM} = $-V_S$, ($-V_S$ + 0.5 V), M, D, P, L, R, F 2/	1		-650	650	
Input offset current	I_{OS}	V_{CM} = $+V_S$ to $-V_S$	1	01, 02	-30	30	nA
			2, 3		-50	50	
		V_{CM} = $+V_S$ to $-V_S$, M, D, P, L, R, F 2/	1		-50	50	
Common mode input voltage range	V_{CMIR}		1, 2, 3	01, 02	$-V_S$	$+V_S$	V
		M, D, P, L, R, F 2/	1				
Common mode rejection ratio	CMRR	V_{CM} = $-V_S$ to $+V_S$	1, 2, 3	01, 02	70		dB
		V_{CM} = $-V_S$ to $+V_S$, M, D, P, L, R, F 2/	1				
		V_{CM} = ($+V_S$ - 0.5 V) to ($-V_S$ + 0.5 V)	1, 2, 3		80		
		V_{CM} = ($+V_S$ - 0.5 V) to ($-V_S$ + 0.5 V), M, D, P, L, R, F 2/	1				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 19.8$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	PSRR	$-V_S$ = -18 V, $+V_S$ = 0.5 V to 18 V, $+V_S$ = 18 V, $-V_S$ = -0.5 V to -18 V	1, 2, 3	01, 02	83		dB
		$-V_S$ = -18 V, $+V_S$ = 0.5 V to 18 V, $+V_S$ = 18 V, $-V_S$ = -0.5 V to -18 V, M, D, P, L, R, F 2/	1				
Open loop gain	A_{VOL}	R_L = 10 kΩ to ground	1, 2, 3	01, 02	90		dB
		R_L = 10 kΩ to ground, M, D, P, L, R, F 2/	1				
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1, 2, 3	01, 02		160	mV
		R_L = no load, M, D, P, L, R, F 2/	1				
		R_L = 10 kΩ	1, 2, 3			175	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1				
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1, 2, 3	01, 02		160	mV
		R_L = no load, M, D, P, L, R, F 2/	1			160	
		R_L = 10 kΩ	1, 2, 3			175	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1			175	
Output short circuit current	I_{SC}	Sourcing: V_{OUT} = -18 V, V_{IN} = 0 V	1, 2, 3	01, 02		-10	mA
		Sourcing: V_{OUT} = -18 V, V_{IN} = 0 V, M, D, P, L, R, F 2/	1				
		Sinking: V_{OUT} = +18 V, V_{IN} = 0 V	1, 2, 3		10		
		Sinking: V_{OUT} = +18 V, V_{IN} = 0 V, M, D, P, L, R, F 2/	1				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 19.8$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current/amplifier	I_S	Unity gain	1	01, 02		2.2	mA
			2, 3			2.8	
		Unity gain, M, D, P, L, R, F 2/	1			2.2	
Large signal slew rate	SR	$A_V = 1$, $R_L = 10$ kΩ, $V_O = 10$ V_{PP}	4. 5. 6	01, 02	60		V/µs
		$A_V = 1$, $R_L = 10$ kΩ, $V_O = 10$ V_{PP}, M, D, P, L, R, F 2/	4		60		
Gain bandwidth product	GBWP	$R_L = 10$ kΩ 3/	4, 5, 6	01, 02	17		MHz
		$R_L = 10$ kΩ, 3/ M, D, P, L, R, F 2/	4		17		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 2.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	V_{OS}	V_{CM} = 0 V	1	01, 02	-400	400	µV
		$V_{CM} = +V_S$ to $-V_S$	1, 2, 3		-500	500	
		$V_{CM} = +V_S$ to $-V_S$, M, D, P, L, R, F 2/	1		-500	500	
Input offset channel to channel match	ΔV_{OS}	$V_{CM} = +V_S$	1, 2, 3	01, 02		800	µV
		$V_{CM} = +V_S$, M, D, P, L, R, F 2/	1				
		$V_{CM} = -V_S$	1, 2, 3			800	
		$V_{CM} = -V_S$, M, D, P, L, R, F 2/	1				
Input bias current	I_B	V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V)	1, 2, 3	01, 02	-400	400	nA
		V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V), M, D, P, L, R, F 2/	1		-400	400	
		$V_{CM} = -V_S$, ($-V_S$ + 0.5 V)	1, 2, 3		-580	580	
		$V_{CM} = -V_S$, ($-V_S$ + 0.5 V), M, D, P, L, R, F 2/	1		-580	580	
Input offset current	I_{OS}	$V_{CM} = +V_S$ to $-V_S$	1	01, 02	-30	30	nA
			2, 3		-50	50	
		$V_{CM} = +V_S$ to $-V_S$, M, D, P, L, R, F 2/	1		-50	50	
Common mode input voltage range	V_{CMIR}		1, 2, 3	01, 02	$-V_S$	$+V_S$	V
		M, D, P, L, R, F 2/	1				
Common mode rejection ratio	CMRR	$V_{CM} = -V_S$ to $+V_S$	1, 2, 3	01, 02	70		dB
		M, D, P, L, R, F 2/	1				
		V_{CM} = ($+V_S$ - 0.5 V) to ($-V_S$ + 0.5 V)	1, 2, 3		74		
		V_{CM} = ($+V_S$ - 0.5 V) to ($-V_S$ + 0.5 V), M, D, P, L, R, F 2/	1				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 2.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	PSRR	$-V_S$ = -2.5 V, $+V_S$ = 2.5 V to 4.5 V, $+V_S$ = 2.5 V, $-V_S$ = -2.5 V to -4.5 V	1, 2	01, 02	80		dB
			3		70		
		$-V_S$ = -2.5 V, $+V_S$ = 2.5 V to 4.5 V, $+V_S$ = 2.5 V, $-V_S$ = -2.5 V to -4.5 V, M, D, P, L, R, F 2/	1		80		
Open loop gain	A_{VOL}	R_L = 10 kΩ to ground	1, 3	01, 02	90		dB
			2		80		
		R_L = 10 kΩ to ground, M, D, P, L, R, F 2/	1		90		
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1, 2, 3	01, 02		85	mV
		R_L = no load, M, D, P, L, R, F 2/	1				
		R_L = 10 kΩ	1, 2, 3			105	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1				
		R_L = 600 Ω	1, 2, 3			400	
		R_L = 600 Ω, M, D, P, L, R, F 2/	1				
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1, 2, 3	01, 02		85	mV
		R_L = no load, M, D, P, L, R, F 2/	1				
		R_L = 10 kΩ	1, 2, 3			105	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1				
		R_L = 600 Ω	1, 2, 3			400	
		R_L = 600 Ω, M, D, P, L, R, F 2/	1				
Supply current/amplifier	I_S	Unity gain	1	01, 02		1.5	mA
			2, 3			2.0	
		Unity gain, M, D, P, L, R, F 2/	1			1.5	
Gain bandwidth product	GBWP	R_L = 10 kΩ 3/	4, 5, 6	01, 02	15		MHz
		R_L = 10 kΩ, 3/ M, D, P, L, R, F 2/	4		15		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 1.35$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage.	V_{OS}	V_{CM} = 0 V	1	01, 02	-400	400	µV
		$V_{CM} = +V_S$ to $-V_S$	1, 2, 3		-500	500	
		M, D, P, L, R, F 2/	1		-500	500	
Input offset channel to channel match	ΔV_{OS}	$V_{CM} = +V_S$	1, 2, 3	01, 02		800	µV
		$V_{CM} = +V_S$, M, D, P, L, R, F 2/	1				
		$V_{CM} = -V_S$	1, 2, 3			800	
		$V_{CM} = -V_S$, M, D, P, L, R, F 2/	1				
Input bias current	I_B	V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V)	1, 2, 3	01, 02	-375	375	nA
		V_{CM} = 0 V, $+V_S$, ($+V_S$ - 0.5 V), M, D, P, L, R, F 2/	1		-375	375	
		$V_{CM} = +V_S$, ($-V_S$ + 0.5 V)	1, 2, 3		-565	565	
		$V_{CM} = +V_S$, ($-V_S$ + 0.5 V), M, D, P, L, R, F 2/	1		-565	565	
Input offset current	I_{OS}	$V_{CM} = +V_S$ to $-V_S$	1	01, 02	-30	30	nA
			2, 3		-50	50	
		$V_{CM} = +V_S$ to $-V_S$, M, D, P, L, R, F 2/	1		-50	50	
Common mode input voltage range	V_{CMIR}		1, 2, 3	01, 02	$-V_S$	$+V_S$	V
		M, D, P, L, R, F 2/	1				
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1, 2, 3	01, 02		50	mV
		R_L = no load, M, D, P, L, R, F 2/	1			50	
		R_L = 10 kΩ	1, 2, 3			70	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1			70	
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1, 2, 3	01, 02		50	mV
		R_L = no load, M, D, P, L, R, F 2/	1			50	
		R_L = 10 kΩ	1, 2, 3			70	
		R_L = 10 kΩ, M, D, P, L, R, F 2/	1			70	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 1.35$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current/amplifier	I_S	Unit gain	1	01, 02		1.5	mA
			2, 3			2.0	
		Unity gain, M, D, P, L, R, F 2/	1			1.5	
Gain bandwidth product	GBWP	$R_L = 10$ kΩ 3/	4, 5, 6	01, 02	10		MHz
		$R_L = 10$ kΩ, 3/ M, D, P, L, R, F 2/	4		10		

1/ Unless otherwise specified, $V_{CM} = V_O = 0$ V and R_L = open.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and levels M, D, P, and L for condition D. However, device type 01 is only tested at the “F” level in accordance with MIL-STD-883, method 1019, condition A to TID level 300 krad(Si) and condition D to TID level 50 krad(Si) (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 02 is only tested at the “L” level in accordance with MIL-STD-883, method 1019, condition D to TID level 50 krad(Si) (see 1.5 herein).

Devices supplied to this drawing are only radiation tested for the parameters referencing this footnote.
Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

3/ Compliance to limits is assured by characterization and/or design.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP	Temperature (T_A)	Effective linear energy transfer (LET)
01, 02	No SEL	125°C	≤ 86 MeV/(mg/cm^2)
	No SEB	125°C	≤ 86 MeV/(mg/cm^2)
	SET observed 4/	25°C	60 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer’s SEE test report for more information.

4/ Single event transients (SET) observed that resulted in a recovery time not exceeding 5 µs with effective LET = 60 MeV/(mg/cm^2).

Device type	01, 02	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUT_A	Amplifier A output
2	$-IN_A$	Amplifier A inverting input
3	$+IN_A$	Amplifier A non-inverting input
4	NC	No internal connection
5	$-V_S$	Negative power supply
6	NC	No internal connection, tied to metal lid.
7	$+IN_B$	Amplifier B non-inverting input
8	$-IN_B$	Amplifier B inverting input
9	OUT_B	Amplifier B output
10	$+V_S$	Positive power supply
Metal lid	NONE	Unbiased, tied to package pin 6.

FIGURE 1. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.
.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4	1, 4
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6 1/	1, 2, 3, 4, 5, 6 1/ 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6 2/
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	1, 4	1, 4

1/ PDA applies to subgroup 1 for device class Q and subgroup 1 and Δ for device class V.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and life test delta parameters. (T_A = +25°C). 1/

Parameters	Symbol	Min	Max	Units
Offset voltage	V_{OS}	-125	125	μV
Input bias current	I_B	-75	75	nA
Supply current / amplifier	I_S	-350	350	μA

1/ Deltas are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C ±10% for SEL and SEB.

f. For SEB test limits, see table IB herein.

4.4.4.3 Neutron testing. When specified in the purchase order or contract, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ± 5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of burnouts (SEB).

c. Number of latch-up (SEL).

d. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-13248

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:

```
  5962         F        13248         01          V          9          A
   |           |                      |           |          |          |
Federal       RHA                   Device      Device      Die        Die
supply     designator                type        class      code     details
 class    (see A.1.2.1)          (see A.1.2.2) designator         (see A.1.2.4)
                                              (see A.1.2.3)
\_______________ _______________/
                V
         Drawing number
```

A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70244SEH	Radiation hardened, 19 MHz, 40 V, low power, dual operational amplifier
02	ISL73244SEH	Radiation hardened, 19 MHz, 40 V, low power, dual operational amplifier

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

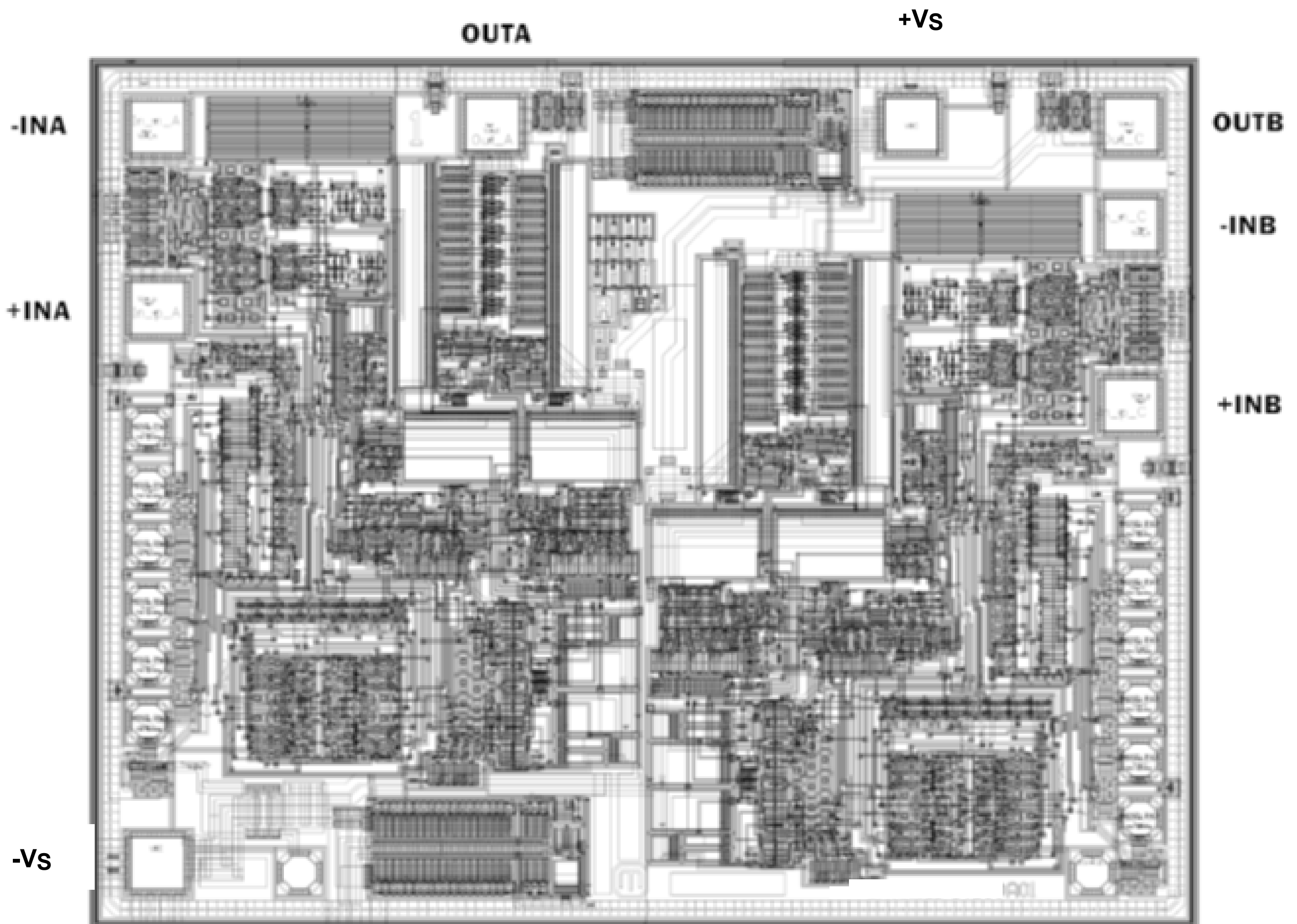

FIGURE A-1. Die bonding pad locations and electrical functions.

Pad name	Pad	X (µm)	Y (µm)	DX (µm)	DY(µm)	Bond wires per pad
OUTB	1	1015.5	664.0	110	110	1
$+V_S$	2	557.0	664.0	110	110	1
OUTA	3	-317.0	664.0	110	110	1
-INA	4	-1015.5	658.0	110	110	1
+INA	5	-1015.5	270.5	110	110	1
$-V_S$	12	-1015.5	-918.0	110	110	1
+INB	21	1015.5	62.0	110	110	1
-INB	22	1015.5	449.5	110	110	1

Note: Origin of coordinates is the centroid of die.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2410 µm (95 mils) Y = 1961 µm (77 mils)
Die thickness: 483 µm ± 25 µm (19 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5%/0.5%)
Thickness: 15 kÅ
Backside metallization: Bare Silicon

Glassivation.
Type: Nitrox
Thickness: 15 kÅ

Substrate: PR40 process: Bonded wafer dielectrically isolated complementary bipolar.

Assembly related information.
Substrate potential: Floating
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 25-07-14

Approved sources of supply for SMD 5962-13248 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1324801VXC	34371	ISL70244SEHVF
5962F1324801V9A	34371	ISL70244SEHVX
5962L1324802VXC	34371	ISL73244SEHVF
5962L1324802V9A	34371	ISL73244SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.