REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Make changes to 1.2.2, 1.5, Table IA, Table IB, figure 2, 4.4.4.1, A.1.2.2, A.1.2.4, figure A-1. Add paragraph A.1.5. - ro	12-04-02	C. SAFFLE
B	Add case outline Y. Under paragraph 1.3, make changes to footnote 2/ and add a footnote for θ_{JA} limits. Under figure 1, case outline X, delete the last sentence from note 2. Make changes to case outline X A1, E1, and L dimensions as specified under figure 1. Delete EIA/JEDEC and device class M references. - ro	13-08-22	C. SAFFLE
C	Make change to the OCPTH calculation under footnote 4/ as specified in paragraph 1.4. - ro	14-01-21	C. SAFFLE
D	Add device types 03 and 04. - ro	18-03-05	C. SAFFLE

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
11-12-12

REVISION LEVEL
D

MICROCIRCUIT, BiCMOS, LINEAR, LOW DROPOUT REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-11212**

SHEET 1 OF 26

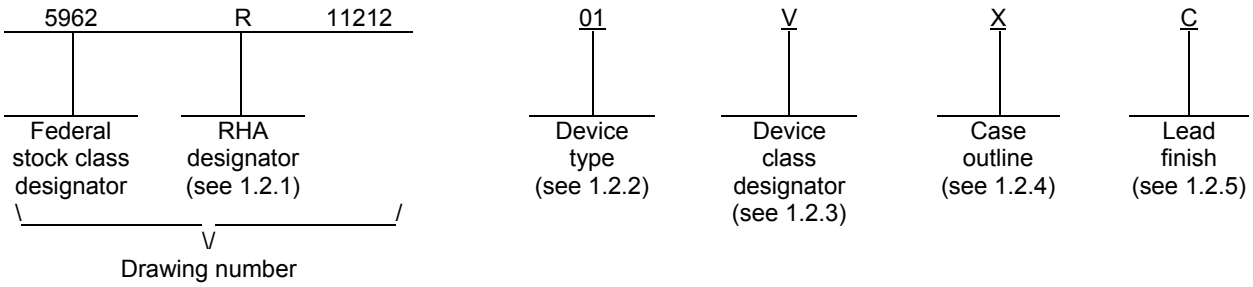
DSCC FORM 2233
APR 97

5962-E579-17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL75051SRH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
02	ISL75051SEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
03	ISL75051ASEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
04	ISL73051ASEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	18	Ceramic metal seal flat pack
Y	See figure 1	18	Ceramic metal seal flat pack with bottom metal

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Input voltage (V_{IN}) relative to GND	-0.3 V to +6.7 V
Output voltage (V_{OUT}) relative to GND	-0.3 V to +6.7 V
PG, EN, OCP/ADJ pins, relative to GND	-0.3 V dc to +6.7 V dc
Power dissipation (P_D) :	
Case outline X	4.46 W
Case outline Y	5.21 W
Maximum junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) :	
Case outline X	4°C/W 2/
Case outline Y	3.3°C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA}) :	
Case outline X	28°C/W 3/
Case outline Y	24°C/W 3/

1.4 Recommended operating conditions.

Input voltage (V_{IN}) relative to GND	2.2 V to +6.0 V
Output voltage (V_{OUT}) range	0.8 V to +5.0 V
PG, EN, OCP/ADJ pins, relative to GND	0 V to +6.0 V
OCP (over current protection) range	0.5 A to 8.5 A 4/
Junction temperature (T_J)	+150°C
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For θ_{JC}, the "case temperature" location is the center of the package underside.

3/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.

4/ The OCP pin allows the short circuit output limit threshold to be programmed by means of a resistor from the OCP pin to GND. The resistor sets the constant current threshold for the output under fault conditions. The calculation for determining OCPTH is as follows. OCPTH = 4.1115 X ROCP - 0.75.
OCPTH = over current threshold in amps. ROCP = OCP resistor in kΩ.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 r(Si)/s):
Device type 01 ..... 100 krad(Si) 5/
Device type 02 and 03 ..... 100 krad(Si) 6/
Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):
Device type 02, 03, and 04 ..... 50 krad(Si) 6/ 7/
Single event phenomenon (SEP) features:
No Single event latchup (SEL) occurs at effective LET (see 4.4.4.2) ..... ≤ 86 MeV/(mg/cm^2) 8/ 9/
No Single event burnout (SEB) occur at effective LET (see 4.4.4.2) ..... ≤ 86 MeV/(mg/cm^2) 8/ 9/
Single event transient (SET) observed
(ΔV_{OUT} within ±5%) at effective LET (see 4.4.4.2) ..... ≤ 86 MeV/(mg/cm^2) 8/ 9/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

5/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krad(Si).

6/ Device types 02 and 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krad(Si), and condition D to a maximum total dose of 50 krad(Si).

7/ Device type 04 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 50 krad(Si).

8/ SEP tests performed with capacitance of 220 µF for C_{IN} and C_{OUT}, 200 nF used for bypass capacitor. SEB and SEL tests done on a stand alone open loop configuration. For SEL, no latch up requiring manual intervention was observed. SET tests done in a closed loop configuration. The (ΔV_{OUT}) was measured across bulk capacitor of the application.

9/ Limits are characterized at initial qualification and after any design or process changes which may affect the upset or latchup characteristics but, not production tested unless specified by the customer through the purchase order or contract.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC characteristics section.							
DC output voltage accuracy	V_{OUT}	V_{OUT} resistor adjust to: 0.52 V, 1.5 V and 1.8 V, 2.2 V < V_{IN} < 3.6 V, 0 A < I_{LOAD} < 3.0 A	1,2,3	01, 02, 03, 04	-1.5	1.5	%
		V_{OUT} resistor adjust to: 5.0 V, V_{OUT} + 0.4 V < V_{IN} < 6.0 V, 0 A < I_{LOAD} < 3.0 A			-1.5	1.5	
Feedback pin	V_{ADJ}	2.2 V < V_{IN} < 6.0 V, I_{LOAD} = 0 A	1,2,3	01, 02, 03, 04	514.8	525.2	mV
DC input line regulation		2.2 V < V_{IN} < 3.6 V, V_{OUT} = 1.5 V	1,3	01, 02, 03, 04		3.5	mV
			2			8.0	
		2.2 V < V_{IN} < 3.6 V, V_{OUT} = 1.8 V	1,3			3.5	
			2			10.5	
		V_{OUT} + 0.4 V < V_{IN} < 6.0 V, V_{OUT} = 5.0 V	1,2,3			20	
DC output load regulation		V_{OUT} = 1.5 V, 0 A < I_{LOAD} < 3.0 A, V_{IN} = V_{OUT} + 0.4 V	1,2,3	01, 02, 03, 04	-4.0	-0.1	mV
		V_{OUT} = 1.8 V, 0 A < I_{LOAD} < 3.0 A, V_{IN} = V_{OUT} + 0.4 V		01, 02	-4.0	-0.05	
				03, 04	-4.8	-0.05	
		V_{OUT} = 5.0 V, 0 A < I_{LOAD} < 3.0 A, V_{IN} = V_{OUT} + 0.4 V		01, 02, 03, 04	-15.0	-0.05	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC characteristics section - continued.							
Feedback input current		V_{ADJ} = 0.5 V	1,2,3	01, 02, 03, 04		1	µA
Ground pin current	I_Q	V_{OUT} = 1.5 V, I_{LOAD} = 0 A, V_{IN} = 2.2 V	1,2,3	01, 02		12	mA
				03, 04		13	
		V_{OUT} = 5.0 V, I_{LOAD} = 0 A, V_{IN} = 6.0 V		01, 02		18	
				03, 04		19	
		V_{OUT} = 1.5 V, I_{LOAD} = 3 A, V_{IN} = 2.2 V		01, 02		13	
				03, 04		14	
		V_{OUT} = 5.0 V, I_{LOAD} = 3 A, V_{IN} = 6.0 V		01, 02		18	
				03, 04		20	
Ground pin current in shutdown	I_{SHDN}	ENABLE pin = 0 V, V_{IN} = 6.0 V	1,2,3	01, 02		10	µA
				03, 04		30	
Dropout voltage 3/	V_{DO}	I_{LOAD} = 1.0 A, V_{OUT} = 2.5 V	1,2,3	01, 02, 03, 04		100	mV
		I_{LOAD} = 2.0 A, V_{OUT} = 2.5 V				200	
		I_{LOAD} = 3.0 A, V_{OUT} = 2.5 V				300	
AC characteristics section.							
Input supply ripple rejection	PSRR	V_{P-P} = 300 mV, f = 1 kHz, I_{LOAD} = 3 A, V_{IN} = 2.5 V, V_{OUT} = 1.8 V	4,5,6	01, 02, 03, 04	42		dB

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Device start-up characteristics.							
Enable pin characteristics section.							
Rising threshold		$2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02, 03, 04	0.6	1.2	V
Falling threshold		$2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02, 03, 04	0.47	0.9	V
Enable pin leakage current		$V_{IN} = 6.0\ V$, EN = 6.0 V	1,2,3	01, 02, 03, 04		1	µA
Enable pin propagation delay		$V_{IN} = 2.2\ V$, EN rise to I_{OUT} rise	9,10,11	01, 02, 03, 04	225	450	µs
Hysteresis		Must be independent of V_{IN}, $2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02, 03, 04	90	318	mV
PG pin characteristics section.							
V_{OUT} error flag rising threshold		$2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02,	85	96	%
				03, 04	85	97	
V_{OUT} error flag falling threshold		$2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02, 03, 04	82	93	%
V_{OUT} error flag hysteresis		$2.2\ V < V_{IN} < 6.0\ V$	1,2,3	01, 02,	2.5	4	%V_{OUT}
				03, 04	2.5	5	
Error flag low voltage		$I_{SINK} = 1$ mA	1,2,3	01, 02, 03, 04		100	mV
		$I_{SINK} = 6$ mA				400	
Error flag leakage current		$V_{IN} = 6.0\ V$, PG = 6.0 V	1,2,3	01, 02, 03, 04		1	µA

1/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation. However, device type 01 is only tested at the "R" level in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein). Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects.
RHA device types 02 and 03 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation for condition A and levels M, D, P, and L for condition D. However, device types 02 and 03 are only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).
RHA device type 04 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 04 is only tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).
Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Unless otherwise specified, $V_{IN} = V_{OUT} + 0.5\ V$, $V_{OUT} = 1.8\ V$, $C_{IN} = C_{OUT} = 220\ \mu F$, and $I_L = 0\ A$.

3/ Dropout is defined as the difference between the supply V_{IN} and V_{OUT}, when the supply produces a 2% drop in V_{OUT} from its nominal value. Data measured within a 3 ms period.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_A)	V_{IN}	Linear energy transfer (LET)
01, 02,	No SEL 3/	+125°C	Maximum bias 6.0 V	Effective LET 4/ ≤ 86 MeV/(mg/cm^2)
	No SEB 3/	+125°C	Maximum bias 6.0 V	Effective LET 4/ ≤ 86 MeV/(mg/cm^2)
	SET observed 3/ 6/ (ΔV_{OUT} within ±5%)	+25°C	Minimum bias 2.2 V	Effective LET 4/ ≤ 86 MeV/(mg/cm^2)
03, 04	No SEL 3/	+125°C	Maximum bias 6.2 V	LET 5/ ≤ 86 MeV/(mg/cm^2)
	No SEB 3/	+125°C	Maximum bias 6.2 V	LET 5/ ≤ 86 MeV/(mg/cm^2)
	SET observed 3/ 6/ (ΔV_{OUT} within ±5%)	+25°C	Minimum bias 2.2 V	Effective LET 4/ ≤ 86 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ SEP tests performed with output capacitance used for SEE testing is 220 μF for C_{IN} and C_{OUT}, 200 nF for bypass capacitor. SEB and SEL tests done on a stand alone open loop configuration. For SEL, no latch up requiring manual intervention were observed. SET tests done in a closed loop configuration. The (ΔV_{OUT}) was measured across bulk capacitor of the application. The device can work down to a V_{OUT} = 0.8 V however, the SET performance of < ±5% at LET = 86 MeV/(mg/cm^2) is guaranteed at $V_{OUT} \geq$ 1.5 V only. SET tests performed with 220 μF, 10 V, 25 MΩ and 0.1 μF CDR04 capacitor on the input and output and fluence 2 x 10^6 ions/cm^2 at ±75 mV output.

4/ Effective LET of 86 MeV/(mg/cm^2) achieved by a beam of silver at LET 43 MeV/(mg/cm^2) at an angle of incidence of 60 degrees.

5/ LET of 86 MeV/(mg/cm^2) achieved by a beam of gold at LET 86 MeV/(mg/cm^2) at an angle of incidence of 0 degrees.

6/ See manufacturer's SEE report for additional details.

Case outline X

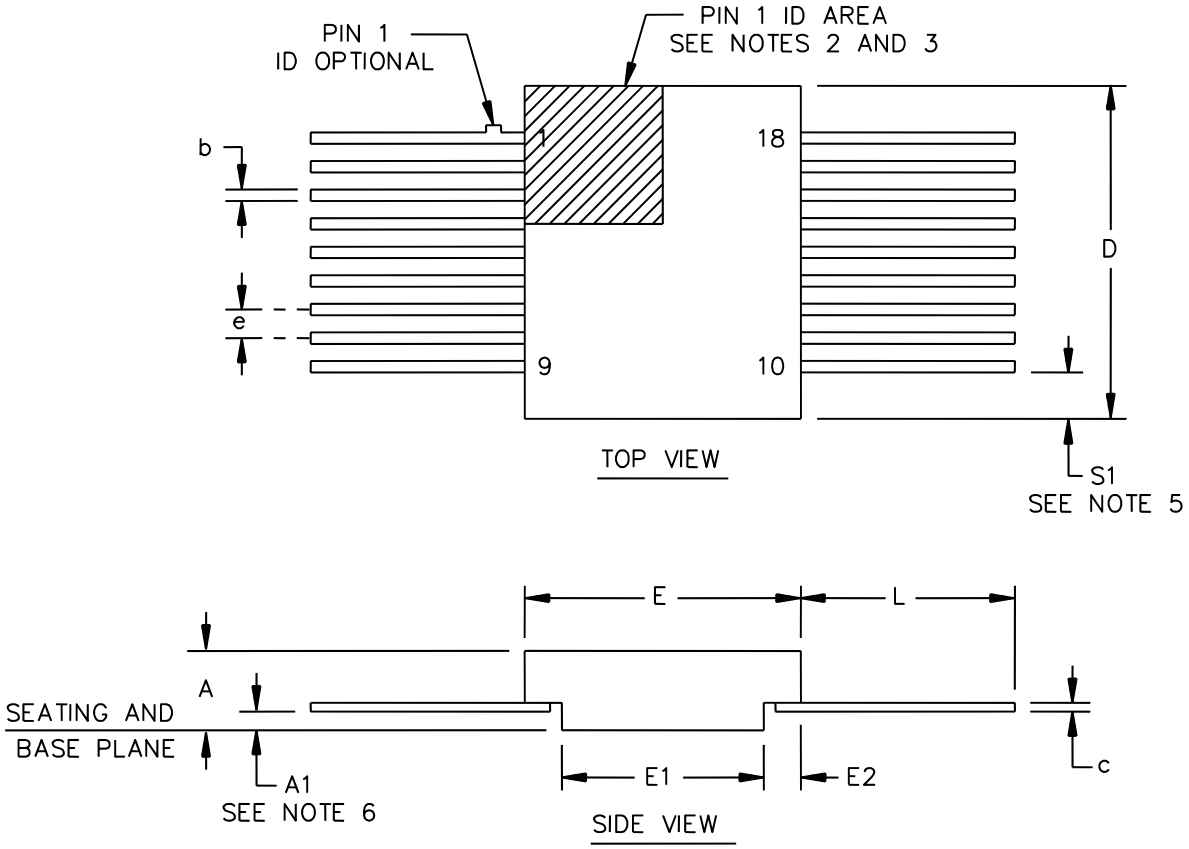


FIGURE 1. Case outlines.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.100	0.122	2.54	3.10
A1	0.026	0.036	0.66	0.92
b	0.013	0.020	0.330	0.508
c	0.004	0.010	0.1	0.25
D	0.456	0.476	11.58	12.09
e	0.040 BSC		1.016 BSC	
E	0.377	0.397	9.576	10.084
E1	0.283	0.303	7.19	7.70
E2	0.03	---	0.76	---
L	0.250	0.295	6.35	7.49
S1	0.005	---	0.127	---

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. Alternately, a tab may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
4. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Measure dimension at all four corners.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outlines - Continued.

Case outline Y

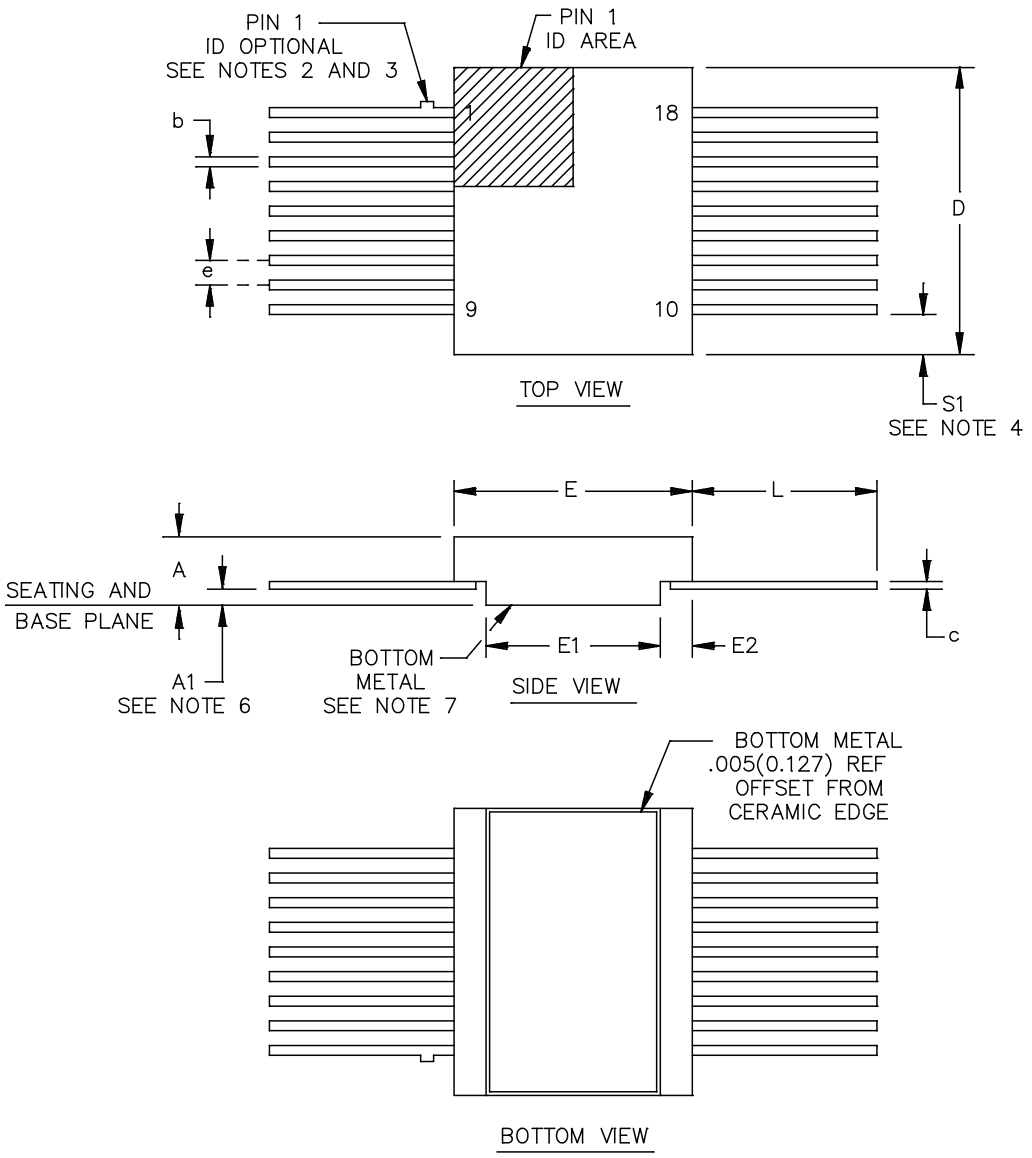


FIGURE 1. Case outlines - Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.100	0.122	2.54	3.10
A1	0.026	0.036	0.66	0.92
b	0.013	0.020	0.330	0.508
c	0.004	0.010	0.102	0.254
D	0.456	0.476	11.58	12.09
e	0.040 BSC		1.016 BSC	
E	0.377	0.397	9.576	10.084
E1	0.283	0.303	7.19	7.70
E2	0.03	---	0.76	---
L	0.250	0.295	6.35	7.49
S1	0.005	---	0.127	---

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. Alternately, a tab may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
4. Measure dimension at all four corners.
5. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is solderable metal surface.

FIGURE 1. Case outlines - Continued.

Device types	01, 02, 03, and 04	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	GND	GND
2	V_{OUT}	V_{OUT}
3	V_{OUT}	V_{OUT}
4	V_{OUT}	V_{OUT}
5	V_{OUT}	V_{OUT}
6	V_{OUT}	V_{OUT}
7	V_{OUT}	V_{OUT}
8	ADJ	ADJ
9	BYP	BYP
10	EN	EN
11	OCP	OCP
12	V_{IN}	V_{IN}
13	V_{IN}	V_{IN}
14	V_{IN}	V_{IN}
15	V_{IN}	V_{IN}
16	V_{IN}	V_{IN}
17	V_{IN}	V_{IN}
18	PG	PG
PACKAGE LID (SEE NOTE)	GND	GND
BOTTOM METAL	---	ELECTRICALLY ISOLATED

NOTE: The metal top lid of the package is connected to pin 1, GND.

FIGURE 2. Terminal connections.

Terminal symbol	Description
V_{IN}	Input supply pins.
PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
GND	GND pin.
V_{OUT}	Output voltage pins.
VADJ	VADJ pin allows V_{OUT} to be programmed with an external resistor divider.
BYP	Connect a 0.2 μF capacitor from BYP pin to GND, to filter the internal VREF.
OCP	OCP pin allows the current limit to be programmed with an external resistor.
EN	V_{IN} independent chip enable. TTL and CMOS compatible.
PACKAGE LID	The metal top lid of the package is connected to pin 1, GND.
BOTTOM METAL	Electrically isolated. The bottom of the package is a solderable metal surface.

FIGURE 2. Terminal connections – Continued.

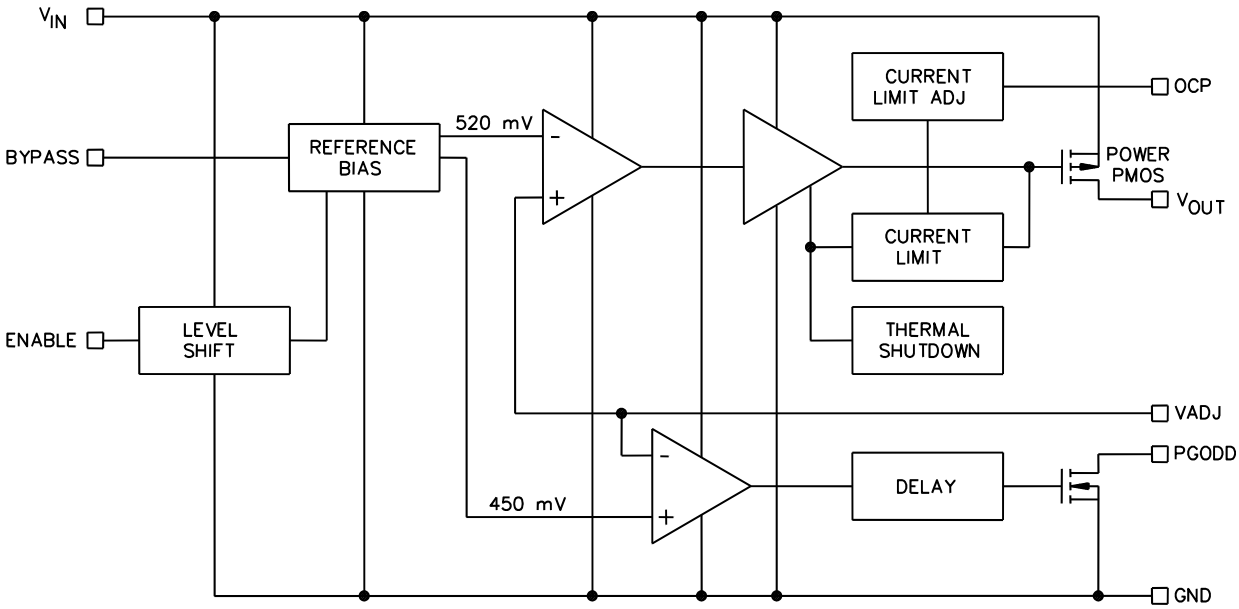


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 9,10,11 1/	1,2,3,4,5, 6,9,10,11 1/ 2/
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11 2/
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroup 1 and deltas.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Conditions	Device type	Min	Max	Units
Ground pin current in shutdown	I_{SHDN}		01, 02	-1	+1	µA
			03, 04	-3	+3	
Feedback pin	V_{ADJ}		01, 02, 03, 04	-1	+1	mV
Ground pin current	I_Q	V_{OUT} = 1.5 V, V_{IN} = 2.2 V, I_{LOAD} = 0 A	01, 02	-1.2	1.2	mA
			03, 04	-1.3	1.3	
Ground pin current	I_Q	V_{OUT} = 1.5 V, V_{IN} = 2.2 V, I_{LOAD} = 3 A	01, 02	-1.3	1.3	mA
			03, 04	-1.4	1.4	
Ground pin current	I_Q	V_{OUT} = 5.0 V, V_{IN} = 6.0 V, I_{LOAD} = 0 A	01, 02, 03, 04	-1.8	1.8	mA
Ground pin current	I_Q	V_{OUT} = 5.0 V, V_{IN} = 6.0 V, I_{LOAD} = 3 A	01, 02	-1.8	1.8	mA
			03, 04	-2.0	2.0	
Change in DC output voltage accuracy	$\Delta V_{OUT}/V_{OUT}$		01, 02, 03, 04	-1	1	%

1/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01 and 02. In addition, for device type 02 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(SI). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C ±10% for SET. The test temperature shall be +125°C ±10% for SEB and SEL.

f. Bias conditions for V_{IN} shall be as listed in Table IB for the latchup measurements.

g. For SEL, SEB, and SET test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latchup (SEL).

c. Number of burnouts (SEB).

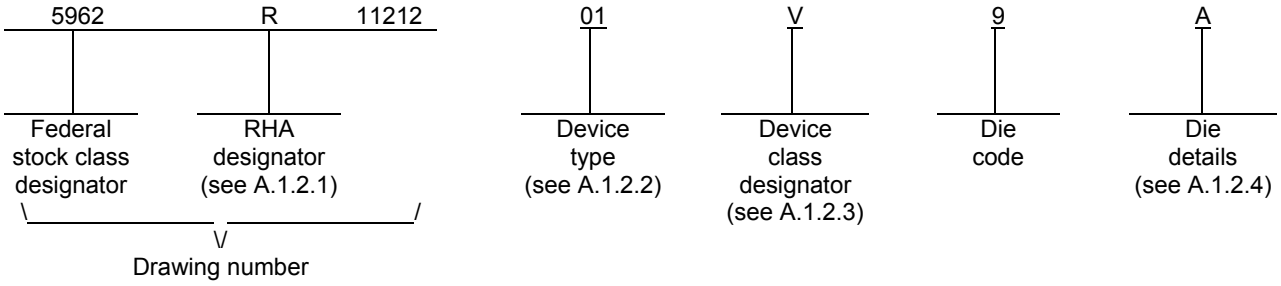
d. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-11212

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL75051SRH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
02	ISL75051SEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
03	ISL75051ASEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator
04	ISL73051ASEH	Radiation hardened BiCMOS 3.0 amp low dropout regulator

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

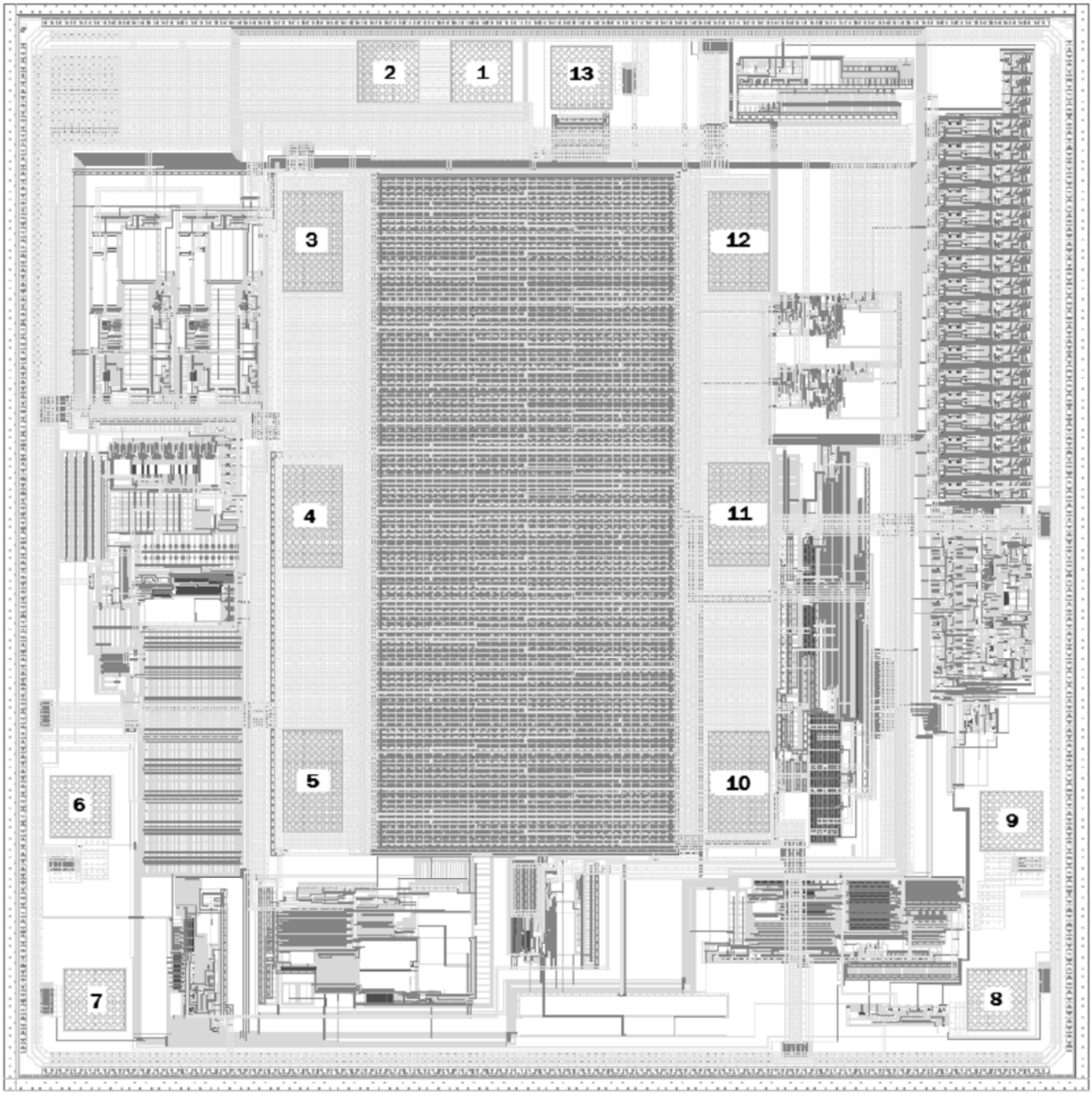


FIGURE A-1. Die bonding pad locations and electrical functions.

Pad	Name	X μm	Y μm
1	GND	0	0
2	GND	-393	0
3	V_{OUT}	-711	-710
4	V_{OUT}	-711	-1858
5	V_{OUT}	-711	-2964
6	ADJ	-1680	-3070
7	BYP	-1621	-3879
8	EN	2164	-3879
9	OCP	2222	-3131
10	V_{IN}	1078	-2965
11	V_{IN}	1078	-1853
12	V_{IN}	1078	-711
13	PG	420	-25

Pad X Y coordinates

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 4555 µm x 4555 µm (179.3 mils x 179.3 mils).
Die thickness: 304.8 µm ± 25.4µm (12.0 mils ± 1 mil).

Interface materials.
Top metallization: AlCu (99.5% / 0.5%).
Thickness: 2.7 µm ±0.4 µm.
Backside metallization: None.

Glassivation.
Type: Silicon oxide and silicon nitride.
Thickness: 0.3 µm ± 0.03 µm and 1.2 µm ± 0.12µm.

Substrate: Silicon.

Process: 0.6 µM BiCMOS junction isolated.

Assembly related information.
Substrate potential: Unbiased.
Special assembly instructions: None.

Weight ofpackaged device.
Case outline X : 1.07 grams normally with leads clipped.

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-03-05

Approved sources of supply for SMD 5962-11212 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1121201VXC	34371	ISL75051SRHVF
5962R1121201QXC	34371	ISL75051SRHQF
5962R1121201V9A	34371	ISL75051SRHVX
5962R1121202VXC	34371	ISL75051SEHVF
5962R1121202VYC	34371	ISL75051SEHVFE
5962R1121202V9A	34371	ISL75051SEHVX
5962R1121203VXC	34371	ISL75051ASEHVF
5962R1121203VYC	34371	ISL75051ASEHVFE
5962R1121203V9A	34371	ISL75051ASEHVX
5962L1121204VXC	34371	ISL73051ASEHVF
5962L1121204VYC	34371	ISL73051ASEHVFE
5962L1121204V9A	34371	ISL73051ASEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert Conlan Blvd. Palm Bay, FL 32905