REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add electrostatic discharge human body model limit under paragraph 1.3. - ro	10-02-12	C. SAFFLE
B	Make changes to footnote 6/ under paragraph 1.5 and footnote 3/ under Table IA. Add a paragraph under paragraph 1.5. - ro	10-09-21	C. SAFFLE
C	Add device type 02. Make changes to 1.2.2, 1.5, Table IA, Table IB, figure 2, and 4.4.4.1. -rrp	11-08-15	C. SAFFLE
D	Under paragraph 1.3, footnote 2/, delete absolute maximum rating 6 V and replace with 6.5 V. Under paragraph 1.3, footnote 3/ add the last sentence. Delete the radiation exposure circuit. - ro	12-07-03	C. SAFFLE
E	Add device type 03 and case outline Y. Make changes to case outline X dimensions A, D, D1, E, E1, and L as specified under figure 1. Add heatsink and package lid descriptions to figure 2. Delete device class M references. - ro	13-06-12	C. SAFFLE
F	Add footnote to device types 01 and 02 as specified under paragraphs 1.2.2 and A.1.2.2. - ro	16-05-16	C. SAFFLE
G	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	21-05-21	J. ESCHMEYER
H	Make changes to Upper and Lower device $r_{DS(ON)}$ parameter limits and delete footnote 4/ from these tests only as specified under Table IA. - ro	22-08-10	J. ESCHMEYER

Revision Status of Sheets

REV	H	H	H	H	H	H	H															
SHEET	23	24	25	26	27	28	29															
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
10-01-20

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

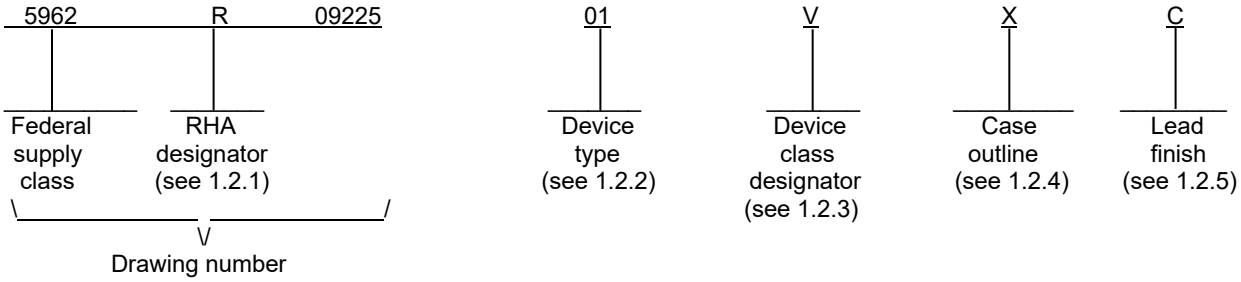
MICROCIRCUIT, RADIATION HARDENED, LINEAR, SYNCHRONOUS BUCK REGULATOR, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL H	SIZE A	CAGE CODE **67268**	**5962-09225**
		SHEET	1 OF 29	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	ISL70001SRH	Radiation hardened, synchronous buck regulator
02 1/	ISL70001SEH	Radiation hardened, synchronous buck regulator
03	ISL70001ASEH	Radiation hardened, synchronous buck regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Quad flat pack
Y	See figure 1	48	Quad flat pack with heat sink

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ In applications where the ENABLE input is tied high to PVIN the input voltage ramp rate must be equal to or greater than 10 V/ms. This is to prevent unwanted voltage from prematurely appearing on the output. For a PVIN voltage that has a slower ramp rate or is stepped up, use of device type 03 is recommended. The parameter PVIN ramp $\leq$ 10 V/ms is not specified in Table I because the customers design or configuration drives the ramp rate.

1.3 Absolute maximum ratings. 2/ 3/ 4/

AVDD pins ..... AGND – 0.3 V to AGND + 5.7 V
DVDD pins ..... DGND – 0.3 V to DGND + 5.7 V
LXx, PVINx pins ..... PGNDx – 0.3 V to PGNDx + 5.7 V
AVDD – AGND, DVDD – DGND ..... PVINx – PGNDx ± 0.3 V
EN, FB, PORSEL, REF pins ..... AGND – 0.3 V to AVDD + 0.3 V
M/S, SYNC, TDI, TDO, ZAP pins ..... DGND – 0.3 V to DVDD + 0.3 V
PGOOD pin ..... DGND – 0.3 V to DGND + 5.7 V
SS pin ..... DGND – 0.3 V to DGND + 2.5 V

Power dissipation (P_D) :
Case outline X:
T_A = +25°C ..... 3.28 W
T_A = +125°C ..... 0.54 W
T_C = +25°C ..... 40.00 W
T_C = +125°C ..... 6.66 W
Case outline Y:
T_A = +25°C ..... 6.31 W
T_A = +125°C ..... 1.05 W
T_C = +25°C ..... 92.30 W
T_C = +125°C ..... 15.38 W

Junction temperature (T_J) ..... +145°C
Maximum lead temperature (soldering, 10 seconds) ..... +260°C
Storage temperature range ..... -65°C to +150°C
Electrostatic discharge (ESD) classification:
Human body model (HBM) ..... 2000 V

Thermal resistance, junction-to-case (θ_{JC})
Case outline X ..... 3.0°C/W 5/
Case outline Y ..... 1.3°C/W 5/

Thermal resistance, junction-to-ambient (θ_{JA})
Case outline X ..... 36.5°C/W 6/
Case outline Y ..... 19°C/W 6/

_____

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ Absolute maximum ratings apply to operation in a heavy ion environment as per Table IB. For applications that operate outside a heavy ion environment, the 5.7 V absolute maximum rating increases to 6.5 V.

4/ The 5.7 V absolute maximum rating must be met for a 20 MHz bandwidth limited observation at the device pins. In addition, for a 600 MHz bandwidth limited observation, the peak transient voltage on PVINx (measured to PGNDx) must be less than 7.1 V with a duration above 5.7 V of less than 10 ns, and the peak transient voltage on LXx (measured to PGNDx) must be less than 7.9 V with a duration above 5.7 V of less than 10 ns.

V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3 V or 5.5 V and GND = AGND = DGND = PGNDx = TDI = TDO = ZAP = 0 V.

5/ For θ_{JC}, the case temperature location is the center of the package underside.

6/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board.

1.4 Recommended operating conditions.

AVDD	AGND + 3 V to 5.5 V
DVDD	DGND + 3 V to 5.5 V
PVINx	PGNDx + 3 V to 5.5 V
AVDD – AGND, DVDD – DGND	PVINx – PGNDx ± 0.1 V
EN, FB, PORSEL	AGND to AVDD
M/S, PGOOD, SYNC	DGND to DVDD
REF, SS	Internally set
TDI, TDO, ZAP	DGND
I_{LXx} (T_J < +145°C)	0 A to 1.0 A
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 7/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):	
Device type 01	Not production tested 8/
Device types 02 and 03	50 krads(Si) 8/ 9/
Single event phenomenon (SEP) (see 4.4.4.2) :	
No SEL occurs at effective LET (V_{IN} = 5.7 V, T_C = +125°C)	≤ 86.4 MeV/(mg/cm^2) 10/
No SEB occurs at effective LET (V_{IN} = 5.7 V, T_C = +125°C)	≤ 86.4 MeV/(mg/cm^2) 10/
No SET occurs at effective LET (< 1 LXx pulse perturbation) (T_C = +25°C)	≤ 86.4 MeV/(mg/cm^2) 10/
Single event phenomenon (SEP) cross sections:	
Single event functional interrupt (SEFI) (V_{IN} = 5 V, T_C = +25°C, LET = 86.4 MeV(mg/cm^2)	= 6.5 x 10^{-8}cm^2 10/ 11/
Single event functional interrupt (SEFI) (V_{IN} = 3 V, T_C = +25°C, LET = 86.4 MeV/(mg/cm^2)	= 1.4 x 10^{-6}cm^2 10/ 11/
Single event functional interrupt (SEFI) (V_{IN} = 3 V, T_C = +25°C, LET = 61 MeV/(mg/cm^2)	= 1.1 x 10^{-7}cm^2 10/ 11/

The manufacturer supplying RHA parts on this drawing has performed characterization testing that demonstrates the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) according to MIL-STD-883 Method 1019 paragraph 3.13.1.1. Therefore this part may be considered ELDRS free.

7/ This part has been tested and does not exhibit enhanced low dose rate sensitivity (ELDRS). Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

8/ For device types 01, 02 and 03, the manufacturer supplying RHA parts on this drawing has performed characterization testing to a level of 150 krads(Si) at low and high dose rate in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1. Therefore, this part may be considered ELDRS free. Testing beyond 150 krads(Si) was not performed.

9/ Device types 02 and 03 are production lot acceptance tested in accordance with MIL-PRF-38535, Appendix B, technology conformance inspection (TCI) group E, subgroup 2 to 50 krads(Si) at low dose rate (≤ 10 mrads(Si)/s).

10/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but devices are not production tested unless specified by the customer through the purchase order or contract.

11/ SEFI behavior is similar to an overcurrent protection (OCP) fault with soft start and automatic recovery.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply section							
Operating supply current	I_{OP}	V_{IN} = 5.5 V	1,2,3	01, 02,		65	mA
		V_{IN} = 3.6 V	1,2,3	03		45	
Shutdown supply current	I_{SD}	V_{IN} = 5.5 V, EN = GND	1,2,3	01, 02		12	mA
				03		6	
		V_{IN} = 3.6 V, EN = GND	1,2,3	01, 02		6	
				03		4.5	
Output voltage section							
Reference voltage tolerance	V_{REF}		1,2,3	01, 02, 03	0.594	0.606	V
Output voltage tolerance	V_{OUT}	V_{OUT} = 0.8 V to 2.5 V, V_{IN} = 4.5 V to 5.5 V, 3/ 4/ I_{OUT} = 0 A to 6 A	4,5,6	01, 02, 03	-2	2	%
		V_{OUT} = 0.8 V to 2.5 V, V_{IN} = 3 V to 3.6 V, 3/ 4/ I_{OUT} = 0 A to 6 A	4,5,6		-2	2	
Feedback (FB) input leakage current	I_{FB}	V_{IN} = 5.5 V, V_{FB} = 0.6 V	1,2,3	01, 02, 03	-1	1	µA
PWM control logic section							
Oscillator accuracy	OSC		4,5,6	01, 02, 03	0.85	1.15	MHz
External oscillator range	EXT_{OSC}		4,5,6	01, 02, 03	0.80	1.20	MHz
Minimum LXx on time	t_{ON}	V_{IN} = 5.5 V, test mode	9,10,11	01, 02,		150	ns
		V_{IN} = 3 V, test mode	9,10,11	03		210	
Minimum LXx off time	t_{OFF}	V_{IN} = 5.5 V, test mode	9,10,11	01, 02,		100	ns
		V_{IN} = 3 V, test mode	9,10,11	03		100	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PWM control logic section - continued.							
Master/slave (M/S) input voltage	MS_{VIH}	Input high threshold	1,2,3	01, 02, 03	V_{IN} - 0.5		V
	MS_{VIL}	Input low threshold	1,2,3			0.5	
Master/slave (M/S) input leakage current	MS_{LKG}	V_{IN} = 5.5 V, M/S = GND or V_{IN}	1,2,3	01, 02, 03	-1	1	µA
Synchronization (SYNC) input voltage	$SYNC_{VIH}$	Input high threshold, M/S = GND	1,2,3	01, 02, 03	2.3		V
	$SYNC_{VIL}$	Input low threshold, M/S = GND	1,2,3			1	
Synchronization (SYNC) input leakage current	$SYNC_{LKG}$	V_{IN} = 5.5 V, M/S = GND, SYNC = GND or V_{IN}	1,2,3	01, 02, 03	-1	1	µA
Synchronization (SYNC) output voltage	$SYNC_{VO}$	V_{IN} – V_{OH} at I_{OH} = -1 mA	1,2,3	01, 02, 03		0.4	V
		V_{OL} at I_{OL} = 1 mA	1,2,3			0.4	
Power blocks section							
Upper device $r_{DS(ON)}$	$r_{DS(ON)}$	V_{IN} = 3 V, 0.4 A per power block, test mode	4	01, 02, 03	180	281	mΩ
			5		225	395	
			6		125	210	
Lower device $r_{DS(ON)}$	$r_{DS(ON)}$	V_{IN} = 3 V, 0.4 A per power block, test mode	4	01, 02, 03	120	195	mΩ
			5		165	275	
			6		82	145	
LXx output leakage	LX_{LKG}	V_{IN} = 5.5 V, EN = LXx = GND, single LXx output	1,2,3	01, 02, 03	-1		µA
		V_{IN} = 5.5 V, EN = GND, LXx = V_{IN}, single LXx output	1,2,3			15	
Deadtime 4/	t_{dead}	Within a single power block or between power blocks	1,2,3	01, 02, 03	1.7		ns
Power on reset (POR) section							
POR select (PORSEL) voltage	$PORSEL_H$	Input high threshold	1,2,3	01, 02, 03	V_{IN} - 0.5		V
	$PORSEL_L$	Input low threshold	1,2,3			0.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power on reset (POR) section - continued.							
POR select (PORSEL) input leakage current	PORSEL LKG	V_{IN} = 5.5 V, PORSEL = GND or V_{IN}	1,2,3	01, 02, 03	-1	1	µA
POR input voltage	POR_{HI}	Rising threshold, PORSEL = V_{IN}	1,2,3	01, 02, 03	4.1	4.45	V
	POR_{HI} V_{hys}	Hysteresis, PORSEL = V_{IN}	1,2,3		225	425	mV
	POR GND	Rising threshold, PORSEL = GND	1,2,3		2.65	2.95	V
	Vhys POR GND	Hysteresis, PORSEL = GND	1,2,3		90	260	mV
Enable (EN) input voltage	EN_{THR}	Rising / falling threshold	1,2,3	01, 02, 03	0.56	0.64	V
Enable (EN) input leakage current	EN_{LKG}		1,2,3	01, 02, 03	-3	3	µA
Enable (EN) sink current	EN_{SNK}		1,2,3	01, 02, 03	6.4	16.6	µA
Soft start section							
Soft start source current	SS_{ISRC}	SS = GND	1,2,3	01, 02, 03	20	27	µA
Soft start discharge on resistance	SS_R		4,5,6	01, 02, 03		4.7	Ω
POWER GOOD signal section							
Rising threshold	PR_{rise}	V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	107	115	%
Rising hysteresis	PR_{hys}	V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	2	5	%
Falling threshold	PR_{fall}	V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	85	93	%
Falling hysteresis	PR_{hys}	V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	2	5	%
Power good drive current	PG_{DR}	V_{IN} = 3 V, PGOOD = 0.4 V, EN = GND	1,2,3	01, 02, 03	7.3		mA
Power good leakage current	PG_{lkg}	V_{IN} = PGOOD = 5.5 V	1,2,3	01, 02, 03		1	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Protection features section							
Undervoltage monitor							
Undervoltage trip threshold	UV_{trip}	V_{IN} = 3 V, V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	71	79	%
Undervoltage recovery threshold	UV_{rec}	V_{IN} = 3 V, V_{FB} as a % of V_{REF}, test mode	4,5,6	01, 02, 03	84	92	%
Overcurrent monitor							
Over current trip level	OC_{trip}	LX4 power block, test mode 5/	1,2,3	01, 02, 03	1.3	2.5	A
Overcurrent or short circuit duty cycle	OC_{DC}	V_{IN} = 3 V, SS interval = 200 µs, test mode, fault interval divided by hiccup interval	4,5,6	01, 02, 03		5	%

1/ Unless otherwise specified, V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3 V or 5.5 V; GND = AGND = DGND = PGNDx = TDI = TDO = ZAP = 0 V; FB = 0.65 V; PORSEL = V_{IN} for 4.5 V $\le V_{IN} \le$ 5.5 V and GND for $V_{IN} <$ 4.5 V; SYNC = LXx = open circuit; PGOOD is pulled up to V_{IN} with a 1 kΩ resistor; REF is bypassed to GND with a 220 nF capacitor; SS is bypassed to GND with a 100 nF capacitor; I_{OUT} = 0 A; $T_A = T_J$ = -55°C to +125°C.

2/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, device types 01, 02, and 03 are tested only at the "R" level in accordance with MIL-STD-883 method 1019 condition A.

RHA device types 01, 02 and 03 supplied on this drawing have had characterization testing performed to a level of 50 krads(Si) that demonstrates the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) according to MIL-STD-883 method 1019 paragraph 3.13.1.1. (see paragraph 1.5 herein). In addition, device types 02 and 03 (device class V) supplied to this drawing is production lot acceptance tested on a wafer by wafer basis to the "L" level (50 krads(Si)) in accordance with MIL-STD-883 method 1019 condition D.

Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Limits do not include tolerance of external feedback resistors. The 0 A to 6 A output current range may be reduced by minimum LXx on time and minimum LXx off time specifications.

4/ Limits established by characterization or analysis and are not production tested.

5/ During an output short circuit, peak current through the power block(s) can continue to build beyond the overcurrent trip level by up to 3 A. With all six power blocks connected, peak current through the power blocks and output inductor could reach (6 x 2.5 A) + 3 A = 18 A. The output inductor must support this peak current without saturating.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	Temperature (T_C)	Bias V_{IN}	Effective linear energy transfer (LET)	Cross section
01, 02, 03	No SEL 3/	+125°C	5.7 V	≤ 86.4 MeV/(mg/cm^2)	
	No SEB 3/	+125°C	5.7 V	≤ 86.4 MeV/(mg/cm^2)	
	No SET 4/	+25°C	3 V or 5.5 V	≤ 86.4 MeV/(mg/cm^2)	
	SEFI 5/	+25°C	5 V	= 86.4 MeV/(mg/cm^2)	6.5 x 10^{-8}cm^2
	SEFI 6/	+25°C	3 V	= 86.4 MeV/(mg/cm^2)	1.4 x 10^{-6}cm^2
	SEFI 7/	+25°C	3 V	= 61 MeV/(mg/cm^2)	1.1 x 10^{-7}cm^2

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ V_{OUT} = 1.8 V, I_{OUT} = 7 A, fluence = 4 X10^7 ions/cm^2, no SEL or SEB.

4/ V_{OUT} = 1.8 V, I_{OUT} = 4 A, fluence = 4.4 X10^7 ions/cm^2, SET < 1 LXx pulse perturbation,

5/ V_{OUT} = 1.8 V, I_{OUT} = 4 A, effective LET = 86.4 MeV/(mg/cm^2), fluence = 1 X10^8 ions/cm^2, SEFI = behavior similar to an overcurrent protection (OCP) fault with soft start and automatic recovery.

6/ V_{OUT} = 1.8 V, I_{OUT} = 4 A, effective LET = 86.4 MeV(mg/cm^2), fluence = 2.2 X10^7 ions/cm^2, SEFI = behavior similar to an overcurrent protection (OCP) fault with soft start and automatic recovery.

7/ V_{OUT} = 1.8 V, I_{OUT} = 4 A, effective LET = 61 MeV/(mg/cm^2), fluence = 4.4 X10^7 ions/cm^2, SEFI = behavior similar to an overcurrent protection (OCP) fault with soft start and automatic recovery.

Case X

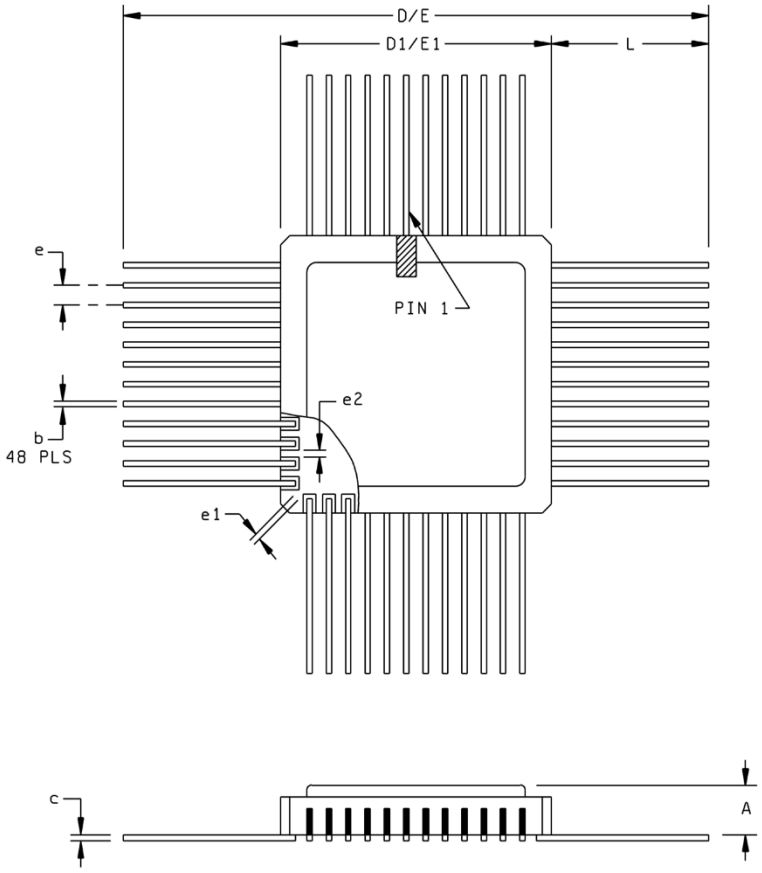


FIGURE 1. Case outlines.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.076	0.099	1.93	2.51	
b	0.008	0.015	0.20	0.38	3
c	0.009	0.016	0.23	0.41	3
D	1.080	1.118	27.43	28.40	
D1	0.555	0.572	14.10	14.53	
E	1.080	1.118	27.43	28.40	
E1	0.555	0.572	14.10	14.53	
e	0.040 BSC		1.02 BSC		
e1	0.015	---	0.38	---	5
e2	0.007	---	0.18	---	
L	0.253	0.287	6.43	7.29	
N		48		48	4

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
3. The maximum limits of lead dimensions b and c shall be measured at the center of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. N is the maximum number of terminal positions.
5. Measure dimension e1 at all four corners.
6. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads

FIGURE 1. Case outlines – continued.

Case Y

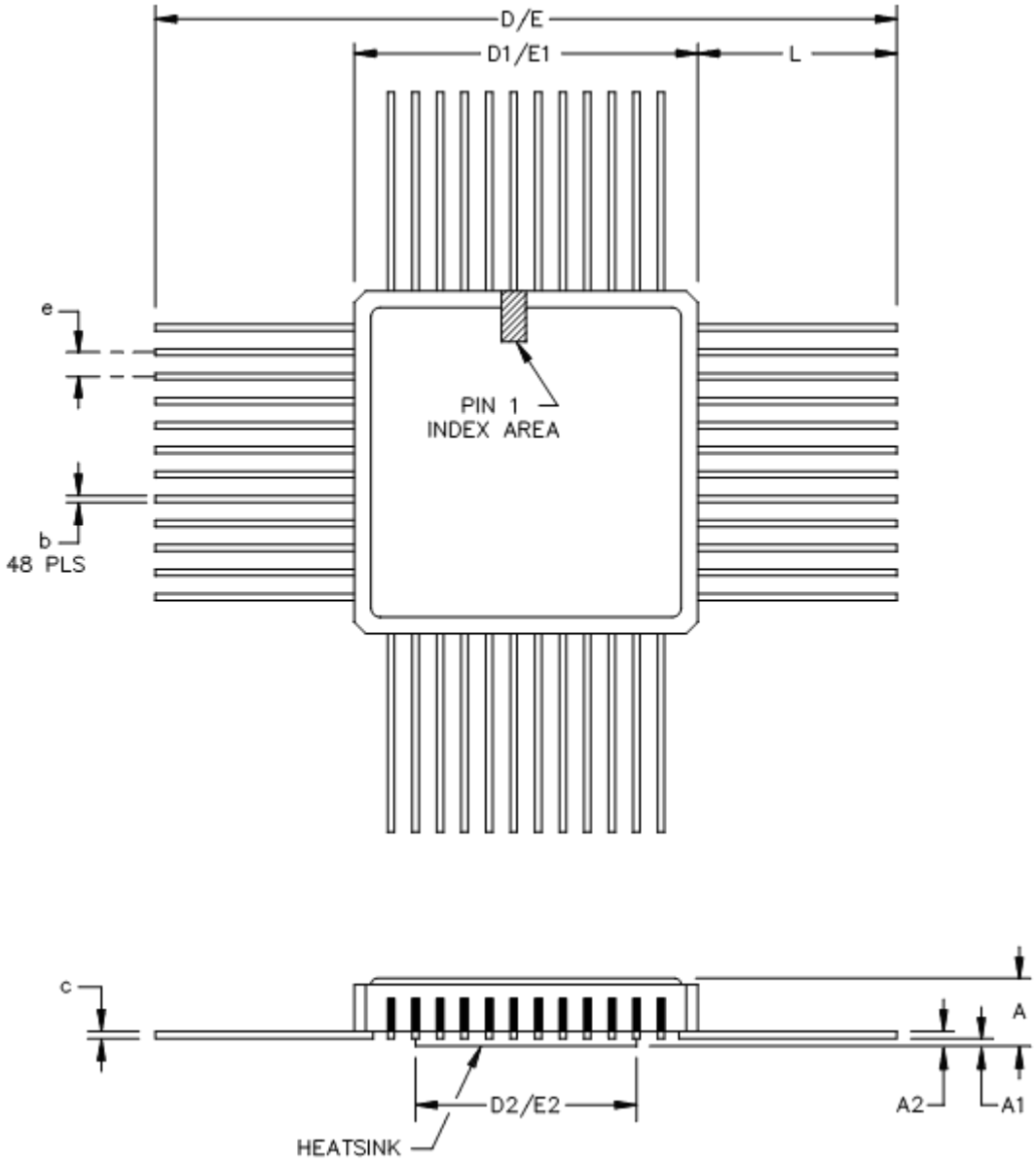


FIGURE 1. Case outlines – continued.

Case Y – continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.105	0.131	2.67	3.33	
A1	0.026	---	0.66	---	2
A2	0.042 REF		1.067 REF		
b	0.008	0.012	0.20	0.30	
c	0.009	0.013	0.23	0.33	
D/E	1.080	1.118	27.43	28.40	
D1/E1	0.555	0.572	14.10	14.53	
D2/E2	0.349	0.359	8.87	9.12	
e	0.040 BSC		1.016 BSC		
L	0.253	0.287	6.43	7.29	
N		48		48	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. . Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.

FIGURE 1. Case outlines – continued.

Device types	01, 02, and 03			
Case outlines	X and Y			
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	PGND1		25	PVIN6
2	PGND1		26	LX6
3	LX1		27	PGND6
4	PVIN1		28	PGND6
5	PVIN1		29	PGND5
6	SYNC		30	PGND5
7	M/S		31	LX5
8	ZAP		32	PVIN5
9	TDI		33	PVIN5
10	TDO		34	PVIN4
11	PGOOD		35	PVIN4
12	SS		36	LX4
13	DVDD		37	PGND4
14	DVDD		38	PGND4
15	DGND		39	PGND3
16	DGND		40	PGND3
17	AGND		41	LX3
18	AGND		42	PVIN3
19	AVDD		43	PVIN3
20	REF		44	PVIN2
21	FB		45	PVIN2
22	EN		46	LX2
23	PORSEL		47	PGND2
24	PVIN6		48	PGND2

FIGURE 2. Terminal connections.

Terminal symbol	Description
PGNDx	These pins are the power grounds associated with the corresponding internal power blocks. Connect these pins directly to the ground plane. These pins should connect to the negative terminals of the input and output capacitors. Locate the input and output capacitors as close as possible to the integrated circuit.
LXx	These pins are the outputs of the corresponding internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous MOSFET power switches. To minimize voltage undershoot, it is recommended that a Schottky diode be connected from these pins to PGNDx. The Schottky diode should be located as close as possible to the integrated circuit.
PVINX	These pins are the power supply inputs for the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3 V to 5.5 V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the integrated circuit.
SYNC	This pin is the synchronization input / output for the integrated circuit. When configured as an output (master mode), this pin drives the SYNC input of another identical device. When configured as an input (slave mode), this pin accepts the SYNC output from another identical device or an external clock. Synchronization of the slave unit is 180° out of phase with respect to the master unit. If synchronizing to an external clock, the clock must be single event effects (SEE) hardened and the frequency must be within the range of 1 MHz ±20 %.
M/S	This pin is the master / slave input for selecting the direction of the bidirectional SYNC pin. For SYNC = output (master mode), connect this pin to DVDD. For SYNC = input (slave mode), connect this pin to DGND.
ZAP	This pin is a trim input and is used to adjust various internal circuitry. Connect this pin to DGND.
TDI	This pin is the test data input of the internal built in test (BIT) circuitry. Connect this pin to DGND.
TDO	This pin is the test data output of the internal built in test (BIT) circuitry. Connect this pin to DGND.
PGOOD	This pin is the power good output. This pin is the open drain logic output that is pulled to DGND when the output voltage is outside a ±11 % normal regulation widow. This pin can be pulled up to any voltage from 0 V to 5.5 V, independent of the supply voltage. A nominal 1 kΩ to 10 kΩ pull up resistor is recommended. Bypass this pin to DGND with a 10 nF ceramic capacitor to mitigate SEE.

FIGURE 2. Terminal connections – continued.

Terminal symbol	Description
SS	This pin is the soft start input. Connect a ceramic capacitor from this pin to DGND to set the soft start ramp time in accordance with the following equation: $t_{SS} = (C_{SS} \times V_{REF}) / I_{SS}$, where t_{SS} = soft start output ramp time, C_{SS} = soft start capacitance, V_{REF} = reference voltage (0.6 V normally), I_{SS} = soft start charging current (23 μA normally). The soft start time is adjustable from approximately 2 ms to 200 ms. The range of soft start capacitor should be 82 nF to 8.2 μF.
DVDD	These pins are the bias supply input for the internal digital control circuitry. Connect these pins together at the integrated circuit and locally filter them to DGND using a 1 Ω resistor and a 1 μF ceramic capacitor. Locate both filter components as close as possible to the integrated circuit.
DGND	These pins are the digital ground associated with the internal digital control circuitry. Connect these pins directly to the ground plane.
AGND	These pins are the analog ground associated with the internal analog control circuitry. Connect these pins directly to the ground plane.
AVDD	This pin is the bias supply input for the internal analog control circuitry. Locally filter this pin to AGND using a 1 Ω resistor and a 1 μF ceramic capacitor. Locate both filter components as close as possible to the integrated circuit.
REF	This pin is the internal reference voltage output. Bypass this pin to AGND with a 220 nF ceramic capacitor located as close as possible to the integrated circuit. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin.
FB	This pin is the voltage feedback input to the internal error amplifier. Connect a resistor from FB to V_{OUT} and from FB to AGND to adjust the output voltage in accordance with the following equation: $V_{OUT} = V_{REF} \times [1 + (R_T / R_B)]$, where V_{OUT} = output voltage, V_{REF} = reference voltage (0.6 V normally), R_T = top divider resistor (must be 1 kΩ), R_B = bottom divider resistor The top divider resistor must be 1 kΩ to mitigate SEE. Connect a 4.7 nF ceramic capacitor across RT to mitigate SEE and to improve stability margins.
EN	This pin is the enable input to the integrated circuit. This is a comparator type input with a rising threshold of 0.6 V and programmable hysteresis. Driving this pin above 0.6 V enables the integrated circuit. Bypass this pin to AGND with a 10 nF ceramic capacitor to mitigate SEE.
PORSEL	This pin is the input for selecting rising and falling power on reset (POR) thresholds. For a nominal 5 V supply, connect this pin to DVDD. For a nominal 3.3 V supply, connect this pin to DGND. For nominal supply voltages between 5 V and 3.3 V, connect this pin to DGND.
HEATSINK	The heatsink is electrically isolated and should be connected to a thermal chassis of any potential for optimal thermal relief.
PACKAGE LID	For case outline X the lid is floating. For case outline Y the lid is connect to PGNDx.

FIGURE 2. Terminal connections – continued.

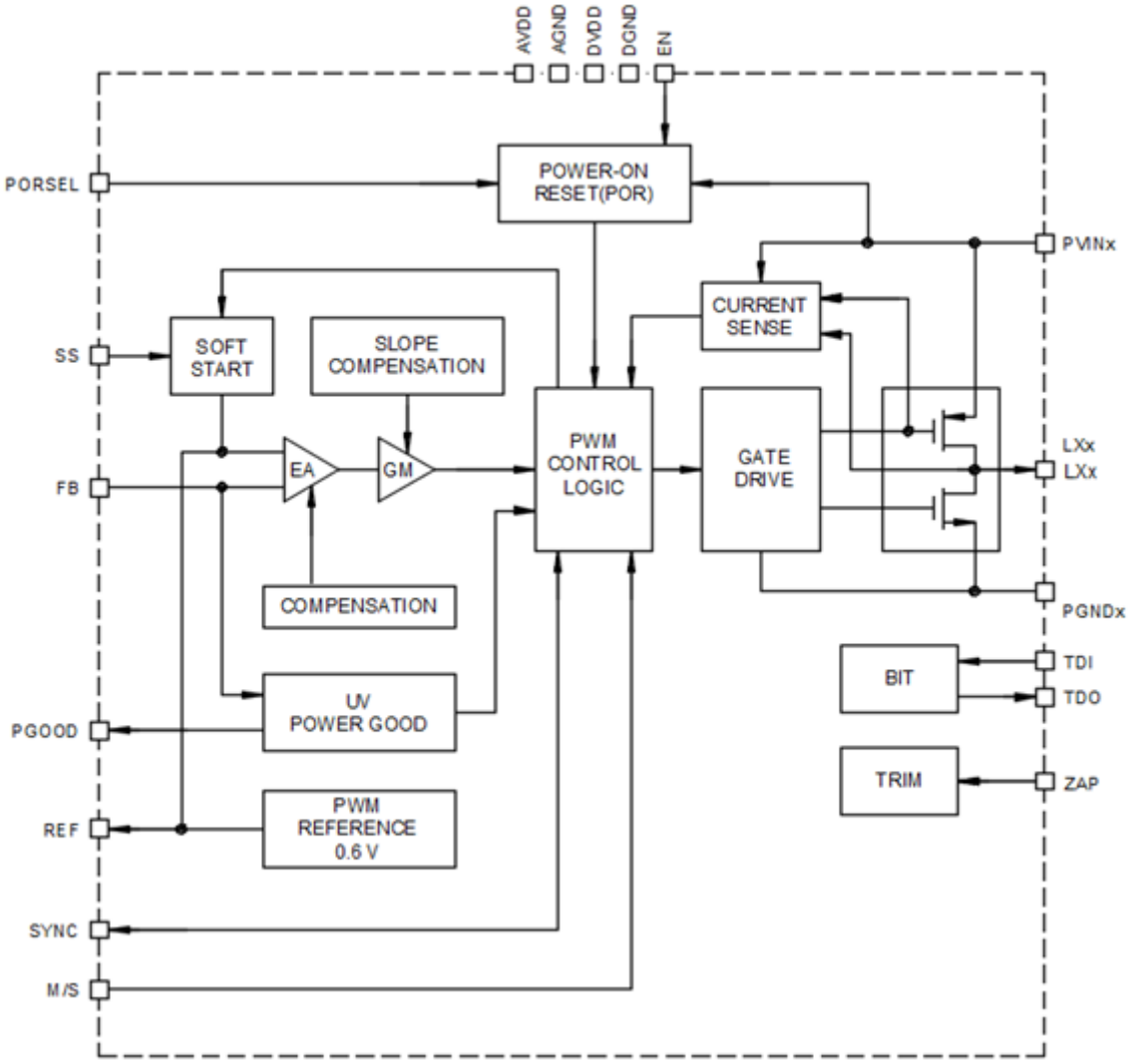


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3, 1/ 2/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 2/ 9,10,11
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroup 1 and deltas.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Device type	Delta limits		Units
			Min	Max	
Shutdown supply current (3.6 V)	I_{SD}	01, 02	-1.20	+1.20	mA
		03	-0.65	+0.65	
Shutdown supply current (5.5 V)	I_{SD}	01, 02	-2.40	+2.40	mA
		03	-0.90	+0.90	
Reference voltage tolerance (3 V)	V_{REF}	01, 02, 03	-3.00	+3.00	mV
Reference voltage tolerance (5.5 V)	V_{REF}	01, 02, 03	-3.00	+3.00	mV
Oscillator accuracy (3 V)	OSC	01, 02, 03	-80	+80	kHz
Oscillator accuracy (5.5 V)	OSC	01, 02, 03	-80	+80	kHz
Soft start source current (3 V)	SS_{ISRC}	01, 02, 03	-2.50	+2.50	µA
Soft start source current (5.5 V)	SS_{ISRC}	01, 02, 03	-2.50	+2.50	µA

1/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, and 03. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein for device types 02 and 03.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +25°C ±10% for SET. The test temperature shall be +125°C ±10% for SEB and SEL.

f. Bias conditions shall be V_{IN} = 5.7 V maximum for the latchup measurements.

g. For SEL, SEB, SET, and SEFI test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Number of burnouts(SEB).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

e. Number of upsets (SEU).

f. Occurrence of SEGR

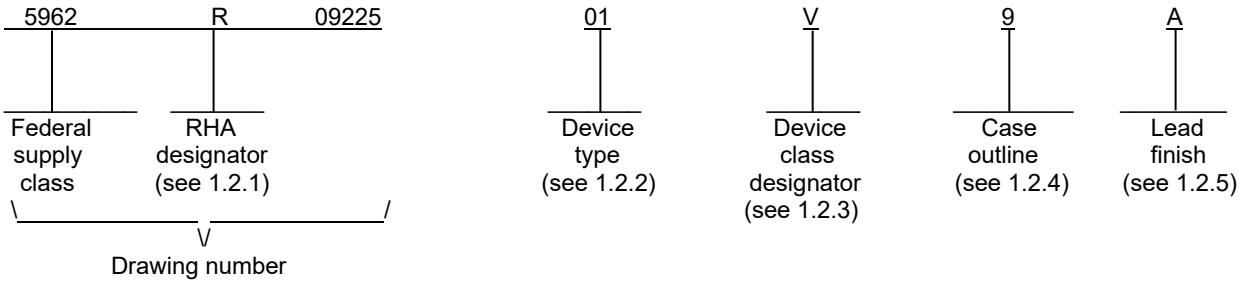
g. Occurrence of SEFI

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-09225

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	ISL70001SRH	Radiation hardened, synchronous buck regulator
02 1/	ISL70001SEH	Radiation hardened, synchronous buck regulator
03	ISL70001ASEH	Radiation hardened, synchronous buck regulator

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

1/ In applications where the ENABLE input is tied high to PVIN the input voltage ramp rate must be equal to or greater than 10 V/ms. This is to prevent unwanted voltage from prematurely appearing on the output. For a PVIN voltage that has a slower ramp rate or is stepped up, use of device type 03 is recommended. The parameter PVIN ramp $\leq$ 10 V/ms is not specified in Table I because the customers design or configuration drives the ramp rate.

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

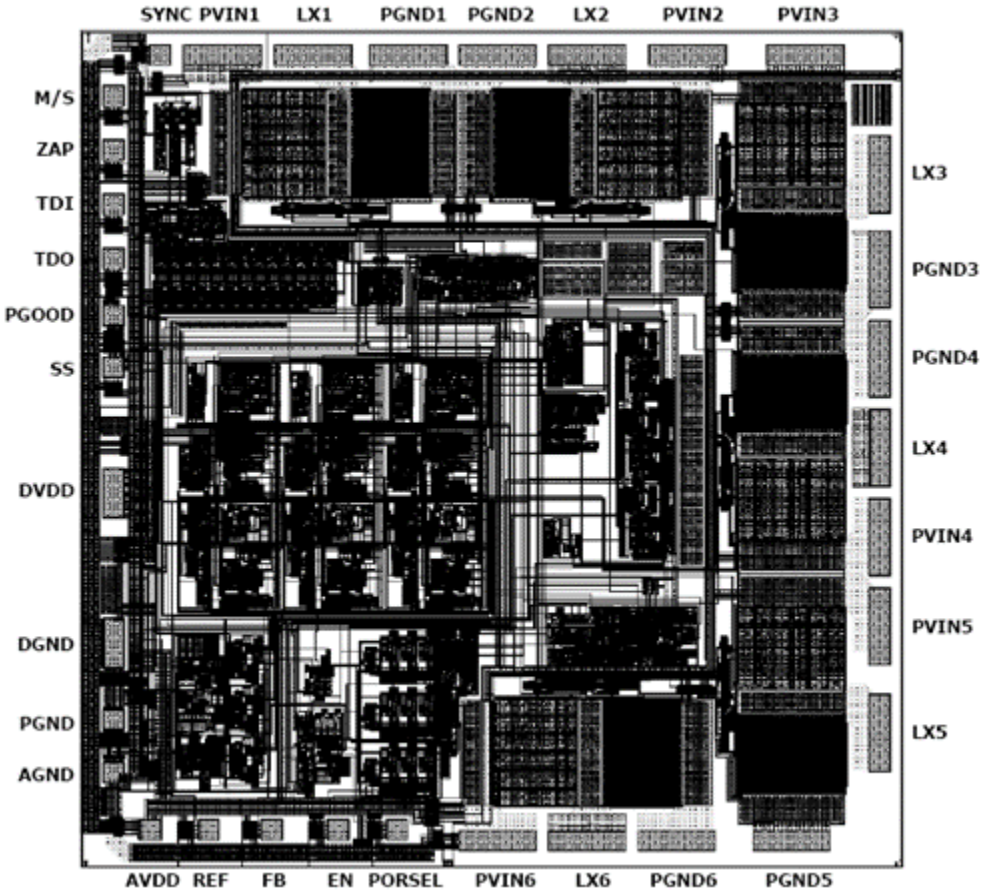
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 5720 μm x 5830 μm (225.2 mils x 229.5 mils)
Die thickness: 483 μm ± 25.4 μm (19.0 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (0.5%) 2.7 μm ± 0.4 μm
Backside metallization: None

Glassivation.
Type: Silicon oxide and silicon nitride
Thickness: 0.3 μm ±0.03 μm and 1.2 μm ±0.12 μm

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: PGND
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-08-10

Approved sources of supply for SMD 5962-09225 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0922501QXC	34371	ISL70001SRHQF
5962R0922501VXC	34371	ISL70001SRHVF
5962R0922501V9A	34371	ISL70001SRHVX
5962R0922502VXC	34371	ISL70001SEHVF
5962R0922502VYC	34371	ISL70001SEHVFE
5962R0922502V9A	34371	ISL70001SEHVX
5962R0922503VXC	34371	ISL70001ASEHVF
5962R0922503VYC	34371	ISL70001ASEHVFE
5962R0922503V9A	34371	ISL70001ASEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406