REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add descriptive designator CDIP2-T8 for case outline letter "P". Under paragraph 1.3, footnote 3/, delete θ_{JA} and substitute θ_{JC}. - ro	10-04-20	C. SAFFLE
B	Under paragraph 1.3; make change to the ESD HBM limit from 250 V to 2,000 V and add new footnote; delete entirely "RTCT pin" and "Other pins" limits. - ro	11-03-01	C. SAFFLE
C	Add device types 05, 06, 07, and 08. Add paragraph 6.7. - ro	12-09-20	C. SAFFLE
D	Add device class T to device type 04. - ro	13-08-13	C. SAFFLE
E	Make changes to correct and clarify SEL limits under paragraph 1.5 and Table IB. - ro	14-10-29	C. SAFFLE
F	Make SEL and SEB changes to paragraphs 1.5, 4.4.4.3, and Table IB by adding 0° and 60° angle of incidence. - ro	15-06-12	C. SAFFLE
G	Add device types 09, 10, 11, and 12. - ro	19-07-02	C. SAFFLE

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
10-01-28

REVISION LEVEL
G

MICROCIRCUIT, LINEAR, PULSE WIDTH MODULATOR CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-07249**

SHEET 1 OF 23

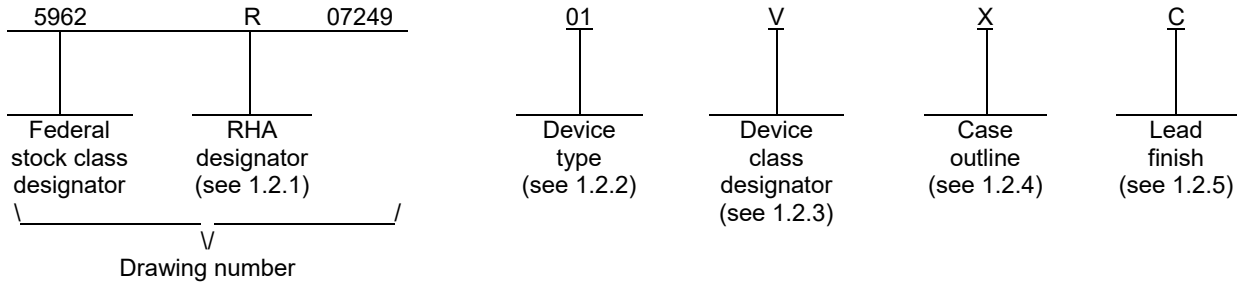
DSCC FORM 2233
APR 97

5962-E402-19

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic	Rising under voltage lockout	Maximum duty cycle	Circuit function
01	ISL78840ASRH	7.0 V	100 %	Pulse width modulator controller
02	ISL78841ASRH	7.0 V	50 %	Pulse width modulator controller
03	ISL78843ASRH	8.4 V	100 %	Pulse width modulator controller
04	ISL78845ASRH	8.4 V	50 %	Pulse width modulator controller
05	ISL78840ASEH	7.0 V	100 %	Pulse width modulator controller
06	ISL78841ASEH	7.0 V	50 %	Pulse width modulator controller
07	ISL78843ASEH	8.4 V	100 %	Pulse width modulator controller
08	ISL78845ASEH	8.4 V	50 %	Pulse width modulator controller
09	ISL738840ASEH	7.0 V	100 %	Pulse width modulator controller
10	ISL738841ASEH	7.0 V	50 %	Pulse width modulator controller
11	ISL738843ASEH	8.4 V	100 %	Pulse width modulator controller
12	ISL738845ASEH	8.4 V	50 %	Pulse width modulator controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	CDIP2-T8	8	Dual in line
X	See figure 1	8	Dual flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD}) ..... GND - 0.3 V to +14.7 V
Output voltage ..... GND - 0.3 V to V_{DD} + 0.3 V
Signal pins ..... GND - 0.3 V to 6.0 V
Electrostatic discharge (ESD) classification:
  Human body model (HBM) ..... 2,000 V 3/
Maximum junction temperature (T_J) ..... +150°C
Maximum storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum lead temperature (soldering, 10 seconds) (lead tips only) ..... +300°C
Thermal resistance, junction to case (θ_{JC}): 4/
  Case P ..... 20°C/W
  Case X ..... 15°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) ..... 9 V to 13.2 V 5/
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.4.1 Operational performance characteristics. 6/

Under voltage lockout (UVLO) section, hysteresis voltage :
  Device types 01 02, 05, 06, 09, and 10 ..... 0.4 V
  Device types 03, 04, 07, 08, 11, and 12 ..... 0.8 V
Voltage reference (V_{REF}) section, long term stability (T_A = 125°C at 1,000 hours) .. 5 mV
Error amplifier (EA) section, open loop voltage gain ..... 90 dB
EA section, unity gain bandwidth ..... 1.5 MHz
EA section, power supply rejection ratio (f = 120 Hz, V_{DD} = 9 V to 13.2 V) ..... 80 dB
Oscillator (OSC) section, temperature stability ..... 5 %
OSC section, amplitude, peak to peak ..... 1.75 V
OSC section, resistance timing / capacitance timing (RTCT) discharge voltage ..... 1 V
OUTPUT section, peak output current (C_{OUT} = 1 nF) ..... 1 A

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Absolute maximum ratings apply to operation in a heavy ion environment as per Table IB. For applications that operate outside a heavy ion environment, the 14.7 V absolute maximum rating increases to 16.5 V.
3/ The HBM rating is 250 V for product having a date code of 1036 or earlier. The HBM rating is 2,000 V for product beginning with date code 1037.
4/ θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.
5/ All voltages are with respect to GND.
6/ The values shown reflect T_A = +25°C operation and are not guaranteed.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):	
Device types 01, 02, 03, 04	100 krads(Si) 7/
Device types 05, 06, 07, 08	100 krads(Si) 8/
Maximum total dose available (dose rate ≤ 0.01 rads(Si)/s):	
Device type 05, 06, 07, 08, 09, 10, 11, 12	50 krads(Si) 8/ 9/
Single event phenomenon (SEP):	
Single event latchup (SEL) observed requiring a power cycle to recover operation at effective LET (see 4.4.4.3)	> 43 MeV/(mg/cm^2) and ≤ 80 MeV/(mg/cm^2) 10/ 11/ 12/
No Single event latchup (SEL) occurs at effective LET (see 4.4.4.3)	≤ 43 MeV/(/mg/cm^2) 10/ 11/
No Single event burnout (SEB) at V_{DD} ≤ 13.5 V with an angle of incidence of 0 degrees for ion LET (see 4.4.4.3)	≤ 80 MeV/(mg/cm^2) 10/ 11/
No Single event burnout (SEB) at V_{DD} ≤ 14.4 V with an angle of incidence of 60 degrees for ion LET (see 4.4.4.3)	≤ 43 MeV/(mg/cm^2) 10/ 11/
No Single event transient (SET) (ΔV_{OUT} within ±3%) at LET (see 4.4.4.3)	≤ 40 MeV/(mg/cm^2) 10/ 11/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

7/ Device types 01, 02, 03, and 04 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si) .

8/ Device types 05, 06, 07, and 08 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

9/ Device types 09, 10, 11, and 12 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 50 krads(Si).

10/ SEP tests performed with V_{REF} bypass capacitor of 0.22 µF and FSW = 200 kHz. SEB and SEL tests done on a stand alone open loop configuration. For SEL, no latch up requiring manual intervention were observed. SET tests done in a closed loop configuration. The (ΔV_{OUT}) was measured across bulk capacitor of the application.

11/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer's SEE test report for more information.

12/ This is a non-destructive event in which part operation is stopped and which requires a power cycle to recover operation. The part does not enter a high current state. See the manufacturer's SEE report for more information.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Undervoltage lockout section							
START threshold voltage			1,2,3	01,02, 05,06, 09,10	6.5	7.5	V
				03,04, 07,08, 11,12	8.0	9.0	
STOP threshold voltage			1,2,3	01,02, 05,06, 09,10	6.1	6.9	V
				03,04, 07,08, 11,12	7.3	8.0	
Startup current	I_{DD}	V_{DD} < START threshold	1,2,3	All		125	µA
		M,D,P,L,R	1			500	
Operating current	I_{DD}	3/	1,2,3	All		4.0	mA
Operating supply current	I_D	Includes 1 nF GATE loading	1,2,3	All		5.5	mA
Reference voltage section							
Overall accuracy	V_{REF}	Over line (V_{DD} = 9 V to 13.2 V), load of 1 mA and 10 mA, temperature	1,2,3	All	4.925	5.050	V
Current limit, sourcing			1,2,3	All	-20		mA
Current limit, sinking			1,2,3	All	5		mA
Current sense section							
Input bias current	I_{IB}	V_{CS} = 1 V	1,2,3	All	-1.0	1.0	µA
Input signal, maximum			1,2,3	All	0.97	1.03	V
Gain, $A_{CS} = \Delta V_{COMP} / \Delta VCS$		0 < V_{CS} < 910 mV, V_{FB} = 0 V	1,2,3	All	2.5	3.5	V/V
CS to OUT delay			9,10,11	All		55	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section							
Reference voltage	V_{REF}	$V_{FB} = V_{COMP}$	1,2,3	All	2.475	2.530	V
FB input bias current	FBI_{IB}	V_{FB} = 0 V	1,2,3	All	-1.0	1.0	µA
COMP sink current		V_{COMP} = 1.5 V, V_{FB} = 2.7 V	1,2,3	All	1.0		mA
COMP source current		V_{COMP} = 1.5 V, V_{FB} = 2.3 V	1,2,3	All	-0.4		mA
COMP high level output voltage	V_{OH}	V_{FB} = 2.3 V	1,2,3	All	4.80	V_{REF}	V
COMP low level output voltage	V_{OL}	V_{FB} = 2.7 V	1,2,3	All	0.4	1.0	V
Oscillator section							
Frequency accuracy		Initial	4,5,6	All	48	53	kHz
Frequency variation with V_{DD}		$(f_{13.2\ V} - f_{9\ V}) / f_{12\ V}$	4,5,6	All		1.0	%
Discharge current	I_{DC}	RTCT = 2.0 V	1,2,3	All	6.5	8.5	mA
Output section							
V_{OUT} differential high side	V_{ODHS}	V_{DD} – OUT, I_{OUT} = -100 mA	1,2,3	All		2.0	V
V_{OUT} differential low side	V_{ODLS}	OUT – GND, I_{OUT} = 100 mA	1,2,3	All		2.0	V
Rise time	t_r	C_{OUT} = 1 nF	9,10,11	All		60	ns
Fall time	t_f	C_{OUT} = 1 nF	9,10,11	All		40	ns
OUTPUT OFF state leakage current		V_{DD} = 5 V	1,2,3	All		50	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse width modulation (PWM) section							
Maximum duty cycle		COMP = V_{REF}	4,5,6	01,03, 05,07, 09,11	94.0		%
				02,04, 06,08, 10,12	47.0		
Minimum duty cycle		COMP = GND	4,5,6	All		0	%

1/ RHA device types 01, 02, 03, and 04 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation. However, device types 01, 02, 03, and 04 are only tested at the "R" level accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein). Device types 01, 02, 03, and 04 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects.

RHA device types 05, 06, 07, and 08 supplied to this drawing will meet all levels M, D, P, L, and R of irradiation for condition A and meet all levels M, D, P, and L for condition D. However, device types 05, 06, 07, and 08 are only tested at the "R" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

RHA device types 09, 10, 11, and 12 supplied to this drawing will meet all levels M, D, P, and L for condition D. However, device types 09, 10, 11, and 12 are only tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Unless otherwise specified, V_{DD} = 13.2 V, resistance timing (RT) = 10 kΩ, and capacitance timing (CT) = 3.3 nF.

3/ This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Temperature (T_A)	Biased V_{DD}	Effective linear energy transfer (LET) and angle of incidence
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	SEL Observed 4/	+125°C ±10° 5/	13.5 V	> 43 MeV/(mg/cm^2) at 0°, > 43 MeV/(mg/cm^2) at 60° and ≤ 80 MeV/(mg/cm^2) at 0°
	No SEL 6/	+125°C ±10° 5/	14.7 V	≤ 43 MeV/(mg/cm^2) at 0°
	No SEB 6/	+125°C ±10° 5/	13.5 V	≤ 80 MeV/(mg/cm^2) at 0°
			14.4 V	≤ 43 MeV/(mg/cm^2) at 60°
	No SET 6/ (ΔV_{OUT} within ±3%)	+25°C ±10° 7/	13.5 V	≤ 40 MeV/(mg/cm^2) at 0°

1/ For single event phenomena (SEP) test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer's SEE test report for more information.
4/ This is a non-destructive event in which part operation is stopped and which requires a power cycle to recover operation. The part does not enter a high current state. See the manufacturer's SEE report for more information.
5/ The worst case temperature, T_A = +125°C ±10° for latch up and burn-out.
6/ SEP tests performed with V_{REF} bypass capacitor of 0.22 μF and FSW = 200 kHz. SEB and SEL tests done on a stand alone open loop configuration. For SEL, no latch up requiring manual intervention were observed. SET tests done in a closed loop configuration. The (ΔV_{OUT}) was measured across bulk capacitor of the application.
7/ The worst case temperature, T_A = +25°C ±10° for SET.

Case X

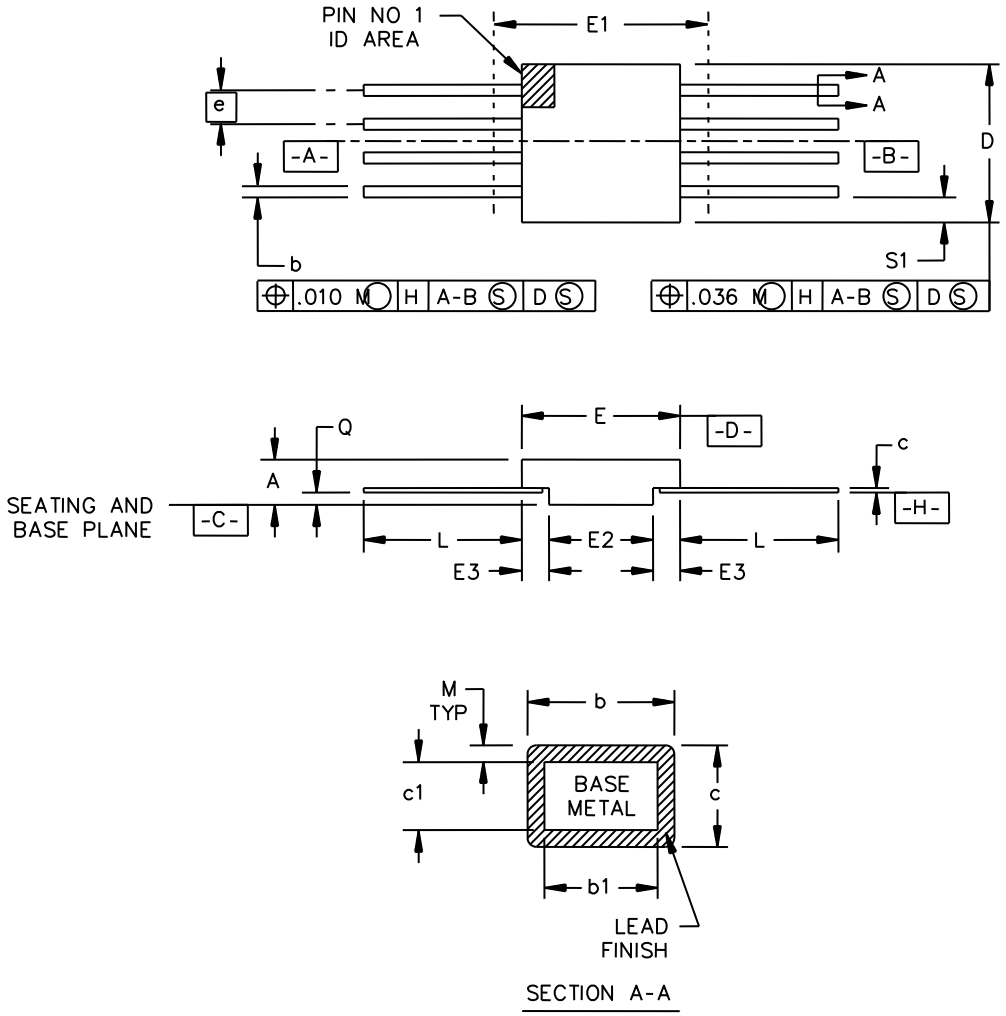


FIGURE 1. Case outline.

Case X – continued.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.070	0.115	1.18	2.92	
b	0.015	0.022	0.38	0.56	
b1	0.015	0.019	0.38	0.48	
c	0.004	0.009	0.10	0.23	
c1	0.004	0.007	0.10	0.18	
D	0.245	0.265	6.22	6.73	4
E	0.245	0.265	6.22	6.73	
E1	---	0.280	---	7.11	4
E2	0.170	0.180	4.32	4.57	
E3	0.030	---	0.76	---	8
e	0.050 BSC		1.27 BSC		
k	---	---	---	---	3
L	0.250	0.370	6.35	9.40	
Q	0.026	---	0.66	---	9
S1	0.005	---	0.13	---	7
M	---	0.0015	---	0.04	
N	8		8		

NOTES:
1. The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
3. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
6. N is the maximum number or terminal positions.
7. Measure dimension S1 at all four corners.
8. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
9. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outline – Continued.

Device types	01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	
Case outlines	P and X	
Terminal number	Terminal symbol	Description
1	COMP	COMP is the output of the error amplifier and the input of the PWM comparator.
2	FB	The output voltage feedback is connected to the inverting input of the error amplifier through this pin.
3	CS	Current sense input to the PWM comparator.
4	RTCT	Oscillator timing control pin.
5	GND	GND is the power and small signal reference ground for all functions.
6	OUT	Drive output to the power switching device
7	V_{DD}	V_{DD} is the power connection for the device.
8	V_{REF}	The 5.00 V reference voltage output.

FIGURE 2. Terminal connections.

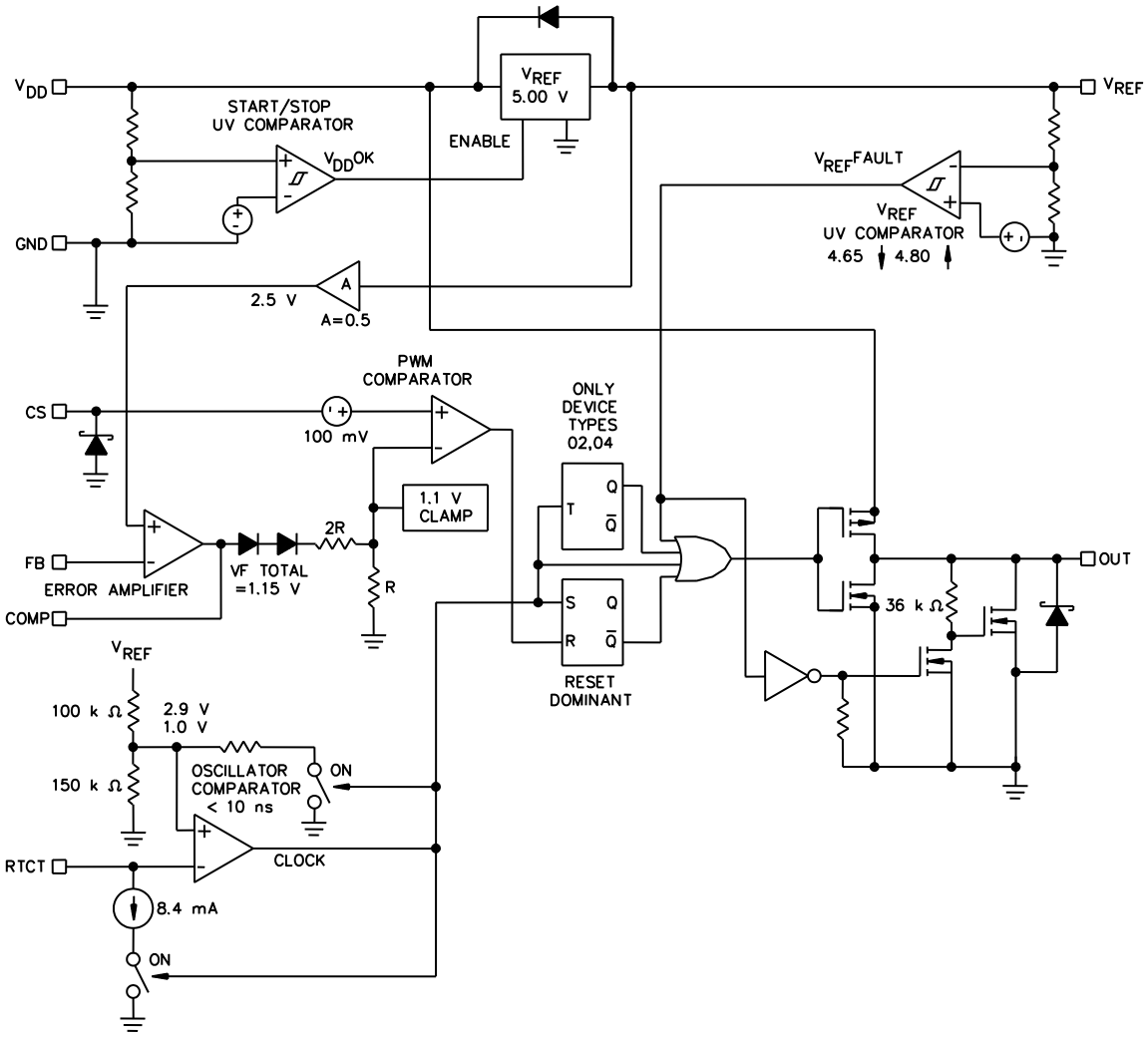


FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	---	1,4,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4, 1/ 2/ 5,6,9,10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4, 2/ 5,6,9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9	As specified in QM plan

1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroup 1 and deltas.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and life test delta parameters. (T_A = +25°C). 1/ 2/

Parameters	Symbol	Min	Max	Units
Reference output voltage	V_{REF}	-50	50	mV
CT discharge current	I_{DC}	-0.5	0.5	mA
Error amp input bias current	FBI_{IB}	-0.2	0.2	μA
Operating supply current	I_D	-0.5	0.5	mA

1/ Deltas are performed at room temperature.
2/ Applies to device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, and 12.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, 03, 04, 05, 06, 07, and 08. In addition, for device types 05, 06, 07, 08, 09, 10, 11, and 12 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq \text{angle} \leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C $\pm$10° for SET. The test temperature shall be +125°C $\pm$10° for SEB and SEL.

f. For SEL, SEB, and SET test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of burnouts (SEB).

d. Number of transients (SET).

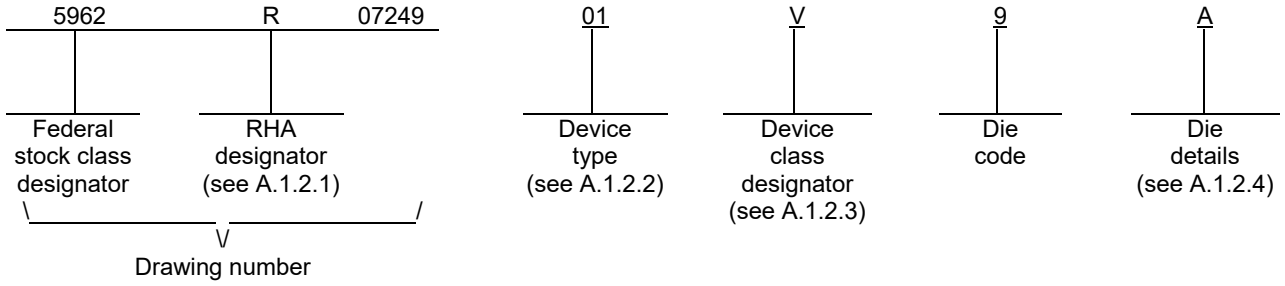
e. Occurrence of latch-up (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-07249

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic	Rising under voltage lockout	Maximum duty cycle	Circuit function
01	ISL78840ASRH	7.0 V	100 %	Pulse width modulator controller
02	ISL78841ASRH	7.0 V	50 %	Pulse width modulator controller
03	ISL78843ASRH	8.4 V	100 %	Pulse width modulator controller
04	ISL78845ASRH	8.4 V	50 %	Pulse width modulator controller
05	ISL78840ASEH	7.0 V	100 %	Pulse width modulator controller
06	ISL78841ASEH	7.0 V	50 %	Pulse width modulator controller
07	ISL78843ASEH	8.4 V	100 %	Pulse width modulator controller
08	ISL78845ASEH	8.4 V	50 %	Pulse width modulator controller
09	ISL738840ASEH	7.0 V	100 %	Pulse width modulator controller
10	ISL738841ASEH	7.0 V	50 %	Pulse width modulator controller
11	ISL738843ASEH	8.4 V	100 %	Pulse width modulator controller
12	ISL738845ASEH	8.4 V	50 %	Pulse width modulator controller

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

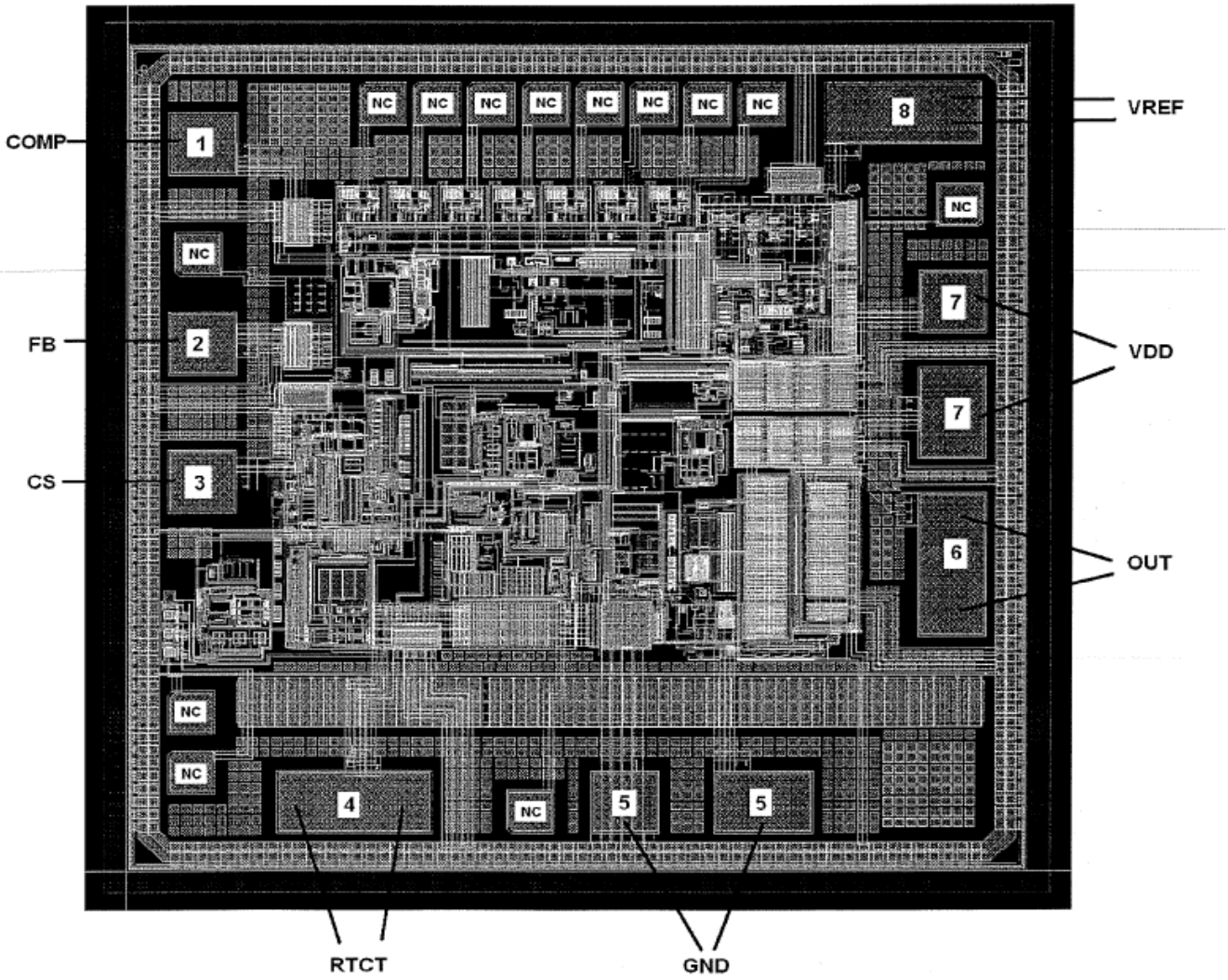


FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: X = 2030 μm (80 mils). Y = 2030 μm (80 mils).
Die thickness: 19 mils ±1 mil

Interface materials.
Top metallization: AlCu (0.5%), 2.7 μm ±0.4 μm
Backside metallization: Silicon

Glassivation.
Type: Silicon oxide and silicon nitride
Thickness: 0.3 μm ±0.03 μm and 1.2 μm ±0.12 μm

Substrate: Silicon. Junction isolation.

Assembly related information.
Substrate potential: Unbiased
Special assembly instructions: 1) CTRT, OUT, and V_{REF} must be double bonded (two wires).
2) GND and V_{DD} must have both bond pads connected.

FIGURE A-1. Die bonding pad locations and electrical functions - continued

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-02

Approved sources of supply for SMD 5962-07249 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0724901QPC	34371	ISL78840ASRHQD
5962R0724902QPC	34371	ISL78841ASRHQD
5962R0724903QPC	34371	ISL78843ASRHQD
5962R0724904QPC	34371	ISL78845ASRHQD
5962R0724901QXC	34371	ISL78840ASRHQF
5962R0724902QXC	34371	ISL78841ASRHQF
5962R0724903QXC	34371	ISL78843ASRHQF
5962R0724904QXC	34371	ISL78845ASRHQF
5962R0724904Q9A	34371	ISL78845ASRHQX
5962R0724904TXC	34371	ISL78845ASRHTF
5962R0724901VPC	34371	ISL78840ASRHVD
5962R0724902VPC	34371	ISL78841ASRHVD
5962R0724903VPC	34371	ISL78843ASRHVD
5962R0724904VPC	34371	ISL78845ASRHVD
5962R0724905VPC	34371	ISL78840ASEHVD
5962R0724906VPC	34371	ISL78841ASEHVD
5962R0724907VPC	34371	ISL78843ASEHVD
5962R0724908VPC	34371	ISL78845ASEHVD
5962L0724909VPC	34371	ISL738840ASEHVD
5962L0724910VPC	34371	ISL738841ASEHVD
5962L0724911VPC	34371	ISL738843ASEHVD
5962L0724912VPC	34371	ISL738845ASEHVD
5962R0724901VXC	34371	ISL78840ASRHVF
5962R0724902VXC	34371	ISL78841ASRHVF
5962R0724903VXC	34371	ISL78843ASRHVF
5962R0724904VXC	34371	ISL78845ASRHVF

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0724905VXC	34371	ISL78840ASEHVF
5962R0724906VXC	34371	ISL78841ASEHVF
5962R0724907VXC	34371	ISL78843ASEHVF
5962R0724908VXC	34371	ISL78845ASEHVF
5962L0724909VXC	34371	ISL738840ASEHVF
5962L0724910VXC	34371	ISL738841ASEHVF
5962L0724911VXC	34371	ISL738843ASEHVF
5962L0724912VXC	34371	ISL738845ASEHVF
5962R0724901V9A	34371	ISL78840ASRHVX
5962R0724902V9A	34371	ISL78841ASRHVX
5962R0724903V9A	34371	ISL78843ASRHVX
5962R0724904V9A	34371	ISL78845ASRHVX
5962R0724905V9A	34371	ISL78840ASEHVX
5962R0724906V9A	34371	ISL78841ASEHVX
5962R0724907V9A	34371	ISL78843ASEHVX
5962R0724908V9A	34371	ISL78845ASEHVX
5962L0724909V9A	34371	ISL738840ASEHVX
5962L0724910V9A	34371	ISL738841ASEHVX
5962L0724911V9A	34371	ISL738843ASEHVX
5962L0724912V9A	34371	ISL738845ASEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.