

DESIGN AND CONSTRUCTION INFORMATION, SEMICONDUCTOR
MIL-PRF-19500

Plant Name and Address	MIL-PRF-19500 Associated Spec.(s)	Semiconductor Device Type(s)	Test Report No. 19500 - -
			Part Name (SCR, FET, etc.)
			Date Rev.
Signature of Responsible Official		*ESD Classification Level	Manufacturer's Die Designation:

* WAFER FABRICATION FACILITY/LOCATION: _____ BEGINNING LOT IDENTIFICATION CODE: _____

[1] CONSTRUCTION TECHNIQUE (Alloy, Planar, etc.): _____

[2] SUBSTRATE:

[a] Material: _____ Silicon _____ Germanium _____ Other _____

[b] Crystal Orientation: _____ (e.g., 111)

[c] Doping Material: _____

[d] Resistivity: _____ Ohm-cm

[3] EPITAXIAL DEPOSITION:

[a] Doping Material: _____

[b] Nominal Thickness: _____

[c] Resistivity: _____ Ohm-cm

[4] DIFFUSION PROFILE:

PROCESS STEP	IDENTITY (N+, Emitter, etc.)	PROCESS TYPE (Alloy, Diffusion, Ion implant, etc.)	DOPANT (As, P, B, Sb, etc.)
1			
2			
3			
4			

[5] SURFACE DEPOSITIONS:

DEPOSITION	MATERIAL	DEPOSITION TECHNIQUE	THICKNESS Min. (Å)	THICKNESS Nom. (Å)
PASSIVATION (Under Metal)				
METALLIZATION (Front)				
METALLIZATION (Back)				
GLASSIVATION (Over Front Metal)				
ORGANIC DIE PROTECTIVE COATING				

[6] LAYOUT GEOMETRY:

[a] Die Size (Nominal): _____ x _____ Mils

[b] Die Thickness (Nominal): _____ Mils

[c] Bond Pad Size (Minimum): _____ x _____ Mils, or _____ Mils Dia.

[7] METALLIZATION CALCULATED MAX. INTERNAL CONDUCTOR CURRENT DENSITY: _____ A/cm²

[8] PHOTOGRAPH OR DRAWING OF THE DIE SURFACE IS ATTACHED _____ YES _____ NO,

Previously submitted on _____ (DATE)

PACKAGE PROPERTIES (TRANSISTORS, ETC.)

Plant Name and Address:

[1] CASE TYPE IDENTIFICATION:

[a] JEDEC Case Outline: _____

[b] Company Case Ident. Number: _____

[2] PACKAGE MATERIALS

DEVICE TYPES:

Part	Material	Underplating & Plating Material	Underplating & Plating Nominal Thickness	Spec. or Dwg. No.
___ Glass-filled Header ___ Solid				
Die-Mount Base				
Lid				
Bonding Posts				
Glass Type for Post Isolation				
Tubulations				
External Leads				

* Qualified Thermal Impedance Limits; Screening _____ °C/W or ΔVsd (max); QCI _____ °C/W or % ΔVsd shift (max)

[3] DIE ATTACH:

[a] Material: _____

[b] Method: _____

[c] Temperature: _____ °C

[4] INTERNAL WIRE BONDING:

Wire Bond	Type Bond	Nr.	Wire Material	Wire Diameter	E, B, etc.

[5] PACKAGE SEALING TECHNIQUE:

[a] Sealing Atmosphere: _____ Moisture Content _____ ppm, max.

[b] Sealing Method: _____ (Oven or Furnace Temperature _____ °C)

[c] Sealing Material: _____

[d] Free Cavity Volume: _____ cc

[e] Organic Material, if any: _____ Cure Cycle TIME _____ TEMP _____ °C

[6] ELEMENT ELECTRICALLY CONNECTED TO CASE (i.e. Collector): _____

[7] POWER AT 25 °C CASE TEMPERATURE: ___FOUR WATTS OR HIGHER ___LESS THAN FOUR WATTS

[8] DESCRIPTION. THE FOLLOWING ITEMS ARE ATTACHED:

[a] Photographs or drawing of internal configuration (header layout and post bonds including die orientation and internal wire runs) _____ YES _____ NO

PREVIOUSLY SUBMITTED: _____ (DATE)

[b] Description of unique construction detail not covered above. _____ YES _____ NO

PACKAGE PROPERTIES (DIODES)

Plant Name and Address:

[1] CASE TYPE IDENTIFICATION:

[a] JEDEC Case Outline: _____

[b] Company Case Ident. Number: _____

[2] PACKAGE MATERIALS

DEVICE TYPES:

Part	Material	Underplating & Plating Material	Underplating & Plating Nominal Thickness	Spec. or Dwg. No.
Glass or Body				
Stud or Base				
Plugs or Lid				
Tubulation				
External Leads				

* Qualified Thermal Impedance Limits; Screening _____ °C/W or ΔVsd (max); QCI _____ °C/W or % ΔVsd shift (max)

[3] DIODE OHMIC CONTACTS (METHODS AND MATERIALS)::

[a] CATHODE:

1. Type Contact: _____

2. Materials: _____

3. Temp: _____ °C

[b] ANODE:

1. Type Contact: _____

2. Materials: _____

3. Temp: _____ °C

[c] MULTIPLE DIE INTERCONNECT: (PAIRS, ARRAYS, ETC.)

1. Type Contact: _____

2. Materials: _____

3. Temp: _____ °C

[4] PACKAGE SEALING TECHNIQUE:

[a] Sealing Atmosphere: _____ Moisture Content _____ ppm, max.

[b] Sealing Method: _____

[c] Sealing Material: _____

[d] Sealing Temperature: _____ °C

[e] Free Cavity Volume: _____ cc

[f] Organic Material, if any: _____ Cure Cycle TIME _____ TEMP _____ °C

[5] ELEMENT ELECTRICALLY CONNECTED TO CASE (i.e. Cathode): _____

[7] METHOD USED TO SHIELD DIE FROM LIGHT: _____

[8] DESCRIPTION. THE FOLLOWING ITEMS ARE ATTACHED:

[a] Photographs or drawing of internal configuration (header layout and post bonds including die orientation and internal wire runs) _____ YES _____ NO

PREVIOUSLY SUBMITTED: _____ (DATE)

[b] Description of unique construction detail not covered above. _____ YES _____ NO