

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. Delete device class M references. Delete footnote 6/ and add two footnotes under paragraph 1.3. Make corrections to dimensions A, D, E, e, and L to case X as specified under figure 1. - ro	13-06-13	C. SAFFLE

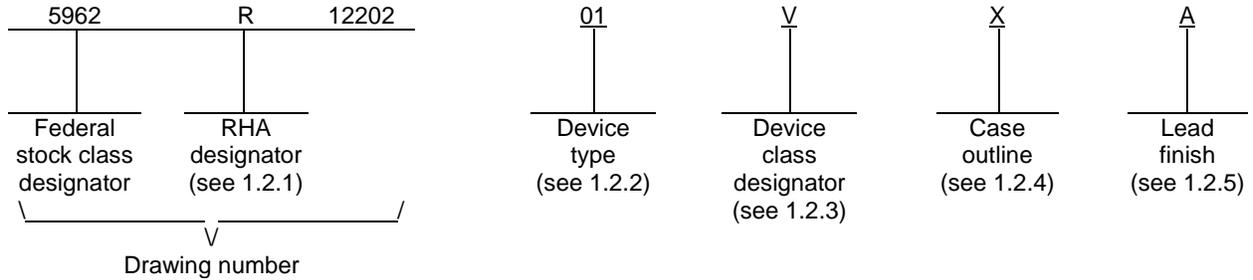
REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY RICK OFFICER		<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY RAJESH PITHADIA																				
	APPROVED BY CHARLES F. SAFFLE		<p align="center">MICROCIRCUIT, LINEAR, SYNCHRONOUS BUCK REGULATOR, MONOLITHIC SILICON</p>																		
	DRAWING APPROVAL DATE 12-05-23																				
	REVISION LEVEL A		SIZE A	CAGE CODE 67268	5962-12202																
		SHEET		1 OF 34																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	ISL70002SEH	Synchronous buck regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	64	Quad flat pack
Y	See figure 1	64	Quad flat pack with heat sink

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 2

1.3 Absolute maximum ratings. 1/ 2/

AVDD	AGND – 0.3 V to AGND + 6.2 V
DVDD	DGND – 0.3 V to DGND + 6.2 V
LXx, PVINx	PGNDx – 0.3 V to PGNDx + 6.2 V 3/
AVDD – AGND, DVDD – DGND	PVINx – PGNDx ± 0.3 V
Signal pins	AGND – 0.3 V to AVDD + 0.3 V 4/
Digital control pins	DGND – 0.3 V to DVDD + 0.3 V 5/
PGOOD	DGND – 0.3 V to DGND + 6.2 V
Soft start (SS)	DGND – 0.3 V to DGND + 2.5 V
Power dissipation (PD) :	
Case outline X:	
T _A = +25°C	3.67 W
T _A = +125°C	0.73 W
T _C = +25°C	83.3 W
T _C = +125°C	16.6 W
Case outline Y:	
T _A = +25°C	7.34 W
T _A = +125°C	1.46 W
T _C = +25°C	178.5 W
T _C = +125°C	35.6 W
Operating junction temperature range (T _J)	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ _{JC}) :	
Case outline X	1.5°C/W 6/
Case outline Y	0.7°C/W 7/
Thermal resistance, junction-to-ambient (θ _{JA}) :	
Case outline X	34°C/W 8/
Case outline Y	17°C/W 9/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Absolute maximum ratings assume operation in a heavy ion environment.
- 2/ Unless otherwise specified, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SCO = SC1 = 3 V to 5.5 V and GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0 V.
- 3/ The 6.2 V absolute maximum rating must be met for a 20 MHz bandwidth limited observation at the device pins. In addition, for a 600 MHz bandwidth limited observation, the peak transient voltage on PVINx (measured to PGNDx) must be less than 7.1 V with a duration above 6.2 V of less than 10 ns, and the peak transient voltage on LXx (measured to PGNDx) must be less than 7.9 V with a duration above 6.2 V of less than 10 ns.
- 4/ EN, FB, ISHx, ISHREFx, OCx, OCSSx, PORSEL, and REF pins.
- 5/ FSEL, GND, ISHCOM, ISEN, ISHEN, ISHRSL, M/S, SYNC, SC0, SC1, TDI, TDO, and TPGM pins.
- 6/ For θ_{JC}, the case temperature location is the center of the package underside.
- 7/ For θ_{JC}, the case temperature location is the center of the exposed metal heatsink on the package underside.
- 8/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board.
- 9/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 3

1.4 Recommended operating conditions. 2/

AVDD	AGND + 3 V to 5.5 V
DVDD	DGND + 3 V to 5.5 V
PVINx	PGNDx + 3 V to 5.5 V
AVDD – AGND, DVDD – DGND	PVINx PGNDx ± 0.1 V
Signal pins	AGND to AVDD 4/
Digital control pins	DGND to DVDD 5/
REF, SS	Internally set
GND, TDI, TDO, TPGM	DGND
ILXx (T _J ≤ +150°C)	0 A to 1.2 A
Ambient operating temperature range (T _A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 10/
Maximum total dose available (dose rate ≤ 0.01 rads(Si)/s)	50 krads(Si) 10/

Single event phenomenon (SEP):

Destructive single event effects (SEE):

No SEL occurs at effective linear energy transfer (LET) (see 4.4.4.4)	≤ 86 MeV/(mg/cm ²) 11/
No SEB observed at effective linear energy transfer (LET) (fluence = 2.4 x 10 ⁷ ions/cm ²)	< 86 MeV/(mg/cm ²) 11/

Nondestructive single event effects (SEE):

No SET observed at effective LET (LX pulse perturbation < 1, at output current 14 A at 1.0 V)..	< 86 MeV/(mg/cm ²) 11/
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Single event functional interrupt (SEFI) configured as current share master and slave mode.

No SEFI observed at surface LET (V _{IN} = 5.5 V, cross-section = 3.03 x 10 ⁻⁸ cm ²)	≤ 43 MeV/(mg/cm ²) 11/
No SEFI observed at surface LET (V _{IN} = 3.0 V, cross-section = 2.26 x 10 ⁻⁸ cm ²)	≤ 43 MeV/(mg/cm ²) 11/

10/ The device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

11/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP/SEE characteristics but, are not production tested unless specified by the customer through the purchase order or contract. For more information on destructive SEE (SEB/SEGR) test results, customers are requested to contact manufacturer.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 4

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

JEDEC Solid State Technology Association

EIA/JEDEC 51-5 - Extension of Thermal Conductivity Test Board Standards for Packages with Direct Thermal Attachment Mechanisms
EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at <http://www.jedec.org>)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 5

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 6

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply section.							
Operating supply current (current share disabled)	IOP1	V _{IN} = 5.5 V	1,2,3	01		105	mA
		V _{IN} = 3.6 V				65	
Standby supply current (current share disabled)	ISBY1	V _{IN} = 5.5 V, EN = GND, ISHEN = GND	1,2,3	01		6	mA
		V _{IN} = 3.6 V, EN = GND, ISHEN = GND				4	
Operating supply current (current share enabled, current share master)	IOP2	V _{IN} = ISHEN = 5.5 V, ISHCOM = open circuit	1,2,3	01		120	mA
Operating supply current (current share enabled, current share slave)	IOP3	V _{IN} = ISHEN = ISHSL = 5.5 V, ISHCOM pulled to V _{IN} with 1 kΩ, M/S = GND, ISHx = ISHREFx = -100 μA, SYNC = external 1 MHz clock	1,2,3	01		120	mA
Standby supply current (current share enabled, current share slave)	ISBY2	V _{IN} = ISHEN = ISHSL = 5.5 V, EN = M/S = GND, SYNC = external 1 MHz clock	1,2,3	01		7	mA
		V _{IN} = ISHEN = ISHSL = 5.5 V, M/S = GND, SYNC external 1 MHz clock, ISHCOM = GND				11	
Output voltage and current section							
Reference voltage	V _{REF}		1,2,3	01	0.594	0.606	V
		M,D,P,L,R	1		0.594	0.604	
Output voltage tolerance <u>3/ 4/</u>	V _{OUT}	V _{OUT} = 0.8 V to 2.5 V for V _{IN} = 4.5 V to 5.5 V,	1,2,3	01	-2	2	%
		V _{OUT} = 0.8 V to 2.5 V for V _{IN} = 3 V to 3.6 V, I _{OUT} = 0 A to 12 A			-2	2	
Error amp input offset voltage	V _{OS}	V _{IN} = 5.5 V, V _{REF} = 600 mV, test mode	1,2,3	01	-1	3	mV

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 7

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage and current section - continued.							
Feedback (FB) input leakage current	FB _{LKG}	V _{IN} = 5.5 V, V _{FB} = 600 mV	1,2,3	01	-1.5	1.5	μA
Sustained output current <u>5/</u>	I _{OUT}	V _{IN} = 3 V, V _{OUT} = 1.8 V, OCA = OCB = P _{VIN}	1,2,3	01	16		A
Pulse width modulator control logic section							
Internal oscillator tolerance	OSC	FSEL = V _{IN} or GND	4,5,6	01	-15	15	%
External oscillator range	EXT _{OSC}	M/S = GND	4,5,6	01	0.4	1.2	MHz
Minimum LXx on time	TON _{MIN}	V _{IN} = 5.5 V, test mode	1,2,3	01		275	ns
		V _{IN} = 3 V, test mode				300	
Minimum LXx off time	TOFF _{MIN}	V _{IN} = 5.5 V, test mode	1,2,3	01		50	ns
		V _{IN} = 3 V, test mode				50	
PORSEL, Master/slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL, input voltage	V _{IH}	Input high threshold	1,2,3	01	V _{IN} - 0.5		V
	V _{IL}	Input low threshold				0.5	
PORSEL, master/slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL input leakage current	INLKG	V _{IN} = 5.5 V	1,2,3	01	-1	1	μA
Synchronization (SYNC) input voltage	SYNC V _{IH}	Input high threshold, M/S = GND	1,2,3	01	2.3		V
	SYNC V _{IL}	Input low threshold, M/S = GND				1	
Synchronization (SYNC) input leakage voltage	SYNC LKG	V _{IN} = 5.5 V, M/S = GND, SYNC = V _{IN} or GND	1,2,3	01	-1	1	μA
Synchronization (SYNC) output voltage	SYNC V _{OH}	V _{IN} - V _{OH} at I _{OH} = -1 mA	1,2,3	01		0.4	V
	SYNC V _{OL}	V _{OL} at I _{OL} = 1 mA				0.4	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 8

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power blocks section							
Upper device r _{DS(ON)}	URON	V _{IN} = 3 V, 4 A load, all power blocks in parallel, test mode	4,5,6	01		40	mΩ
Lower device r _{DS(ON)}	LRON	V _{IN} = 3 V, 4 A load, all power blocks in parallel, test mode	4,5,6	01		30	mΩ
LXx output leakage	LXLKG	V _{IN} = 5.5 V, EN = LXx = GND, single LXx output	1,2,3	01	-1		μA
		V _{IN} = LXx = 5.5 V, EN = GND, single LXx output				10	
Deadtime <u>4/</u>	TDEAD	Within single power block or between power blocks	9,10,11	01	2.2		ns
Power on reset section							
VIN POR	PORHI	Rising threshold, PORSEL = V _{IN}	1,2,3	01	4.1	4.45	V
	POR HI V _{hys}	Hysteresis, PORSEL = V _{IN}			225	425	mV
	PORGND	Rising threshold, PORSEL = GND			2.65	2.95	V
	PORGND V _{hys}	Hysteresis, PORSEL = GND			70	240	mV
Enable (EN) input voltage	ENThr	Rising / falling threshold	1,2,3	01	0.56	0.64	V
Enable (EN) input leakage current	ENLKG	V _{IN} = 5.5 V, EN = V _{IN} or GND	1,2,3	01	-3	3	μA
Enable (EN) sink current	ENSNK	EN = 0.3 V	1,2,3	01	6.4	16.6	μA
Soft start section							
Soft start source current	ISSSRC	SS = GND	1,2,3	01	20	27	μA
Soft start discharging on resistance	SSRES		1,2,3	01		4.7	Ω

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 9

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power good signal section.							
Rising threshold	PGOOVTH	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	107	115	%
Rising hysteresis	PGOOVHYS	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	2	5	%
Falling threshold	PGOUVTH	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	85	93	%
Falling hysteresis	PGOUVHYS	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	2	5	%
Power good drive current	PG _{DRV}	V _{IN} = 3 V, PGOOD = 0.4 V, EN = GND	1,2,3	01	7.2		mA
Power good leakage current	PG _{LKG}	V _{IN} = PGOOD = 5.5 V	1,2,3	01		1	μA
Protection features section.							
Undervoltage monitor							
Undervoltage trip threshold	UV _{TRIP}	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	71	79	%
Undervoltage recovery threshold	UV _{REC}	V _{FB} as a % of V _{REF} , test mode	1,2,3	01	84	92	%
Overcurrent monitor.							
Overcurrent trip level <u>6/</u>	OC _{TRIP}	I _{OCx} = 60 μA, test mode	1,2,3	01	5.35	7.35	A
		I _{OCx} = 240 μA, test mode			23	26	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 10

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current share section.							
Slave load current <u>4/ 5/</u>	ISLV	Master load current = 12 A, V _{IN} = 3.3 V, V _{OUT} = 0.8 V, SC1 = ISHSL = M/S = 0, SC0 = ISHEN = FSEL = 1, SYNC = 1 MHz external, 500 nH inductor	1,2,3	01	7	17	A
		Master load current = 12 A, V _{IN} = 3.3 V, V _{OUT} = 1.8 V, SC0 = ISHSL = M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1 MHz external, 500 nH inductor			7	17	
		Master load current = 12 A, V _{IN} = 5.0 V, V _{OUT} = 1.8 V, SC0 = ISHSL = M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1 MHz external, 500 nH inductor			7	17	
		Master load current = 12 A, V _{IN} = 5.0 V, V _{OUT} = 2.5 V, ISHSL = M/S = 0, SC0 = SC1 = ISHEN = FSEL = 1, SYNC = 1 MHz external, 500 nH inductor			7	17	
ISHx, ISHREFx, tristate leakage current	ISHLKG	V _{IN} = 5.5 V, EN = GND	1,2,3	01	-1	1	μA
Master ISHCOM pull up resistance	ISHCOM RUP	ISHCOM = -50 μA	4,5,6	01	6.5	13	kΩ
Slave ISHCOM input leakage current	ISHCOM LKG	V _{IN} = ISHSL = 5.5 V	1,2,3	01	-1	1	μA
Slave ISHCOM pull down resistance	ISHCOM RDN	ISHSL = V _{IN} , EN = GND, ISHCOM = 7.2 mA	1,2,3	01	35	125	Ω

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 11

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current share section – continued.							
Slave ISHCOM input high voltage	ISHCOM V _{IH}	ISHSL = V _{IN}	1,2,3	01	42	62	% of V _{IN}
Slave ISHCOM input low voltage	ISHCOM V _{IL}	ISHSL = V _{IN}	1,2,3	01	26	46	% of V _{IN}
Slave ISHCOM input voltage hysteresis	ISHCOM HYST	ISHSL = V _{IN}	1,2,3	01	7	24	% of V _{IN}
ISHSL input leakage current	ISHSL LKG		1,2,3	01	-1	1	μA
ISHSL input high voltage	ISHSL V _{IH}		1,2,3	01	V _{IN} - 0.5		V
ISHSL input low voltage	ISHSL V _{IL}		1,2,3	01		0.5	V
Slope compensation (SC) referred to V _{OUT}	SC11FS1	SC1 = SC0 = V _{IN}	1,2,3	01	5.9	17.7	A/μs
	SC10FS1	SC1 = V _{IN} , SC0 = GND			3.0	8.8	
	SC01FS1	SC1 = GND, SC0 = V _{IN}			1.5	4.5	
	SC00FS1	SC1 = SC0 = GND			0.7	2.2	
	SC11FS0	FSEL = GND, SC1 = SC0 = V _{IN}			2.9	8.8	
	SC10FS0	FSEL = GND, SC1 = V _{IN} , SC0 = GND			1.4	4.5	
	SC01FS0	FSEL = GND, SC1 = GND, SC0 = V _{IN}			0.7	2.2	
	SC00FS0	FSEL = GND, SC1 = SC0 = GND			0.3	1.2	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 12

TABLE IA. Electrical performance characteristics – Continued.

- 1/ Unless otherwise specified, $V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SCO = SC1 = 3\text{ V to }5.5\text{ V}$; $GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TD0 = TPGM = 0\text{ V}$; $FB = 0.65\text{ V}$; $PORSEL = V_{IN}$ for $4.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ and GND for $V_{IN} < 4.5\text{ V}$; $LXx = SYNC = \text{open circuit}$; OCx is connected to $OCSSx$ with a $10\text{ k}\Omega$; OCx is connected to GND with a $4.99\text{ k}\Omega$ resistor shunted by a 6.8 nF capacitor; $PGOOD$ is pulled up to V_{IN} with a $1\text{ k}\Omega$ resistor; REF is bypassed to GND with a 220 nF capacitor; SS is bypassed to GND with a 100 nF capacitor; $T_A = T_J = -55^\circ\text{C to }+125^\circ\text{C}$.
- 2/ RHA devices supplied to this drawing meet levels M, D, P, L, and R of irradiation for condition A and levels M, D, P, and L for condition D. However, devices are only tested at the R level in accordance with MIL-STD-883, method 1019, condition A and the L level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).
When performing post irradiation electrical measurements for any RHA level, $T_A = +25^\circ\text{C}$ (see 1.5 herein).
- 3/ Limits do not include tolerance of external feedback resistors. The 0 A to 12 A output current range may be reduced by minimum LXx on time and minimum LXx off time specifications.
- 4/ Limits established by characterization or analysis and are not production tested.
- 5/ Tested sequentially on LX2, LX6, and LX9.
- 6/ Tested sequentially on LX2 and LX6 at 535 mA to 735 mA and 2.3 A to 2.6 A.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 13

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP/SEE	Temperature (T _C)	V _{IN}	Linear energy transfer (LET) [MeV/(mg/cm ²)]	Fluence / cross section
01	No SEL	+125°C	6.2 V	Effective LET ≤ 86	<u>3/</u>
	No SEB	+125°C	6.2 V	Effective LET ≤ 86	Fluence = 2.4x10 ⁷ ions/cm ²
	SET observed	+25°C	3 V or 5.5 V	Effective LET = 86	<u>4/</u>
	No SEFI	+25°C	3.0 V	Surface LET = 43	Cross section = 2.26 x 10 ⁻⁸ cm ² <u>5/</u>
	No SEFI	+25°C	5.5 V	Surface LET = 43	Cross section = 3.03 x 10 ⁻⁸ cm ² <u>6/</u>

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ All test conditions using a minimum of 4 units unless otherwise noted.

3/ V_{OUT} = 1.0 V, I_{OUT} = 14 A, fluence = 8 X10⁶ ions/cm², no destructive effects (single device – no current share).
 V_{OUT} = 1.0 V, I_{OUT} = 2 A total, fluence = 4 X10⁶ ions/cm², no destructive effects (two samples configured in current share mode, slave device irradiated, 2 devices tested).

4/ V_{OUT} = 1.0 V, I_{OUT} = 6 A/part, fluence = 4.4 X10⁷ ions/cm², tested in master and slave mode at 3 V and 5.5 V. SET no more than 1 LX pulse perturbation before correction, with a ΔV_{out} < 1%.

5/ No SEFI events observed at surface LET = 43 MeV/(mg/cm²), V_{OUT} = 1.0 V, I_{OUT} = 6 A/part, master/slave mode V_{IN} = 3.0 V and cross section = 2.26 x 10⁻⁸ ions/cm² (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)

6/ No SEFI events observed at surface LET = 43 MeV/(mg/cm²), V_{OUT} = 1.0 V, I_{OUT} = 6 A/part, master/slave mode V_{IN} = 5.5 V and cross section = 3.3 x 10⁻⁸ ions/cm² (SEFI is defined as non-destructive phenomenon similar to a restart or an overcurrent protection (OCP) fault, with a soft start and recovery without requiring external intervention.)

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 14

Case X

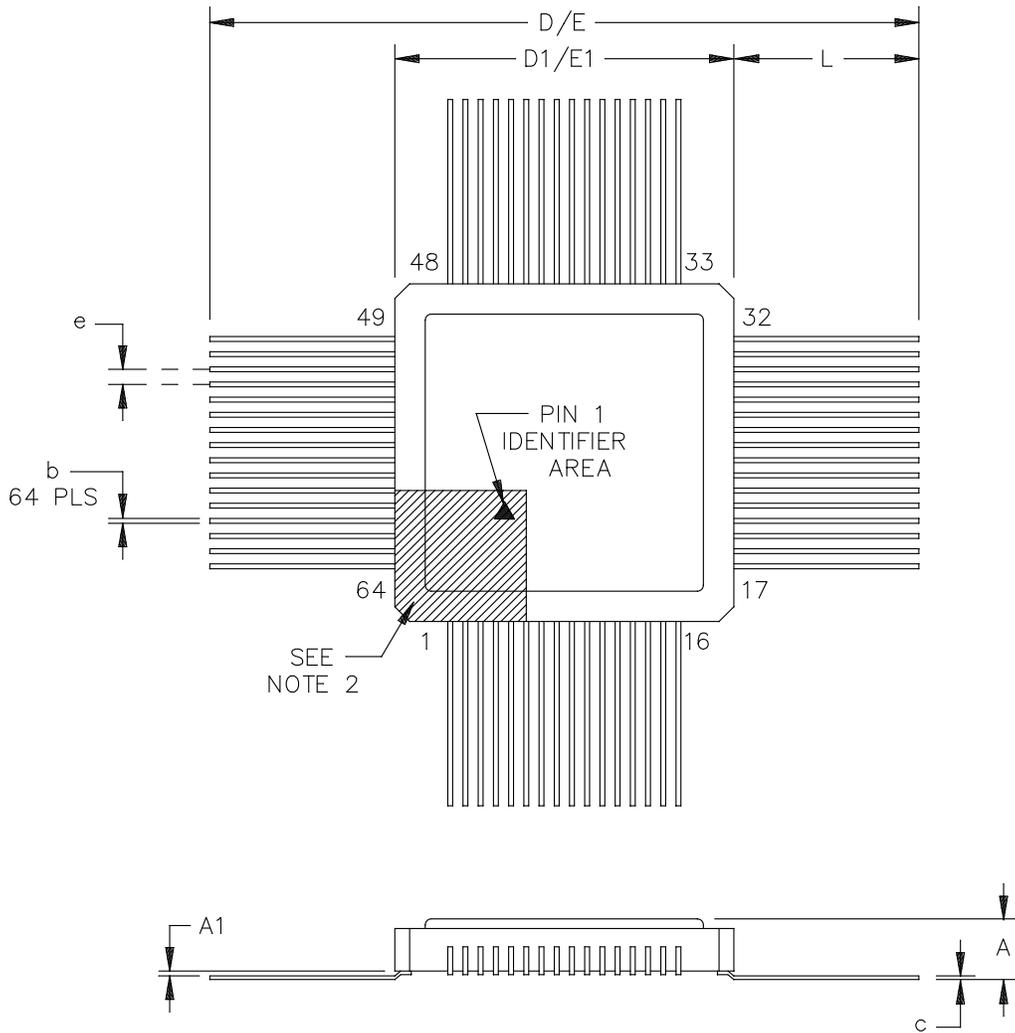


FIGURE 1. Case outlines.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
A

5962-12202

SHEET
15

Case X – continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.075	0.105	1.91	2.67	
A1	0.008 REF		0.20 REF		
b	0.006	0.010	0.15	0.25	
c	0.005	0.0075	0.125	0.188	
D	1.080	1.118	27.43	28.40	
D1	0.547	0.567	13.90	14.40	
E	1.080	1.118	27.43	28.40	
E1	0.547	0.567	13.90	14.40	
e	0.25 BSC		0.635 BSC		
L	0.255	0.290	6.48	7.37	
N	64		64		

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Pin 1 identifier location. Pin 1 is the bottom left pin.

FIGURE 1. Case outlines – continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 16

Case Y

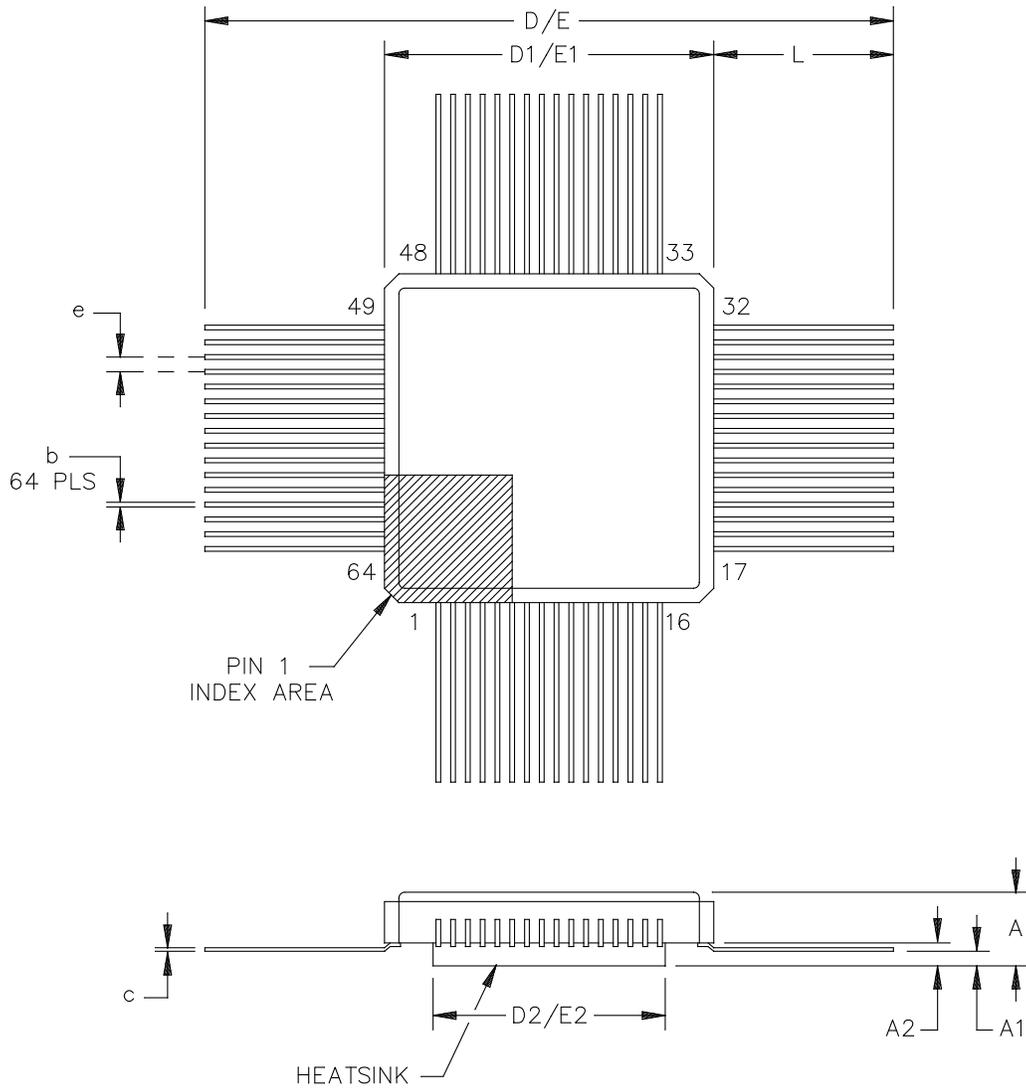


FIGURE 1. Case outlines – continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 17

Case Y – continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.111	0.135	2.82	3.43	
A1	0.026	---	0.66	---	2
A2	0.048 REF		1.22 REF		
b	0.006	0.010	0.15	0.25	
c	0.005	0.0075	0.125	0.188	
D/E	1.080	1.118	27.43	28.40	
D1/E1	0.547	0.567	13.90	14.40	
D2/E2	0.395	0.405	10.03	10.29	
e	0.025 BSC		0.635 BSC		
L	0.255	0.290	6.48	7.37	
N	64		64		

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.

FIGURE 1. Case outlines – continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 18

Device type	01		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	FB	17	PORSEL
2	ISHA	18	TD0
3	ISHREFA	19	TD1
4	ISHB	20	TPGM
5	ISHREFB	21	GND
6	ISHC	22	SYNC
7	ISHREFC	23	PVIN10
8	AVDD	24	LX10
9	AGND	25	PGND10
10	DGND	26	PGND9
11	DVDD	27	LX9
12	SS	28	PVIN9
13	PGOOD	29	M/S
14	ISHCOM	30	FSEL
15	ISHSL	31	NC
16	ISHEN	32	PVIN8

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 19

Device type	01		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
33	LX8	49	PVIN3
34	PGND8	50	NC
35	PGND7	51	SC0
36	LX7	52	SC1
37	PVIN7	53	PVIN2
38	PVIN6	54	LX2
39	LX6	55	PGND2
40	PGND6	56	PGND1
41	PGND5	57	LX1
42	LX5	58	PVIN1
43	PVIN5	59	EN
44	PVIN4	60	OCSSB
45	LX4	61	OCB
46	PGND4	62	OCSSA
47	PGND3	63	OCA
48	LX3	64	REF

FIGURE 2. Terminal connections - continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 20

Terminal symbol	Description
FB	<p>This pin is the voltage feedback input to the internal error amplifier. Connect a resistor from FB to V_{OUT} and from FB to AGND to adjust the output voltage in accordance with equation: $V_{OUT} = V_{REF} \cdot [1 + (R_T/R_B)]$. Where: V_{OUT} = output voltage. V_{REF} = reference voltage (0.6 V normally). R_T = top divider resistor (must be 1 kΩ). R_B = bottom divider resistor. The top divider resistor must be 1 kΩ to mitigate SEE. Connect a 4.7 nF ceramic capacitor across R_T to mitigate SEE and to improve stability margins. If using current share, tie FB of the master to FB of the slave.</p>
ISHA/B/C	<p>If configured as a current share master (ISHSL = DGND), the ISHA/B/C pins are outputs that provides a current equal to 25 times the redundant A/B/C error amplifier output currents plus ISHREFA/B/C (nominally 100 μA each). If configured as a current share slave (ISHSL = DVDD), the ISHA/B/C pins are inputs that become the slave's redundant A/B/C error amp output current. If using current share, tie ISHA/B/C of the master to ISHA/B/C of the slave. If not using current share, tie ISHA/B/C to DVDD. ISHA/B/C is tri-stated prior to a valid POR.</p>
ISHREFA/B/C	<p>If configured as a current share master (ISHSL = DGND), the ISHREFA/B/C pins provide a reference output current equal to 100 μA each. If configured as a current share slave (ISHSL = DVDD), the ISHREFA/B/C pins accept a reference input current. For a current share slave, this input current is used together with the ISHA/B/C current to determine the master's redundant A/B/C error amp output current. If using current share, tie ISHREFA/B/C of the master to ISHREFA/B/C of the slave. If not using current share, tie ISHREFA/B/C to DVDD. The purpose of the reference current is to reduce the impact of external noise coupling onto ISHA/B/C. ISHREFA/B/C are tri-stated prior to a valid POR.</p>
AVDD	<p>This pin is the bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 1 W resistor and a 1 μF ceramic capacitor. Locate both filter components as close as possible to the device. AVDD should be the same voltage as DVDD and PVINx (±200 mV).</p>
AGND	<p>This pin is the analog ground associated with the internal analog control circuitry. Connect this pin directly to the printed circuit board (PCB) ground plane.</p>
DGND	<p>This pin is the digital ground associated with the internal digital control circuitry. Connect this pin directly to the PCB ground plane.</p>
DVDD	<p>This pin is the bias supply input to the internal digital control circuitry. Locally filter this pin to DGND using a 1 W resistor and a 1 μF ceramic capacitor. Locate both filter components as close as possible to the device. DVDD should be the same voltage as AVDD and PVINx (±200mV).</p>

FIGURE 2. Terminal connections - continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 21

Terminal symbol	Description
SS	<p>This pin is the soft-start input. Connect a ceramic capacitor from this pin to DGND to set the soft-start output ramp time in accordance with equation:</p> $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$ <p>Where: t_{SS} = soft-start output ramp time. C_{SS} = soft-start capacitor. V_{REF} = reference voltage (0.6 V normally). I_{SS} = soft-start charging current (23 μA normally). Soft-start time is adjustable from approximately 2 ms to 200 ms. The range of the soft-start capacitor should be 8.2 nF to 8.2 μF, inclusive. If using current share, C_{SS} of the slave should be at least twice the C_{SS} of the master.</p>
PGOOD	<p>This pin is the power-good output. This pin is an open drain logic output that is pulled to DGND when the output voltage is outside a $\pm 11\%$ normal regulation window. This pin can be pulled up to any voltage from 0 V to 5.5 V, independent of the supply voltage. A nominal 1 kW to 10 kW pull-up resistor is recommended. Bypass this pin to DGND with a 10 nF ceramic capacitor to mitigate SEE. If using current share, tie PGOOD of the master to PGOOD of the slave.</p>
ISHCOM	<p>ISHCOM is a bidirectional communication line between a current share master and a current share slave. If using current share, tie ISHCOM of the master to ISHCOM of the slave. The master enables the slave by resistively (~ 8.5 kΩ) pulling ISHCOM high. The slave indicates an over-current fault condition to the master by pulling ISHCOM low. To mitigate SET, connect a 47 pF ceramic capacitor from ISHCOM to the PCB ground plane. If not using current share this pin should be floated or connected to the PCB ground plane. ISHCOM is tri-stated if ISHEN is low.</p>
ISHSL	<p>This pin is a logic input that is used to configure the device as a current share master or slave. Tie this pin to DVDD to configure the device as a current share slave. Tie this pin to the PCB ground plane to configure the device as a current share master, or if the current share feature is not being used.</p>
ISHEN	<p>This pin is an input that enables/disables the current share feature. To enable the current share feature, tie this pin to DVDD. To disable the current share feature, tie this pin to the PCB ground plane.</p>
PORSEL	<p>This pin is the input for selecting the rising and falling POR (power-on-reset) thresholds. For a nominal 5 V supply, connect this pin to DVDD. For a nominal 3.3 V supply, connect this pin to DGND. For nominal supply voltages between 5 V and 3.3 V, connect this pin to DGND.</p>
TDO	<p>This pin is the test data output of the internal BIT circuitry. Connect this pin to the PCB ground plane.</p>
TDI	<p>This pin is the test data input of the internal BIT circuitry. Connect this pin to the PCB ground plane.</p>
TPGM	<p>This pin is a trim input and is used to adjust various internal circuitry. Connect this pin to the PCB ground plane.</p>

FIGURE 2. Terminal connections - continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 22

Terminal symbol	Description
GND	This pin is connected to an internal metal die trace that serves as a sensitive node noise shield. Connect this pin to the PCB ground plane.
SYNC	When SYNC is configured as an output (clock master mode, M/S = DVDD), this pin drives the SYNC input of another same device with a square wave that is inverted (~180° out of phase) from the master clock driving the master PWM circuits. When configured as an input (clock slave mode, M/S = DGND), this pin uses the SYNC output from another exact device or an external clock to drive the clock slave PWM circuitry. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 400 kHz to 1.2 MHz.
PVINx	These pins are the power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3 V to 5.5 V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the device. PVINx should be the same voltage as DVDD and AVDD (± 200 mV).
LXx	These pins are the outputs of the corresponding internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous metal oxide semiconductor field effect transistor (MOSFET) power switches.
PGNDx	These pins are the power grounds associated with the corresponding internal power blocks. These pins also provide the ground path for the metal package lid. Connect these pins directly to the PCB ground plane. These pins should also connect to the negative terminals of the input and output capacitors. Locate the input and output capacitors as close as possible to the device.
M/S	This pin is the clock master/slave input for selecting the direction of the bi-directional SYNC pin. For SYNC = output (master mode), connect this pin to DVDD. For SYNC = input (slave mode), connect this pin to the PCB ground plane.
FSEL	This pin is the oscillator frequency select input. Tie this pin to DVDD to select a 1 MHz nominal oscillator frequency. Tie this pin to the PCB ground plane to select a 500 kHz nominal oscillator frequency.
NC	These are no connect pins that are not connected to anything internally. They should be connected to the PCB ground plane.
SC0/1	<p>These pins are inputs that comprise a 2-bit code to select the slope compensation (SC) current ramp referred to the output as shown below.</p> <p>SC1 = V_{IN}, SC0 = V_{IN}: SC = 13.4 A/μs for FSEL = V_{IN} and SC = 6.6 A/μs for FSEL = GND.</p> <p>SC1 = V_{IN}, SC0 = GND: SC = 6.7 A/μs for FSEL = V_{IN} and SC = 3.3 A/μs for FSEL = GND.</p> <p>SC1 = GND, SC0 = V_{IN}: SC = 3.4 A/μs for FSEL = V_{IN} and SC = 1.6 A/μs for FSEL = GND.</p> <p>SC1 = GND, SC0 = GND: SC = 1.7 A/μs for FSEL = V_{IN} and SC = 0.8 A/μs for FSEL = GND.</p> <p>If using current share, SC0 and SC1 of the slave must match the master SC0 and SC1.</p>

FIGURE 2. Terminal connections - continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 23

Terminal symbol	Description
EN	This pin is the enable input to the device. This is a comparator type input with a rising threshold of 0.6 V and programmable hysteresis. Driving this pin above 0.6 V enables the device. Bypass this pin to the PCB ground plane with a 10 nF ceramic capacitor to mitigate SEE.
OCSSB/A	This pin is a source follower output that is used to set the redundant A/B peak overcurrent limit threshold during soft-start. Connect a resistor from this pin to the PCB ground plane in accordance with the following equation: $ROC_{SSx} (k\Omega) = (60 \times ROC_x) / [(IOC_{SSx} \times ROC_x) - 60]$, where $ROC_x (k\Omega)$ is the resistor value chosen to set the peak overcurrent limit during normal operation and $IOC_{SSx} (A)$, is the desired peak current limit threshold during soft-start.
OCB/A	This pin is an current source output that is used to set the redundant A/B peak overcurrent limit threshold during normal operation. Connect a resistor from this pin to the PCB ground plane in accordance with the following equation: $ROC_x (k\Omega) = 60 / IOC$, where $IOC (A)$ is the desired peak current limit threshold during normal operation.
REF	This pin is the internal reference voltage output. Bypass this pin to the PCB ground plane with a 220 nF ceramic capacitor located as close as possible to the device. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin. If using current share, tie REF of the master to REF of the slave through a 10 Ω resistor.
HEATSINK	The heatsink is connected to device pin 50 (NC) and is electrically isolated. The heatsink should be connected to a thermal chassis of any potential for optimal thermal relief.
PACKAGE LID	For case outlines X and Y the lid is connected to the PGNDx pins.

FIGURE 2. Terminal connections - continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 24

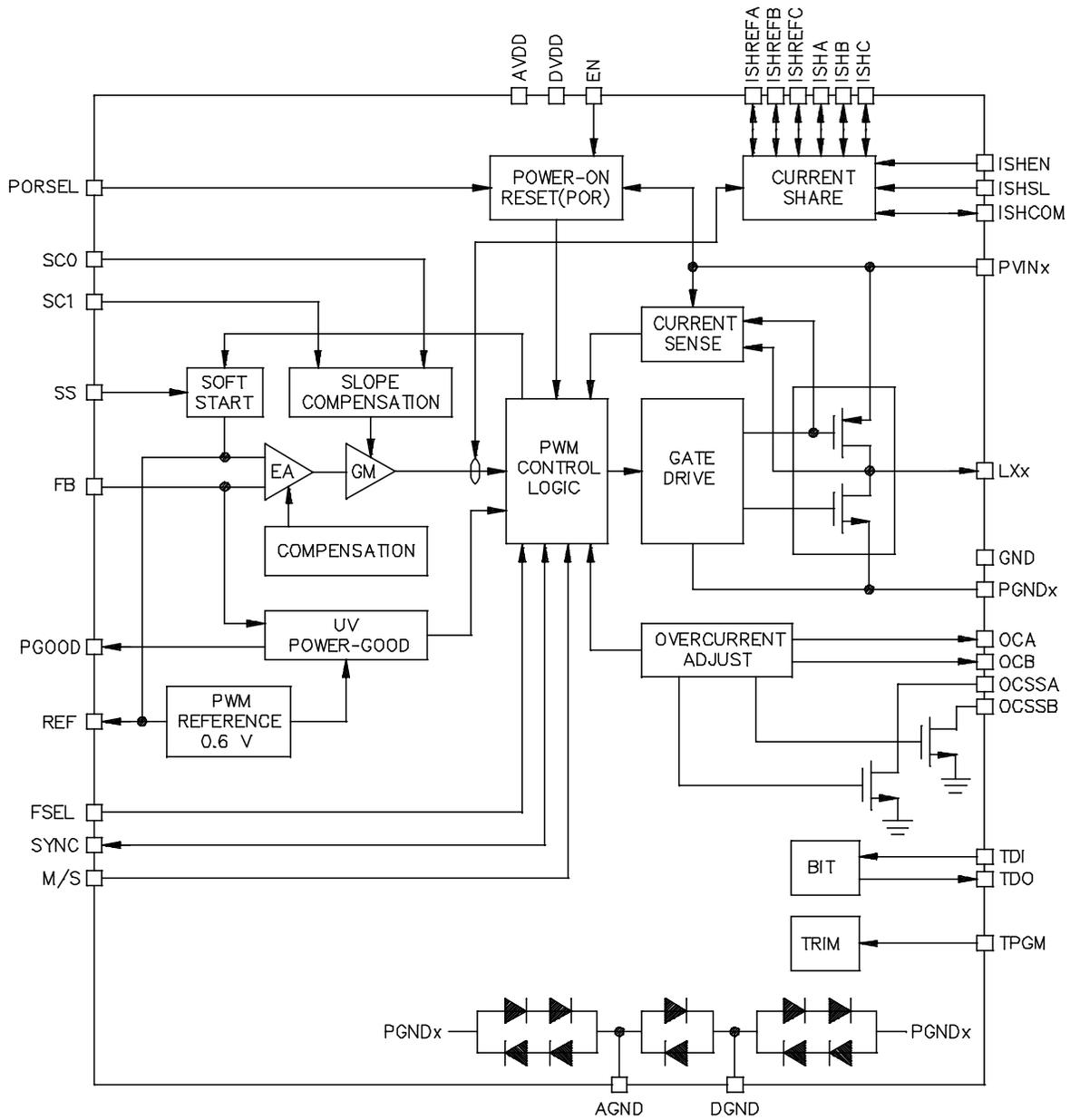


FIGURE 3. Block diagram.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 25

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 26

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4	1,4
Final electrical parameters (see 4.2)	1,2,3,4,5,6 <u>1/</u>	1,2,3, <u>1/ 2/</u> 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3, <u>2/</u> 4,5,6
Group D end-point electrical parameters (see 4.4)	1,4	1,4
Group E end-point electrical parameters (see 4.4)	1,4	1,4

- 1/ For device class Q, PDA applies to subgroup 1.
For device class V, PDA applies to subgroups 1 and Δ.
- 2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Delta limits		Units
		Min	Max	
Standby supply current (3.6 V) (current share disabled)	ISBY1_3.6 V	-1.20	+1.20	mA
Standby supply current (5.5 V) (current share disabled)	ISBY1_5.5 V	-2.40	+2.40	mA
Reference voltage tolerance (3 V)	V _{REF} _3.0 V	-2.00	+2.00	mV
Reference voltage tolerance (5.5 V)	V _{REF} _5.5 V	-2.00	+2.00	mV
Oscillator accuracy (3 V) 1 MHz	OSC_3.0 V	-80	+80	kHz
Oscillator accuracy (5.5 V) 1 MHz	OSC_5.5 V	-80	+80	kHz
Soft start source current (3 V)	ISSSRC_3.0 V	-2.50	+2.50	μA
Soft start source current (5.5 V)	ISSSRC_5.0 V	-2.50	+2.50	μA

1/ Deltas are performed at room temperature.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 27

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C} \pm 10\%$ for SET. The test temperature shall be $+125^{\circ}\text{C} \pm 10\%$ for SEB and SEL.
- f. Bias conditions shall be $V_{IN} = 6.2$ V maximum for the latchup measurements.
- g. For SEL, SEB, SET, and SEFI test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 28

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Occurrence of latchup (SEL).
- d. Occurrence of burnouts (SEB).
- e. Number of transients (SET).
- f. Number of single event functional interrupts (SEFI).

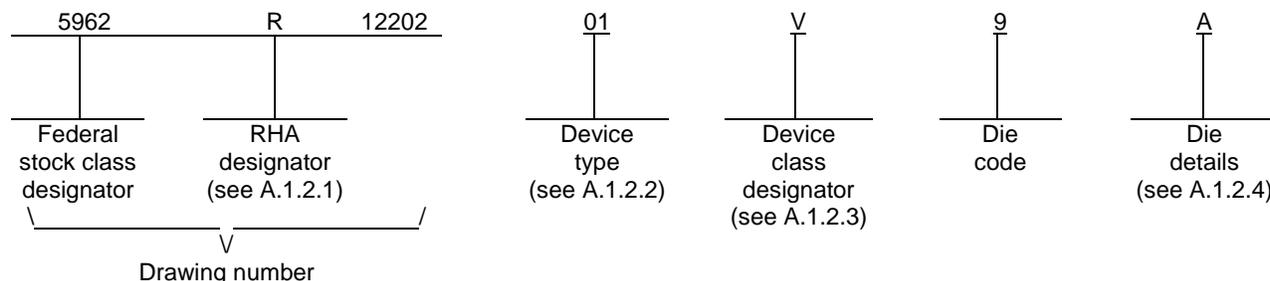
STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 29

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-12202

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	ISL70002SEH	Synchronous buck regulator

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A	REVISION LEVEL A	5962-12202 SHEET 30
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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-12202

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 31

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-12202

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 32

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-12202

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

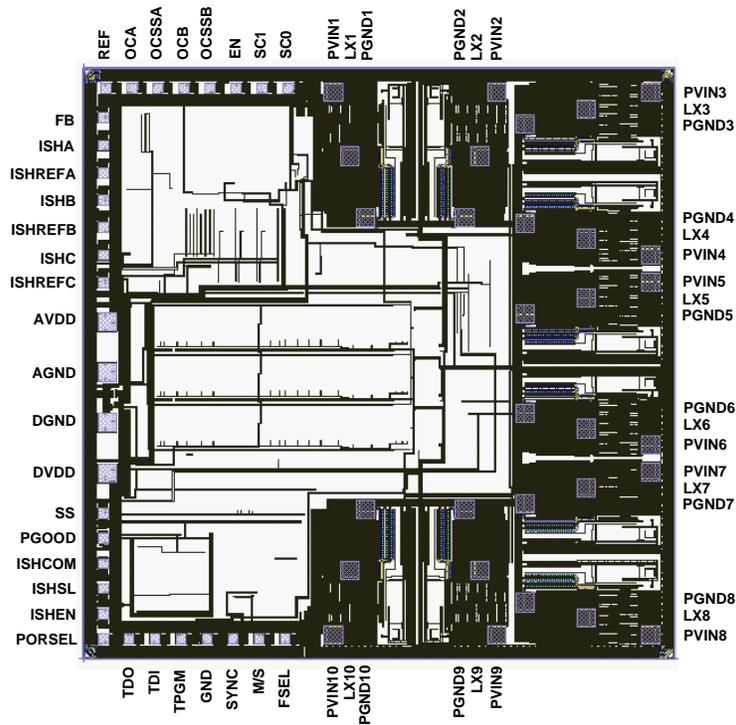
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12202
		REVISION LEVEL A	SHEET 33

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-12202



Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 8300 μm x 8300 μm (327 mils x 327 mils)
Die thickness: 300 μm \pm 25.4 μm (12.0 mils \pm 1 mil)

Interface materials.

Top metallization: AlCu (0.5%)
Thickness: 2.7 μm \pm 0.4 μm
Backside metallization: None

Glassivation.

Type: Silicon oxide and silicon nitride
Thickness: 0.3 μm \pm 0.03 μm and 1.2 μm \pm 0.12 μm

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: PGND
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A	5962-12202
	REVISION LEVEL A	SHEET 34

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-06-13

Approved sources of supply for SMD 5962-12202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R1220201VXC	34371	ISL70002SEHVF
5962R1220201VYC	34371	ISL70002SEHVF
5962R1220201V9A	34371	ISL70002SEHVX

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34371

Vendor name
and address

Intersil Corporation
1001 Murphy Ranch Road
Milpitas, CA 95035-6803

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.