REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

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TITLE
MICROCIRCUIT, LINEAR, RADIATION-TOLERANT 3-A DDR TERMINATION REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. V62/22615

REV

PAGE 1 OF 14

AMSC N/A

5962-V076-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a radiation-tolerant 3-A double data rate (DDR) termination regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/22615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H3302-SEP	Radiation-tolerant 3-A DDR termination regulator

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	JEDEC MO-153	Thermally Enhanced Thin Shrink Small-Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Input voltage:
- VDD, VLDOIN, VTTSNS, VDDQSNS ..... -0.36 V to 3.6 V
- EN ..... -0.3 V to 3.6 V
- PGND to AGND ..... -0.3 V to 0.3 V

Output voltage:
- VTT, VTTREF ..... -0.3 V to 3.6 V
- PGOOD ..... -0.3 V to 3.6 V

Junction temperature (T_J) ..... -55°C to 150°C
Storage temperature (T_{STG}) ..... -55°C to 150°C
Electrostatic discharge (ESD) ratings:
- Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ..... ±4000 V 3/
- Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ..... ±750 V 4/

Thermal characteristics
- Junction to ambient thermal resistance (θ_{JA}) ..... 25.9 °C/W
- Junction to case (top) thermal resistance ($\theta_{JC(TOP)}$) ..... 15.9 °C/W
- Junction to board thermal resistance (θ_{JB}) ..... 7.9 °C/W
- Junction to top characterization parameter (Ψ_{JT}) ..... 0.2 °C/W
- Junction to board characterization parameter (Ψ_{JB}) ..... 7.9 °C/W
- Junction to case (bottom) thermal resistance ($\theta_{JC(BOT)}$) ..... 1.1 °C/W

1.4 Recommended operating conditions. 2/

Input voltage:
- VDD ..... 2.375 V to 3.5 V
- VDDQSNS ..... 1 V to 3.5 V
- VLDOIN ..... 0.9 V to 3.5 V
- EN, VTTSNS, PGOOD ..... -0.1 V to 3.5 V
- PGND ..... -0.1 V to 0.1 V

Output voltage:
- VTT ..... -0.1 V to 3.5 V
- VTTREF ..... -0.1 V to 1.8 V

Input current:
- PGOOD ..... 0 mA to 4 mA

Output current:
- VTT ..... -3 A to 3 A
- VTTREF ..... -0.01 A to 0.01 A

Junction temperature (T_J) ..... -55°C to 125°C

_____

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are referenced to AGND unless otherwise specified.
3/ JEDEC JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	50 krads (Si) 5/
Single event phenomenon (SEP):	
No SEL occurs at effective linear energy transfer (LET) (see 4.3)	≤ 48 MeV/(mg/cm^2) 6/
No SEB observe at effective LET (see 4.3)	≤ 48 MeV/(mg/cm^2) 6/
No SEGR observe at effective LET (see 4.3)	≤ 48 MeV/(mg/cm^2) 6/

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org/.)

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JEP155 – Recommended ESD target levels for HBM/MM qualification.
JEDEC JEP157 – Recommended ESD-CDM target levels.
JEDEC JS-001 – Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Human Body Model (HBM)
JEDEC JS-002 – Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Charged Device Model (CDM)
JEDEC JESD57 – Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Radiation.

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

5/ The manufacturer supplying device type 01 has performed total ionizing dose (TID) in accordance with MIL-STD-883 method 1019 condition A. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 50 krads(Si). For more information on TID test report, please contact device manufacturer.

6/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver (Ag) ion beam was used at an angle of incidence of 0º at flux of 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) and SEB/SEGR was occurred at surface LET of 48 MeV·cm^2/mg under certain test conditions. SEE test shall be perform in accordance with JESD57. For more information on SEE/SEP test please contact device manufacturer.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/		Device type	Limits		Unit
					Min	Max	
SUPPLY CURRENTS							
Quiescent current	I_{VDD}	EN = 3.3 V, no load		01		30	mA
Shutdown current	$I_{VDD(SHDN)}$	EN = 0 V, no load	VDDQSNS = 0 V			3	mA
			VDDQSNS > 0.78 V			6	
Quiescent current of VLDOIN	I_{VLDOIN}	EN = 3.3 V, no load				1200	µA
Shutdown current of VLDOIN	$I_{VLDOIN(SHDN)}$	EN = 0 V, no load				1	µA
VDDQSNS input current	$I_{VDDQSNS}$	EN = 3.3 V				6	µA
VTT OUTPUT							
Output DC voltage, VTT	VTTSNS	I_{VTT} = 5 mA	VDDQSNS = VLDOIN = 2.5 V (DDR1)	01	1.24	1.26	V
			VDDQSNS = VLDOIN = 1.8V (DDR2)		0.89	0.91	
			VDDQSNS = VLDOIN = 1.5 V (DDR3)		0.745	0.759	
			VDDQSNS = VLDOIN = 1.35 V (DDR3L)		0.67	0.684	
			VDDQSNS = VLDOIN = 1.2 V (DDR4)		0.596	0.608	
		I_{VTT} = –5 mA	VDDQSNS = VLDOIN = 2.5 V (DDR1)		1.25	1.27	V
			VDDQSNS = VLDOIN = 1.8V (DDR2)		0.9	0.92	
			VDDQSNS = VLDOIN = 1.5 V (DDR3)		0.752	0.768	
			VDDQSNS = VLDOIN = 1.35 V (DDR3L)		0.675	0.692	
			VDDQSNS = VLDOIN = 1.2 V (DDR4)		0.602	0.618	
		–1 A ≤ I_{VTT} ≤ 1 A	VDDQSNS = VLDOIN = 2.5 V (DDR1)		1.24	1.28	V
			VDDQSNS = VLDOIN = 1.8V (DDR2)		0.885	0.93	
			VDDQSNS = VLDOIN = 1.5 V (DDR3)		0.735	0.78	
			VDDQSNS = VLDOIN = 1.35 V (DDR3L)		0.66	0.72	
			VDDQSNS = VLDOIN = 1.2 V (DDR4)		0.585	0.63	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test conditions 2/		Device type	Limits		Unit
					Min	Max	
VTT OUTPUT – Continued.							
Dropout voltage, V_{DO} = VLDOIN – VTTREF V_{DO} recorded when VTT – VTTREF = 50 mV	V_{DO}	VDDQSNS = 2.5 V (DDR1)	I_{VTT} = 0.5 A	01		60	mV
			I_{VTT} = 1 A			180	
			I_{VTT} = 2 A			465	
		VDDQSNS = 1.8 V (DDR2)	I_{VTT} = 0.5 A			70	
			I_{VTT} = 1 A			200	
			I_{VTT} = 2 A			475	
		VDDQSNS = 1.5 V (DDR3)	I_{VTT} = 0.5 A			65	
			I_{VTT} = 1 A			180	
			I_{VTT} = 2 A			420	
		VDDQSNS = 1.35 V (DDR3L)	I_{VTT} = 0.5 A			60	
			I_{VTT} = 1 A			180	
			I_{VTT} = 2 A			420	
		VDDQSNS = 1.2 V (DDR4)	I_{VTT} = 0.5 A			60	
			I_{VTT} = 1 A			180	
			I_{VTT} = 2 A			420	
VTT Tolerance to VTTREF (VTT – VTTREF)	$VTT_{(TOL)}$	I_{VTT} = -3 A			1	30	mV
		I_{VTT} = 3 A			-30	-1	
VTT sourcing current limit	$I_{LIM\_SRC\_VTT}$	Ramp output 0 A to 10 A, record current when VTT reaches lowest value			5	9	A
VTT sinking current limit	$I_{LIM\_SNK\_VTT}$	Ramp output 0 A to -10 A, record current when VTT reaches highest value			5	10	A
VTT discharge resistance	R_{DSCHRG}	VDDQSNS = 0 V, VTT = 0.3 V, EN = 0 V				25	Ω
POWER GOOD							
VTT PGOOD threshold with respect to VTTREF	$V_{PG(LOW, Falling)}$	PGOOD window lower falling threshold		01	-21%	-18%	
	$V_{PG(LOW, Rising)}$	PGOOD window lower rising threshold			-17%	-13%	
VTT PGOOD threshold with respect to VTTREF	$V_{PG(HI, Falling)}$	PGOOD window high falling threshold			13%	17%	
	$V_{PG(HI, Rising)}$	PGOOD window high rising threshold			18%	21%	
VTT PGOOD hysteresis	$V_{PG(HYST)}$				5% TYP		
PGOOD startup delay	$t_{PG(delay)}$	Startup rising edge, VTTSNS within 20% of VTTREF			4 TYP		ms
PGOOD bad delay	$t_{PG\_BAD(delay)}$	VTTSNS outside of the ±20% PGOOD window			1.95 TYP		µs
Power good output low	$V_{PG(OL)}$	$I_{PGOOD(SINK)}$ = 4 mA				0.4	V
Power good leakage	$I_{PG(LKG)}$	VTTSNS = VTTREF (PGOOD high impedance), PGOOD = VDD + 0.2 V				1	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test conditions 2/		Device type	Limits Min	Limits Max	Unit
VDDQSNS AND VTTREF							
VDDQSNS UVLO turn-on threshold	$VDDQSNS_{UVLO}$	VDDQSNS rising		01		900	mV
VDDQSNS UVLO hysteresis	$VDDQSNS_{UVLO(HYST)}$					150	
VTTREF voltage	VTTREF				VDDQSNS/2 TYP		V
VTTREF voltage tolerance to VDDQSNS		-10 mA ≤ I_{VTTREF} ≤ 10 mA	VDDQSNS = 2.5 V		49%	51%	
			VDDQSNS = 1.8 V		49%	51%	
			VDDQSNS = 1.5 V		49%	51.25%	
			VDDQSNS = 1.35 V		49%	51.5%	
			VDDQSNS = 1.2 V		49%	51.5%	
		-3 mA ≤ I_{VTTREF} ≤ 3 mA	VDDQSNS = 1.5 V		49%	51%	
			VDDQSNS = 1.35 V		49%	51%	
			VDDQSNS = 1.2 V		49%	51%	
VTTREF sourcing current limit	$I_{LIM\_SRC\_VTTREF}$	Sourcing current ramped from 0 to 55 mA. Find when VTTREF drops to half its original value.			35		mA
VTTREF sinking current limit	$I_{LIM\_SNK\_VTTREF}$	Sinking current ramped from 0 to 16.5 mA. Find when VTTREF hits peak value.			12		
VTTREF discharge current	$I_{VTTREF(dis)}$	EN = 0 V, VDDQSNS = 0 V, VTTREF = 0.5 V			1.3 TYP		mA
UVLO AND ENABLE							
VDD UVLO turn-on threshold	VDD_{UVLO}			01		2.3	V
VDD UVLO hysteresis	$VDD_{UVLO(HYST)}$				40 TYP		mV
Enable high-level input voltage (turn-on)	V_{IH_EN}					1.7	V
Enable low-level input voltage (turn-off)	V_{IL_EN}				0.3		V
Enable hysteresis voltage	$V_{EN(HYS)}$				700 TYP		mV
Enable input leakage current	$I_{EN(LKG)}$				-1	1	µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, 2.375 ≤ VDD ≤ 3.5 V, VLDOIN = 1.8 V, VDDQSNS = 1.8 V, EN = VDD, T_A = – 55°C to 125°C; all voltages with respect to AGND.

TABLE IB. SEP test limits. 1/ 2/ 3/

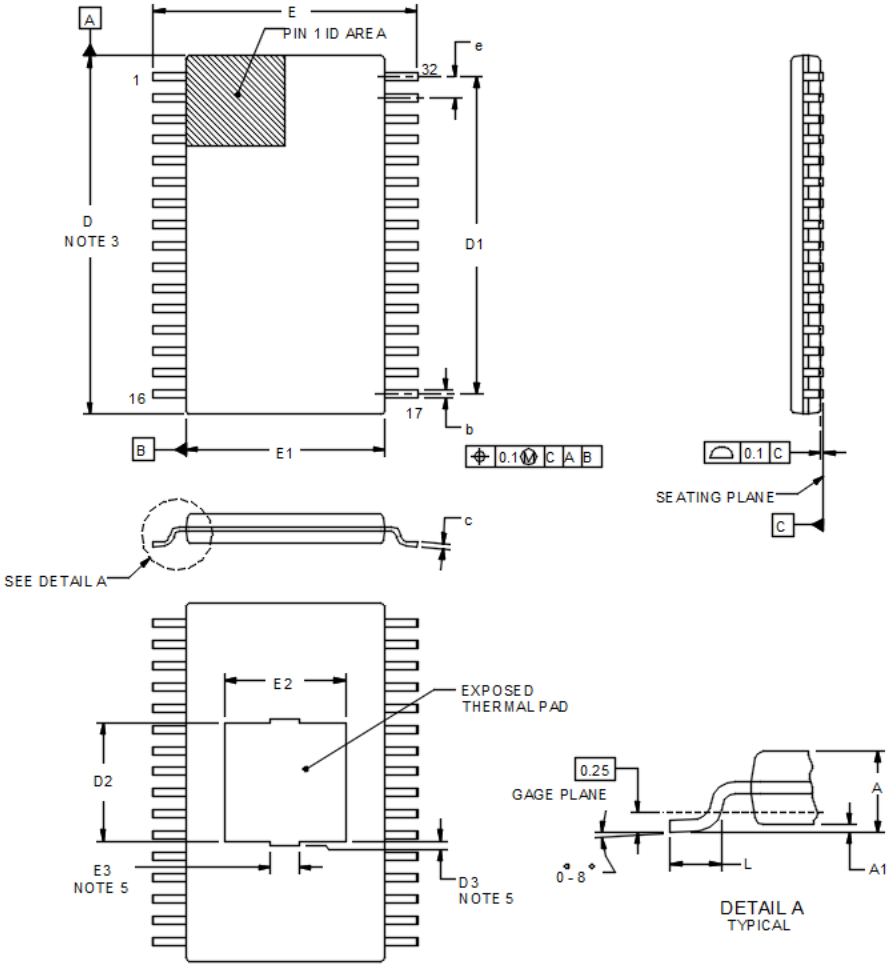
Device type	SEP/SEE	Temperature (T_A)	VIN	Effective Linear energy transfer (LET)
01	No SEL	125 ºC	3.5 V	LET ≤ 48 [MeV/(mg/cm^2)]
	No SEB/SEGR	25 ºC	3.5 V	LET ≤ 48 [MeV/(mg/cm^2)]

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver (Ag) ion beam was used at an angle of incidence of 0º at flux of 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) and SEB/SEGR was occurred at surface LET of 48 MeV·cm^2/mg under certain test conditions. SEE test shall be perform in accordance with JESD57. For more information on SEE/SEP test please contact device manufacturer.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.2	D3	0.15 REF	
A1	0.05	0.15	e	0.65 BSC	
b	0.19	0.30	E	7.9	8.3
c	0.15 TYP		E1	6.0	6.2
D	10.9	11.1	E2	3.29	4.11
D1	9.75 BSC		E3	0.9 REF	
D2	3.16	4.06	L	0.50	0.75

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

FIGURE 1. Case outline.

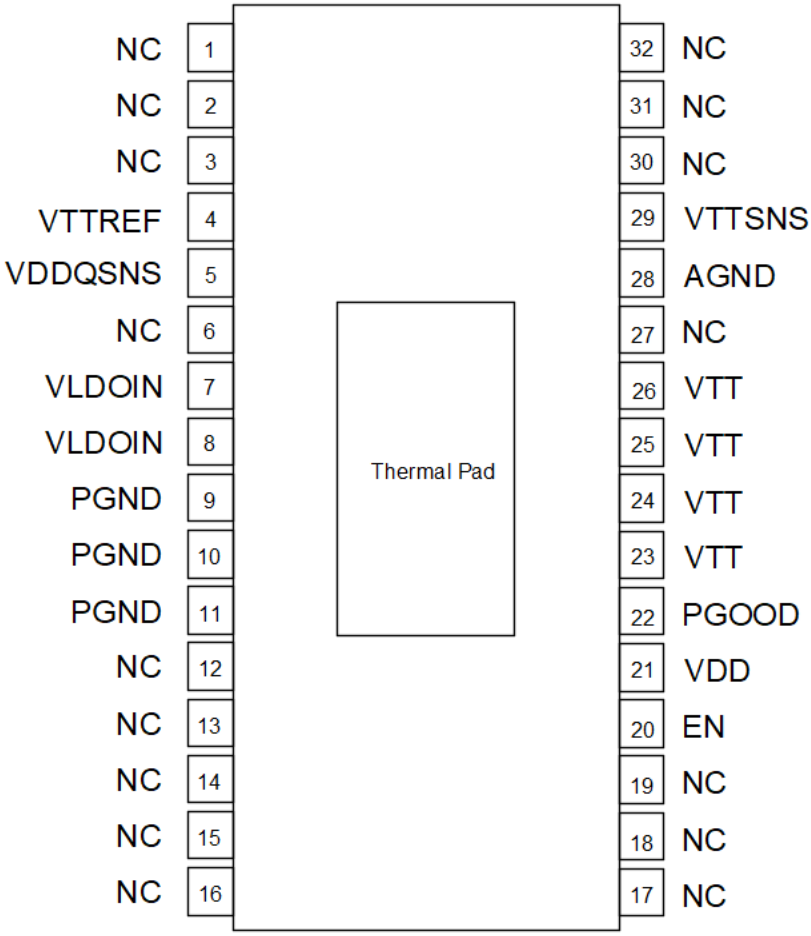


FIGURE 2. Terminal connections.

PIN		I/O	Description
Name	No.	1/	
VTTREF	4	O	Reference output. Connect to GND through 0.1-µF ceramic capacitor.
VDDQSNS	5	I	VDDQ sense input. Reference input for VTTREF. 2/
VLDOIN	7, 8	I	Supply voltage for the LDO. Connect to VDDQ voltage or an alternate voltage source.
PGND	9-11	—	Power ground. Connect to system ground.
EN	20	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
VDD	21	I	2.5- or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1 and 10 µF is required.
PGOOD	22	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
VTT	23-26	O	Power output for VTT LDO.
AGND	28	—	Signal ground. Connect to system ground.
VTTSNS	29	I	Voltage sense for VTT. Place capacitor close to pin. Route sense line to VTT near load.
NC	1-3, 6, 12-19, 27, 30-32	—	No connect. This pin is not internally connected. It is recommended to connect these pins to ground to prevent charge buildup; however, these pins can also be left open or tied to any voltage between ground and VDD.
Thermal Pad			Connect to PGND. This is internally floating.

1/ I = Input, O = Output, — = Other
2/ VDDQSNS shall be connected to the regulated voltage supplying VDDQ. If the VDDQ supply is also used for VLDOIN, an RC filter is recommended to isolate transients from VLDOIN to VDDQ.

FIGURE 2. Terminal connections – Continued.

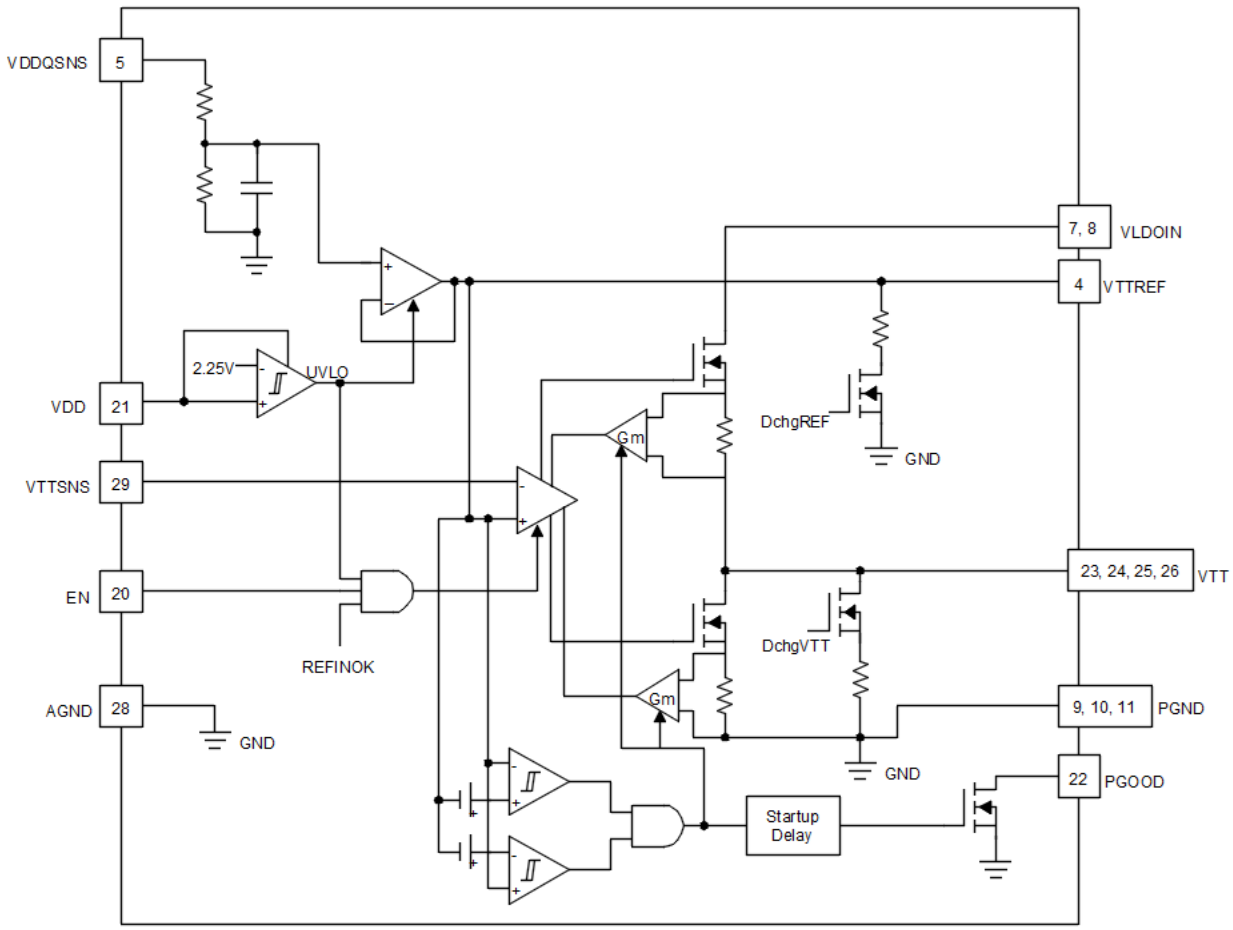


FIGURE 3. Functional Block Diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60˚ to the normal, inclusive (i.e., 0°≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ± 10% for SEL.

f. For SEP test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/22615-01XE	01295	TPS7H3302MDAPTSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243