| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| | | | |

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | 23 | 24 | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |

**PMIC N/A**

Original date of drawing

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**TITLE**

MICROCIRCUIT, DIGITAL, 3-V to 5.5-V RS-485 TRANSCEIVERS WITH 1.8 V VIO CAPABILITY, MONOLITHIC SILICON

| SIZE | CAGE CODE | DWG NO. |
|---|---|---|
| A | 16236 | V62/22613 |

**REV**

**PAGE** 1 OF 24

AMSC N/A

5962-V122-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of an enhanced 3-V to 5.5-V RS-485 transceivers with 1.8 V $V_{IO}$ capability microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/22613 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | THVD2410V-EP | Enhanced 3-V to 5.5-V RS-485 transceivers with 1.8 V VIO capability |
| 02 | THVD2450V-EP | Enhanced 3-V to 5.5-V RS-485 transceivers with 1.8 V VIO capability |
| 03 | THVD2452V-EP | Enhanced 3-V to 5.5-V RS-485 transceivers with 1.8 V VIO capability |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 10 | See figure 1 | Plastic small outline - no lead (VSON) |
| Y | 14 | See figure 1 | Small outline integrated circuit (SOIC) |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/ 2/

Logic supply voltage range ($V_{IO}$) .................... -0.5 V to $V_{CC}$ + 0.2 V
Bus supply voltage range ($V_{CC}$) .................... -0.5 V to 6.5 V
Bus voltage 3/ .................... -70 V to 70 V
Input voltage, range at any logic pin (D, DE, SLR or $\overline{RE}$) .................... -0.3 V to $V_{IO}$ + 0.2 V
Receiver output current range ($I_O$) .................... -24 mA to 24 mA
Storage temperature range ($T_{STG}$) .................... -65°C to 170°C
Power dissipation ($P_D$), Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z), $V_{CC}$ = 5.5 V, $T_A$ = 125°C, square wave at 50% duty cycle:
Unterminated, $R_L$ = 300 Ω, $C_L$ = 50 pF (driver):
THVD2410V-EP, 250 kbps .................... 160 mW
1 Mbps .................... 250 mW
THVD2450V-EP, THVD2452V-EP, 20 Mbps .................... 310 mW
50 Mbps .................... 630 mW
RS-422 load, $R_L$ = 100 Ω, $C_L$ = 50 pF (driver):
THVD2410V-EP, 250 kbps .................... 170 mW
1 Mbps .................... 250 mW
THVD2450V-EP, THVD2452V-EP, 20 Mbps .................... 290 mW
50 Mbps .................... 570 mW
RS-485 load, $R_L$ = 54 Ω, $C_L$ = 50 pF (driver):
THVD2410V-EP, 250 kbps .................... 220 mW
1 Mbps .................... 280 mW
THVD2450V-EP, THVD2452V-EP, 20 Mbps .................... 325 mW
50 Mbps .................... 560 mW
ESD ratings, Electrostatic discharge ($V_{(ESD)}$):
Human body model (HDM), per ANSI/ESDA/JEDEC JS-001: 4/
Bus terminals and GND .................... ±16,000 V
All pins except bus terminals and GND .................... ±4,000 V
Charge device model (CDM), per JEDEC JESD22-C101 .................... ±1,500 V 5/
ESD ratings [IEC]:
Electrostatic discharge ($V_{(ESD)}$), half duplex devices THVD2410V/2450V-EP: 6/
Contact discharge, per IEC 61000-4-2, bus terminals and GND .................... ±15,000 V
Air-gap discharge, per IEC 61000-4-2, bus terminals and GND .................... ±15,000 V
Electrostatic discharge ($V_{(ESD)}$), full duplex devices THVD2452V-EP: 6/
Contact discharge, per IEC 61000-4-2, bus terminals and GND .................... ±8,000 V
Air-gap discharge, per IEC 61000-4-2, bus terminals and GND .................... ±8,000 V
Electrical fast transient ($V_{(EFT)}$), per IEC 61000-4-4, bus terminals .................... ±4,000 V

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1/ Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
2/ All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
3/ Range at any bus pin as differential or common-mode with respect to GND.
4/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
5/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
6/ For optimized IEC ESD performance, it is recommended to have series resistor (≥ 50 Ω) on all logic inputs to minimize transient currents going into or out of the logic pins.

1.4 Recommended operating conditions. 1/

Supply voltage range ($V_{CC}$) .................... 3.0 V to 5.5 V
I/O supply voltage range ($V_{IO}$) .................... 1.65 V to $V_{CC}$ V
Input voltage at any bus terminal range (separately or common mode) ($V_I$) 2/ .................... -12 V to 12 V
High-level input voltage range (driver, driver enable, receiver enable,
and slew rate select inputs) ($V_{IH}$) .................... 0.7*$V_{IO}$ V to $V_{IO}$ V
Low-level input voltage range (driver, driver enable, receiver enable,
and slew rate select inputs) ($V_{IL}$) .................... 0 V to 0.3*$V_{IO}$ V
Differential input voltage bus pins range ($V_{ID}$) .................... -25 V to 25 V
Output current range, driver ($I_O$) .................... -60 mA to 60 mA
Output current range, receiver ($I_{OR}$):
$V_{IO}$ = 1.8 V or 2.5 V .................... -4 mA to 4 mA
$V_{IO}$ = 3.3 V or 5 V .................... -8 mA to 8 mA
Minimum differential load resistance ($R_L$) .................... 54 Ω
Maximum signaling rate ($1/t_{UI}$):
THVD2410V with SLR = $V_{IO}$ .................... 250 kbps
SLR = GND or floating .................... 1 Mbps
THVD2450V, THVD2452V with SLR = $V_{IO}$ .................... 20 Mbps
SLR = GND or floating .................... 50 Mbps
Operating ambient temperature range ($T_A$) .................... -55°C to 125°C
Junction temperature range ($T_J$) .................... -55°C to 150°C

Thermal characteristics: 3/

| Thermal metric | Symbol | Case X | Case Y | Unit |
|---|---|---|---|---|
| Thermal resistance, junction-to-ambient 4/ | $R_{\theta JA}$ | 46.7 | 87.5 | °C/W |
| Thermal resistance, junction-to-case (top) 5/ | $R_{\theta JC(TOP)}$ | 47.7 | 41.8 | °C/W |
| Thermal resistance, junction-to-case (bottom) 6/ | $R_{\theta JC(BOTTOM)}$ | 4.6 | N/A | °C/W |
| Thermal resistance, junction-to-board 7/ | $R_{\theta JB}$ | 19.1 | 43.7 | °C/W |
| Characterization parameter, junction-to-top 8/ | $\psi JT$ | 0.7 | 8.1 | °C/W |
| Characterization parameter, junction-to-board 9/ | $\psi JB$ | 19.1 | 43.3 | °C/W |

1/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
2/ The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used.
3/ For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
4/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
5/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
6/ The thermal resistance, junction-to-case (bottom) is obtained by simulations of this device as configured per MIL-STD-883 method 1012.1.
7/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.
8/ Characterization parameter, junction-to-top ($\psi JT$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
9/ Characterization parameter, junction-to-board ($\psi JB$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

## 2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

| | | |
|---|---|---|
| JEDEC PUB 95 | – | Registered and Standard Outlines for Semiconductor Devices |
| JEDEC JEP 155 | – | Recommended ESD Target Levels for HBM/MM Qualification |
| JEDEC JEP 157 | – | Recommended ESD-CDM Target Levels |
| JEDEC JS-001 | – | Human Body Model Testing of Integrated Circuits |
| JEDEC JS-002 | – | Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM) |
| JESD22-C101 | – | Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components |

(Copies of these documents are available online at https://www.jedec.org.)

International Electrotechnical Commission

| | | |
|---|---|---|
| IEC 61000-4-2 | – | Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test |
| IEC 61000-4-4 | – | Electromagnetic Compatibility (EMC) - Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test |

(Copies of these documents are available from https://www.iec.ch.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagrams. The functional block diagrams shall be as shown in figure 3.

3.5.4 Functional modes. The functional modes shall be as shown in Figure 4.

3.5.5 Measurement of driver differential output voltage with common-mode load. The measurement of driver differential output voltage with common-mode load shall be as shown in figure 5.

3.5.6 Measurement of driver differential and common-mode output with RS-485 load. The measurement of driver differential and common-mode output with RS-485 load shall be as shown in figure 6.

3.5.7 Measurement of driver differential output rise and fall times and propagation delays. The measurement of driver differential output rise and fall times and propagation delays shall be as shown in figure 7.

3.5.8 Measurement of driver enable and disable times with active high output and pull-down load. The measurement of driver enable and disable times with active high output and pull-down load shall be as shown in figure 8.

3.5.9 Measurement of driver enable and disable times with active low output and pull-up load. The measurement of driver enable and disable times with active low output and pull-up load shall be as shown in figure 9.

3.5.10 Measurement of receiver output rise and fall times and propagation delays. The measurement of receiver output rise and fall times and propagation delays shall be as shown in figure 10.

3.5.11 Measurement of receiver enable/disable times with driver enabled. The measurement of receiver enable/disable times with driver enabled shall be as shown in figure 11.

3.5.12 Measurement of receiver enable times with driver disabled. The measurement of receiver enable times with driver disabled shall be as shown in figure 12.

3.5.13 Measurement of fail-safe delay. The measurement of fail-safe delay shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions 2/ 3/ | Device type | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| **Driver** | | | | | | |
| Driver differential output voltage magnitude | $\|V_{OD}\|$ | $R_L$ = 60 Ω, -25 V ≤ $V_{test}$ ≤ 25 V (See Figure 5) | All | 1.5 | | V |
| | | $R_L$ = 60 Ω, -25 V ≤ $V_{test}$ ≤ 25 V, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V (See Figure 5) | | 2.1 | | |
| | | $R_L$ = 100 Ω (See Figure 6) | | 2 | | |
| | | $R_L$ = 54 Ω (See Figure 6) | | 1.5 | | |
| Change in differential output voltage | $\Delta\|V_{OD}\|$ | $R_L$ = 54 Ω or 100 Ω (See Figure 6) | All | -50 | 50 | mV |
| Common-mode output voltage | $V_{OC}$ | $R_L$ = 54 Ω or 100 Ω (See Figure 6) | All | 1 | 3 | V |
| Change in steady-state common-mode output voltage | $\Delta V_{OC(SS)}$ | $R_L$ = 54 Ω or 100 Ω (See Figure 6) | All | -50 | 50 | mV |
| Short-circuit output current | $I_{OS}$ | DE = $V_{IO}$, -70 V ≤ ($V_A$ or $V_B$) ≤ 70 V, or A shorted to B (A, B are driver terminals for half duplex, Y/Z are for full duplex) | All | -250 | 250 | mA |
| **Receiver** | | | | | | |
| Bus input current | $I_I$ | DE = 0 V, $V_{CC}$ and $V_{IO}$ = 0 V or 5.5 V, $V_I$ = 12 V | All | | 125 | µA |
| | | $V_I$ = 25 V | | | 250 | |
| | | $V_I$ = -7 V | | -100 | | |
| | | $V_I$ = -25 V | | -350 | | |
| Positive-going input threshold voltage | $V_{TH+}$ 4/ | Over common-mode range of ±12 V | All | 40 | 200 | mV |
| Negative-going input threshold voltage | $V_{TH-}$ 4/ | | | -200 | -40 | |
| Input hysteresis | $V_{HYS}$ | | | 250 typical | | |
| Input fail-safe threshold | $V_{TH\_FSH}$ | | | -40 | 40 | |
| Input differential capacitance | $C_{A,B}$ | Measured between A and B, f = 1 MHz | All | 50 typical | | pF |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -8 mA, $V_{IO}$ = 3 to 3.6 V or 4.5 V to 5.5 V | All | $V_{IO}$ – 0.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{IO}$ = 3 to 3.6 V or 4.5 V to 5.5 V | All | | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -4 mA, $V_{IO}$ = 1.65 to 1.95 V or 2.25 V to 2.75 V | All | $V_{IO}$ – 0.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4 mA, $V_{IO}$ = 1.65 to 1.95 V or 2.25 V to 2.75 V | All | | 0.4 | V |
| Output high-impedance current, R pin | $I_{OZ}$ | $V_O$ = 0 V or $V_{IO}$, $\overline{RE}$ = $V_{IO}$ | All | -1 | 1 | µA |
| **Logic** | | | | | | |
| Input current (DE, SLR) | $I_{IN}$ | 1.65 V ≤ $V_{IO}$ ≤ 5.5 V, 0 V ≤ $V_{IN}$ ≤ $V_{IO}$ | All | | 5 | µA |
| Input current (D, $\overline{RE}$) | $I_{IN}$ | 1.65 V ≤ $V_{IO}$ ≤ 5.5 V, 0 V ≤ $V_{IN}$ ≤ $V_{IO}$ | All | -5 | | µA |
| **Thermal protection** | | | | | | |
| Thermal shutdown threshold | $T_{SHDN}$ | Temperature rising | All | 150 | | °C |
| Thermal shutdown hysteresis | $T_{HYS}$ | | All | 10 typical | | °C |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ 3/ | | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **Supply** | | | | | | | |
| Rising under-voltage threshold on $V_{CC}$ | $UV_{VCC(rising)}$ | | | All | | 2.6 | V |
| Falling under-voltage threshold on $V_{CC}$ | $UV_{VCC(falling)}$ | | | All | 1.95 | | V |
| Hysteresis on under-voltage of $V_{CC}$ | $UV_{VCC(hys)}$ | | | All | 150 typical | | mV |
| Rising under-voltage threshold on $V_{IO}$ | $UV_{VIO(rising)}$ | | | All | | 1.6 | V |
| Falling under-voltage threshold on $V_{IO}$ | $UV_{VIO(falling)}$ | | | All | 1.2 | | V |
| Hysteresis on under-voltage of $V_{IO}$ | $UV_{VIO(hys)}$ | | | All | 30 typical | | mV |
| Supply current (quiescent), $V_{CC}$ = 4.5 V to 5.5 V | $I_{CC}$ | Driver and receiver enabled | $\overline{RE}$ = 0 V, DE = $V_{IO}$, No load | All | | 5.3 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE}$ = $V_{IO}$, DE = $V_{IO}$, No load | All | | 4.2 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE}$ = 0 V, DE = 0 V, no load | All | | 2.4 | mA |
| | | Driver and receiver disabled | $\overline{RE}$ = $V_{IO}$, DE = 0 V, D = open, no load | All | | 1.2 | µA |
| Supply current (quiescent), $V_{CC}$ = 3 V to 3.6 V | $I_{CC}$ | Driver and receiver enabled | $\overline{RE}$ = 0 V, DE = $V_{IO}$, no load | All | | 4.1 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE}$ = $V_{IO}$, DE = $V_{IO}$, no load | All | | 3 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE}$ = 0 V, DE = 0 V, no load | All | | 2.2 | mA |
| | | Driver and receiver disabled | $\overline{RE}$ = $V_{IO}$, DE = 0 V, D = open, no load | All | | 1 | µA |
| Logic supply current (quiescent), VIO = 3 to 3.6 V | $I_{IO}$ | Driver disabled, receiver enabled, SLR = GND | DE = 0 V, $\overline{RE}$ = 0 V, no load | All | | 8.4 | µA |
| | | Driver disabled, receiver enabled, SLR = $V_{IO}$ | DE = 0 V, $\overline{RE}$ = 0 V, no load | All | | 8.4 | µA |
| | | Driver disabled, receiver disabled, SLR = GND | DE = 0 V, $\overline{RE}$ = $V_{IO}$ V, no load | All | | 1 | µA |
| | | Driver disabled, receiver disabled, SLR = $V_{IO}$ | DE = 0 V, $\overline{RE}$ = $V_{IO}$ V, no load | All | | 4 | µA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ 3/ | | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **Switching Characteristics: 250 kbps (THVD2410V-EP with SLR = $V_{IO}$)**<br>**Driver** | | | | | | | |
| Differential output rise/fall time | $t_r$, $t_f$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3V | RL = 54 Ω,<br>CL = 50 pF<br>See Figure 7 | All | 450 | 1200 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5V | | | 500 | 1200 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3V | | | | 720 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5V | | | | 770 | ns |
| Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | $t_{SK(P)}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3V | | | | 70 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5V | | | | 70 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | $\overline{RE}$ = X | See Figure 8 and Figure 9 | All | | 75 | ns |
| Enable time | $t_{PZH}$, $t_{PZL}$ | $\overline{RE}$ = 0 V | | All | | 280 | ns |
| | | $\overline{RE}$ = $V_{IO}$ | | | | 4.5 | µs |
| Time to shutdown | $t_{SHDN}$ | $\overline{RE}$ = $V_{IO}$ | | All | 50 | 500 | ns |
| **Receiver** | | | | | | | |
| Output rise/fall time | $t_r$, $t_f$ | CL = 15 pF | See Figure 10 | All | | 20 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | | | All | | 1270 | ns |
| Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | $t_{SK(P)}$ | | | All | | 45 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | DE = X | | All | | 40 | ns |
| Enable time | $t_{PZH(1)}$ | $V_{IO}$ = 3 to 3.6 V, DE = $V_{IO}$ | See Figure 11 | All | | 120 | ns |
| | | $V_{IO}$ = 1.65 to 1.95 V, DE = $V_{IO}$ | | | | 130 | ns |
| | $t_{PZL(1)}$ | $V_{IO}$ = 3 to 3.6 V, DE = $V_{IO}$ | | | | 1320 | ns |
| | | $V_{IO}$ = 1.65 to 1.95 V, DE = $V_{IO}$ | | | | 1320 | ns |
| | $t_{PZH(2)}$, $t_{PZL(2)}$ | DE = 0 V | See Figure 12 | All | | 5.4 | µs |
| Delay to enter fail-safe operation | $t_{D(OFS)}$ | $C_L$ = 15 pF | See Figure 13 | All | 7 | 18 | µs |
| Delay to exit fail-safe operation | $t_{D(FSO)}$ | | | | 540 | 1260 | ns |
| Time to shutdown | $t_{SHDN}$ | DE = 0 V | See Figure 12 | All | 50 | 500 | ns |
| **Switching Characteristics: 1 Mbps (THVD2410V-EP with SLR = 0 or floating)**<br>**Driver** | | | | | | | |
| Differential output rise/fall time | $t_r$, $t_f$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | $R_L$ = 54 Ω,<br>$C_L$ = 50 pF<br>See Figure 7 | All | 125 | 300 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 130 | 300 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | | 240 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | | 280 | ns |
| Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | $t_{SK(P)}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | | 20 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | | 15 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | $\overline{RE}$ = X | See Figure 8 and Figure 9 | All | | 95 | ns |
| Enable time | $t_{PZH}$, $t_{PZL}$ | $\overline{RE}$ = 0 V | | All | | 275 | ns |
| | | $\overline{RE}$ = $V_{IO}$ | | | | 4.6 | µs |
| Time to shutdown | $t_{SHDN}$ | $\overline{RE}$ = $V_{IO}$ | | All | 50 | 500 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ 3/ | | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **Switching Characteristics: 1 Mbps (THVD2410V-EP with SLR = 0 or floating)<br>Receiver** | | | | | | | |
| Output rise/fall time | $t_r$, $t_f$ | CL = 15 pF | See Figure 10 | All | | 15 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | | | All | | 85 | ns |
| Pulse skew, $\|t_{PHL} - t_{PLH}\|$ | $t_{SK(P)}$ | | | All | | 12.5 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | DE = X | | All | | 40 | ns |
| Enable time | $t_{PZH(1)}$, $t_{PZL(1)}$ | $V_{IO}$ = 3 to 3.6 V, DE = $V_{IO}$ | See Figure 11 | All | | 120 | ns |
| | | $V_{IO}$ = 1.65 to 1.95 V, DE = $V_{IO}$ | | | | 130 | ns |
| | $t_{PZH(2)}$, $t_{PZL(2)}$ | DE = 0 V | See Figure 12 | All | | 4.5 | µs |
| Delay to enter fail-safe operation | $t_{D(OFS)}$ | $C_L$ = 15 pF | See Figure 13 | All | 7 | 18 | µs |
| Delay to exit fail-safe operation | $t_{D(FSO)}$ | | | | 27 | 60 | ns |
| Time to shutdown | $t_{SHDN}$ | DE = 0 V | See Figure 12 | All | 50 | 500 | ns |
| **Switching Characteristics: 20 Mbps (THVD2450V-EP, THVD2452V-EP with SLR = $V_{IO}$)<br>Driver** | | | | | | | |
| Differential output rise/fall time | $t_r$, $t_f$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | $R_L$ = 54 Ω, $C_L$ = 50 pF See Figure 7 | All | 4 | 15 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 4 | 15 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | 6 | 30 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 4 | 26 | ns |
| Pulse skew, $\|t_{PHL} - t_{PLH}\|$ | $t_{SK(P)}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | | 3 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | | 3 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | $\overline{RE}$ = X | See Figure 8 and Figure 9 | | | 35 | ns |
| Enable time | $t_{PZH}$, $t_{PZL}$ | $\overline{RE}$ = 0 V | | | | 39 | ns |
| | | $\overline{RE}$ = $V_{IO}$ | | | | 4.5 | µs |
| Time to shutdown | $t_{SHDN}$ | $\overline{RE}$ = $V_{IO}$ | | | 50 | 500 | ns |
| **Receiver** | | | | | | | |
| Output rise/fall time | $t_r$, $t_f$ | $C_L$ = 15 pF | See Figure 10 | All | | 6 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $V_{IO}$ = 3 V to 3.6 V | | All | 25 | 58 | ns |
| | | $V_{IO}$ = 1.65 V to 1.95 V | | | 25 | 60 | ns |
| Pulse skew, $\|t_{PHL} - t_{PLH}\|$ | $t_{SK(P)}$ | $C_L$ = 15 pF | | All | | 5 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | DE = X | | All | | 25 | ns |
| Enable time | $t_{PZH(1)}$, $t_{PZL(1)}$ | DE = $V_{IO}$ | See Figure 11 | All | | 82 | ns |
| | $t_{PZH(2)}$, $t_{PZL(2)}$ | DE = 0 V | See Figure 12 | All | | 5 | µs |
| Delay to enter fail-safe operation | $t_{D(OFS)}$ | $C_L$ = 15 pF | See Figure 13 | All | 7 | 18 | µs |
| Delay to exit fail-safe operation | $t_{D(FSO)}$ | | | | 19 | 50 | ns |
| Time to shutdown | $t_{SHDN}$ | DE = 0 V | See Figure 12 | All | 50 | 500 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ 3/ | | Device type | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| **Switching Characteristics: 50 Mbps (THVD2450V-EP, THVD2452V-EP with SLR = 0 or floating)** | | | | | | | |
| **Driver** | | | | | | | |
| Differential output rise/fall time | $t_r$, $t_f$ | $V_{IO}$ = 3 to 3.6 V, $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | $R_L$ = 54 Ω, $C_L$ = 50 pF See Figure 7 | All | 1 | 7 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 1 | 6 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $V_{IO}$ = 3 to 3.6 V, $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | 5 | 19 | ns |
| | | $V_{IO}$ = 1.65 to 1.95 V, $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | | 7 | 22 | ns |
| | | $V_{IO}$ = 3 to 3.6 V, $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 4 | 15 | |
| | | $V_{IO}$ = 1.65 to 1.95 V, $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | 6 | 19 | |
| Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$ | $t_{SK(P)}$ | $V_{CC}$ = 3 to 3.6 V, typical at 3.3 V | | All | | 3 | ns |
| | | $V_{CC}$ = 4.5 to 5.5 V, typical at 5 V | | | | 3 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | $\overline{RE}$ = X | See Figure 8 and Figure 9 | All | | 30 | ns |
| Enable time | $t_{PZH}$, $t_{PZL}$ | $\overline{RE}$ = 0 V, $V_{IO}$ = 1.65 to 1.95 V, 2.25 to 2.75 V | | All | | 35 | ns |
| | | $\overline{RE}$ = 0 V, $V_{IO}$ = 3 V to $V_{CC}$ V | | | | 32 | |
| | | $\overline{RE}$ = $V_{IO}$ | | | | 4.5 | µs |
| Time to shutdown | $t_{SHDN}$ | $\overline{RE}$ = $V_{IO}$ | | All | 50 | 500 | ns |
| **Receiver** | | | | | | | |
| Output rise/fall time | $t_r$, $t_f$ | $C_L$ = 15 pF | See Figure 10 | All | | 6 | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 15 pF, $V_{IO}$ = 3 V to 3.6 V | | All | 25 | 58 | ns |
| | | $C_L$ = 15 pF, $V_{IO}$ = 1.65 V to 1.95 V | | | 25 | 60 | ns |
| Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$ | $t_{SK(P)}$ | $C_L$ = 15 pF | | All | | 5 | ns |
| Disable time | $t_{PHZ}$, $t_{PLZ}$ | DE = X | | All | | 25 | ns |
| Enable time | $t_{PZH(1)}$, $t_{PZL(1)}$ | DE = $V_{IO}$ | $V_{IO}$ = 1.65 V to 1.95 V, See Figure 11 | All | | 82 | ns |
| | | | $V_{IO}$ = 3 V to 3.6 V, See Figure 11 | | | 75 | ns |
| | $t_{PZH(2)}$, $t_{PZL(2)}$ | DE = 0 V | See Figure 12 | All | | 5 | µs |
| Delay to enter fail-safe operation | $t_{D(OFS)}$ | $C_L$ = 15 pF | See Figure 13 | All | 7 | 18 | µs |
| Delay to exit fail-safe operation | $t_{D(FSO)}$ | | | | 19 | 50 | ns |
| Time to shutdown | $t_{SHDN}$ | DE = 0 V | See Figure 12 | All | 50 | 500 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

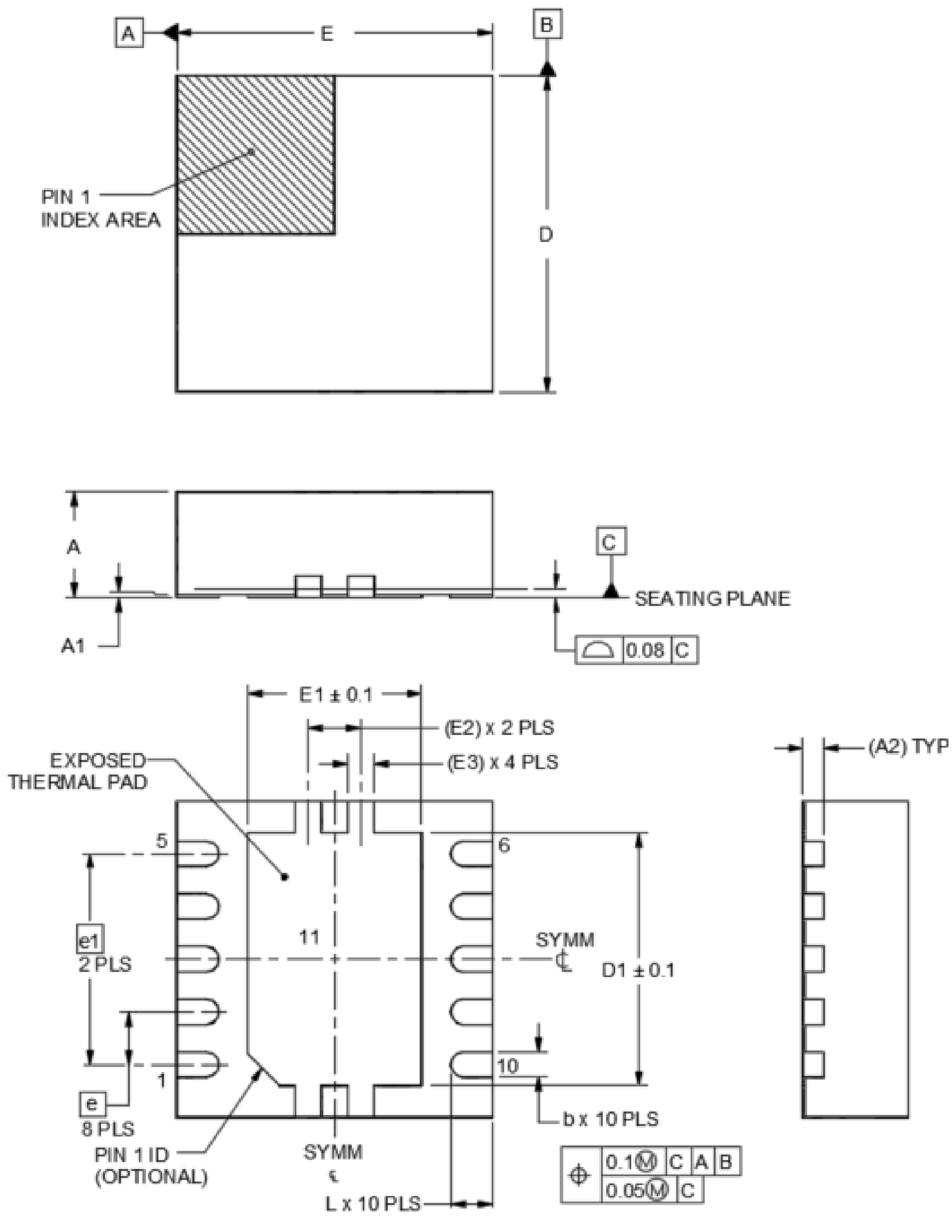
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V, $V_{IO}$ = 3.3 V, unless otherwise noted.

3/ A, B are driver output and receiver input terminals for half duplex devices; A/B are receiver input, Y/Z are driver output terminals for full duplex devices.

4/ Under any specific conditions, $V_{TH+}$ is assured to be at least $V_{HYS}$ higher than $V_{TH-}$.

Case X




NOTES:
1. All linear dimensions are millimeter. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

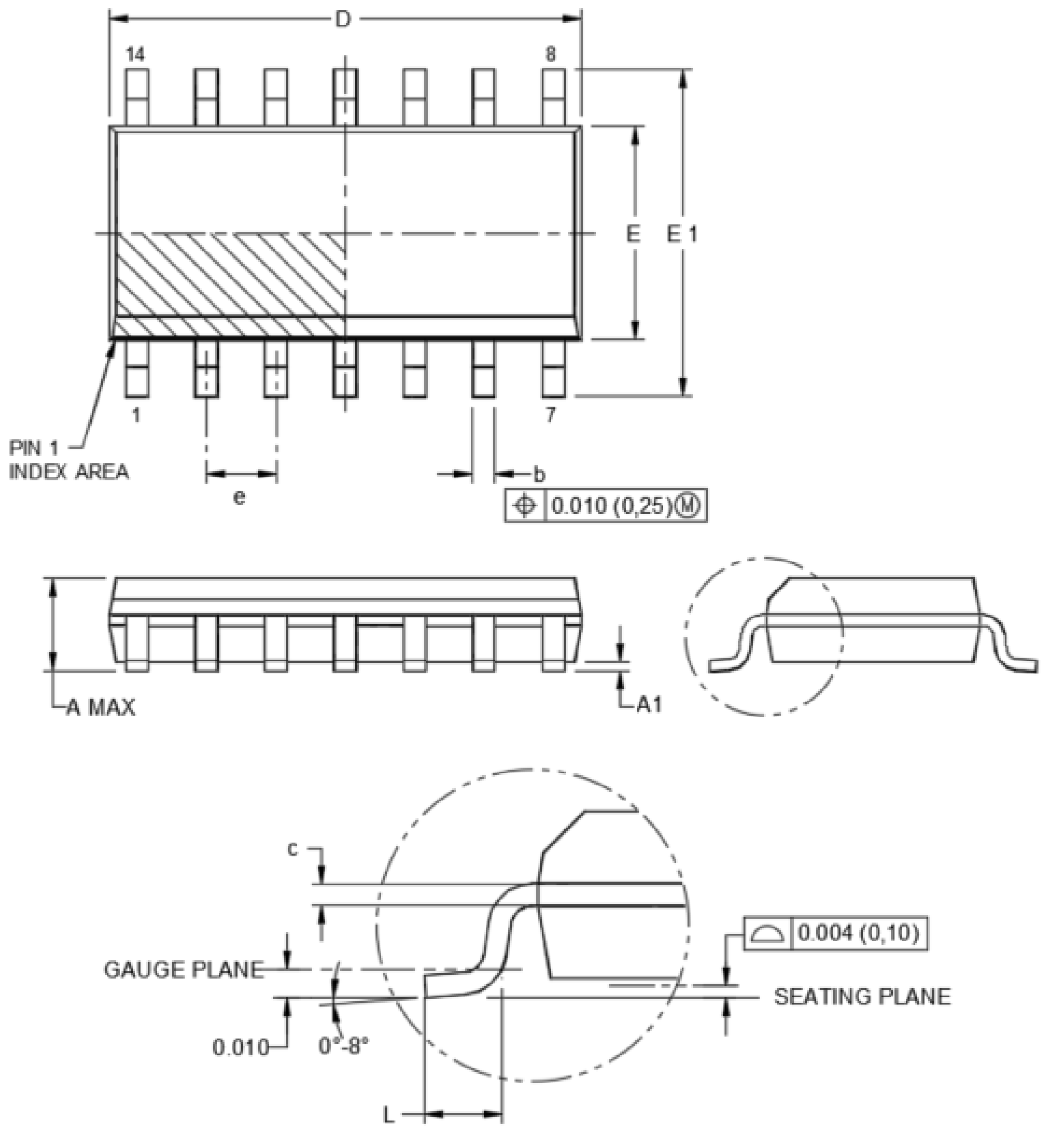
FIGURE 1. Case outline.

Case X - continued

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Millimeters | | Inches | |
| | Minimum | Maximum | Minimum | Maximum |
| A | 0.80 | 1.00 | 0.031 | 0.039 |
| A1 | 0.00 | 0.05 | 0.00 | 0.002 |
| A2 | 0.20 TYP | | 0.008 TYP | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D/E | 2.90 | 3.10 | 0.114 | 0.122 |
| D1 | 2.30 | 2.50 | 0.091 | 0.098 |
| E1 | 1.55 | 1.75 | 0.061 | 0.069 |
| E2 | 0.50 REF | | 0.020 REF | |
| E3 | 0.25 REF | | 0.010 REF | |
| e | 0.50 BSC | | 0.020 BSC | |
| e1 | 2.00 BSC | | 0.079 BSC | |
| L | 0.30 | 0.50 | 0.012 | 0.020 |

FIGURE 1. Case outline – Continued.

Case Y




NOTES:

1. All linear dimensions are in inches.
2. D dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inches (0.15 mm) each side.
3. E dimension does not include interlead flash. Interlead flash shall not exceed 0.017 inches (0.43 mm) per side.
4. Reference JEDEC registration MS-012, variation AB.

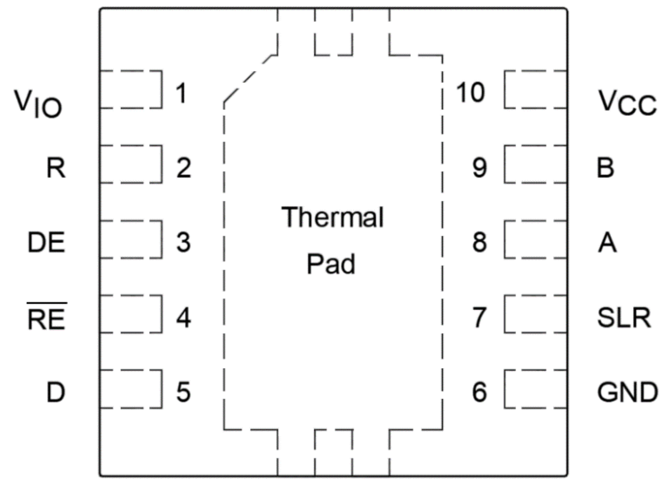
FIGURE 1. Case outline – Continued.

Case Y – continued

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Minimum | Maximum | Minimum | Maximum |
| A | | 0.069 | | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| b | 0.012 | 0.020 | 0.31 | 0.51 |
| c | 0.005 | 0.010 | 0.13 | 0.25 |
| D | 0.337 | 0.344 | 8.55 | 8.75 |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| E1 | 0.228 | 0.244 | 5.80 | 6.20 |
| e | 0.050 BSC | | 1.27BSC | |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

FIGURE 1. Case outline - Continued.

Case X




Case Y

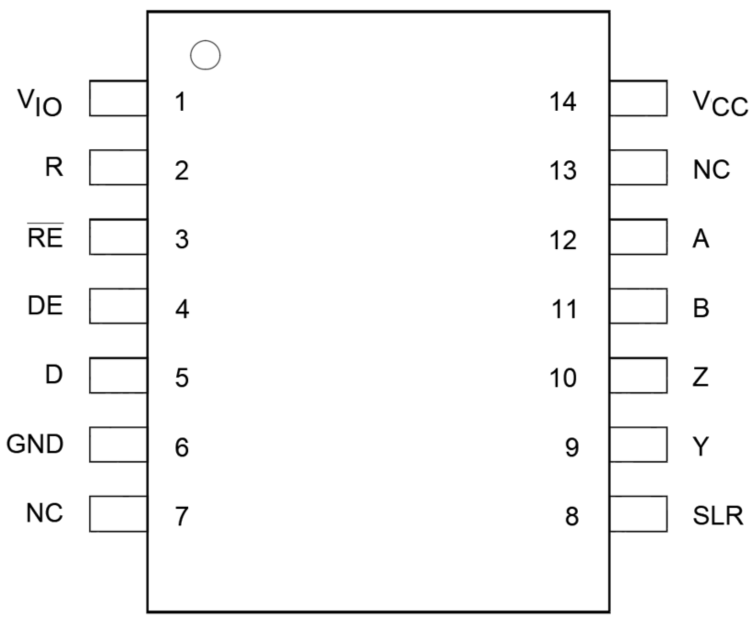
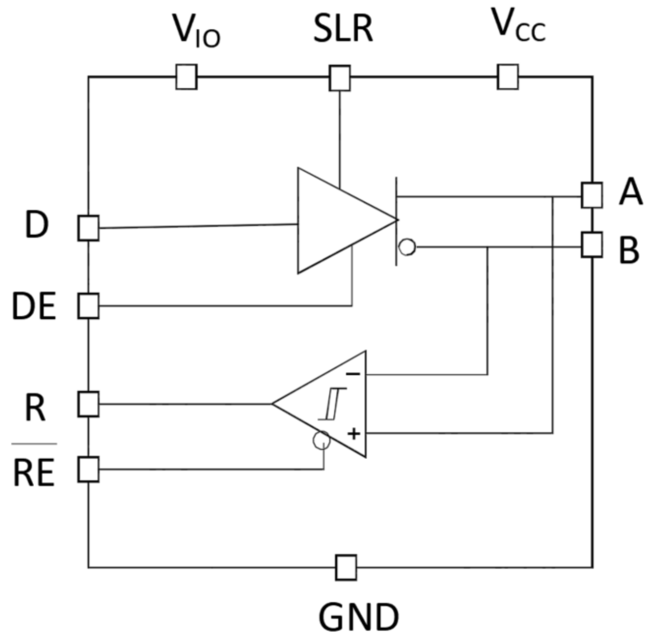


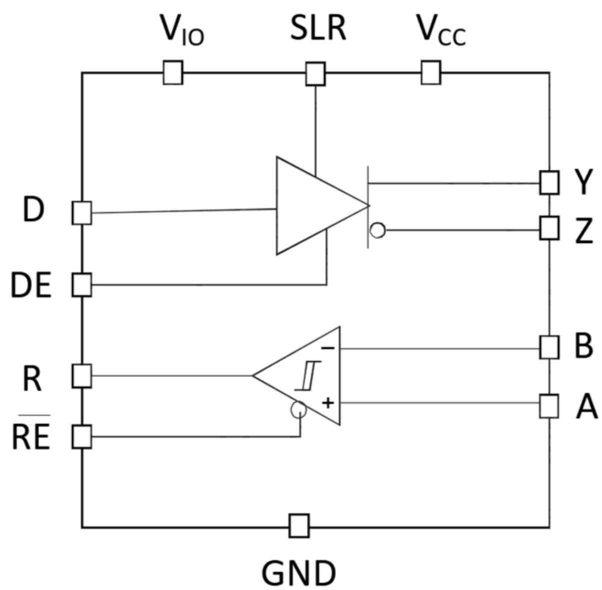

FIGURE 2. Terminal connections.

| Case outline | X | Y | X, Y | |
|---|---|---|---|---|
| Terminal symbol | Device type 01, 02 | Device type 03 | Type | Description |
| | Terminal number | | | |
| $V_{IO}$ | 1 | 1 | Logic supply | 1.65 V to 5.5 V supply for logic I/O signals (R, $\overline{RE}$, D, DE, and SLR) |
| R | 2 | 2 | Digital output | Receive data output |
| DE | 3 | 3 | Digital input | Driver enable input; integrated pull-down |
| $\overline{RE}$ | 4 | 4 | Digital input | Receiver enable input; integrated pull-up |
| D | 5 | 5 | Digital input | Transmission data input; integrated pull-up |
| GND | 6 | 6 | Reference potential | Local device ground |
| SLR | 7 | 8 | Digital input | Slew rate select; integrated pull-down. For THVD2410V-EP: low = 1 Mbps, high = 250 kbps. Defaults to 1 Mbps if SLR is left floating. For THVD2450V-EP and THVD2452V-EP: low = 50 Mbps, high = 20 Mbps. Defaults to 50 Mbps if left floating |
| A | 8 | 11 | Bus input | Bus I/O (half-duplex), bus input (full-duplex) |
| B | 9 | 12 | Bus input | Bus I/O (half-duplex), bus input (full-duplex) |
| $V_{CC}$ | 10 | 14 | Bus supply | 3 V to 5.5 V supply for the transceiver |
| Y | - | 9 | Bus output | Bus output, Y |
| Z | - | 10 | Bus output | Bus output, Z |
| NC | - | 7, 13 | | No connect pin. Internally not connected |

FIGURE 2. Terminal connections – Continued.




**Device types 01, 02: THVD2410V-EP and THVD2450V-EP**




**Device type 03: THVD2452V-EP**

FIGURE 3. Functional block diagram.

**Driver**

| Input | Enable | Outputs | | Function |
|---|---|---|---|---|
| **D** | **DE** | **A/Y** | **B/Z** | |
| H | H | H | L | Actively drive bus high |
| L | H | L | H | Actively drive bus low |
| X | L | Z | Z | Driver disabled |
| X | Open | Z | Z | Driver disabled by default |
| Open | H | H | L | Actively drive bus high by default |

**Receiver**

| Differential input | Enable | Outputs | Function |
|---|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | **R** | |
| $V_{TH+} < V_{ID}$ | L | H | Receive valid bus high |
| $V_{TH-} < V_{ID} < V_{TH+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{TH-}$ | L | L | Receive valid bus low |
| X | H | Z | Receiver disabled |
| X | Open | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

FIGURE 4. Functional modes.

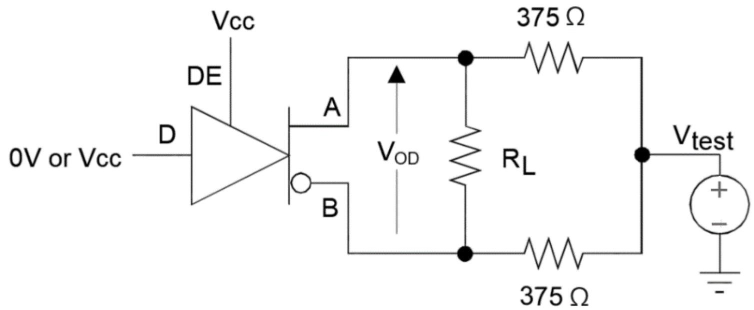



FIGURE 5. Measurement of driver differential output voltage with common-mode load.

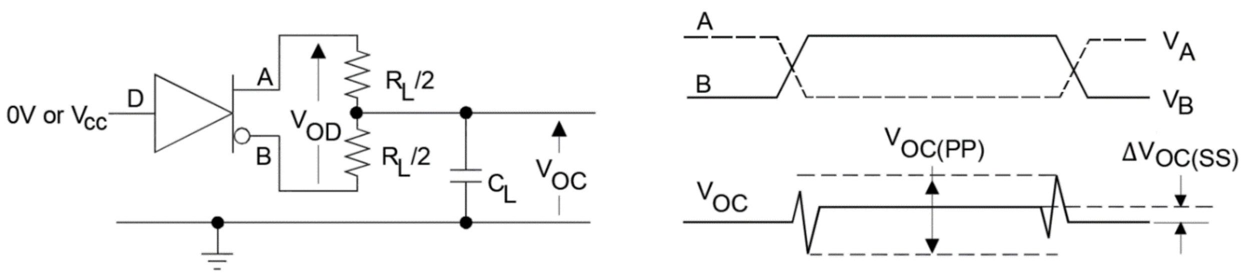



FIGURE 6. Measurement of driver differential and common mode output with RS-485 load.

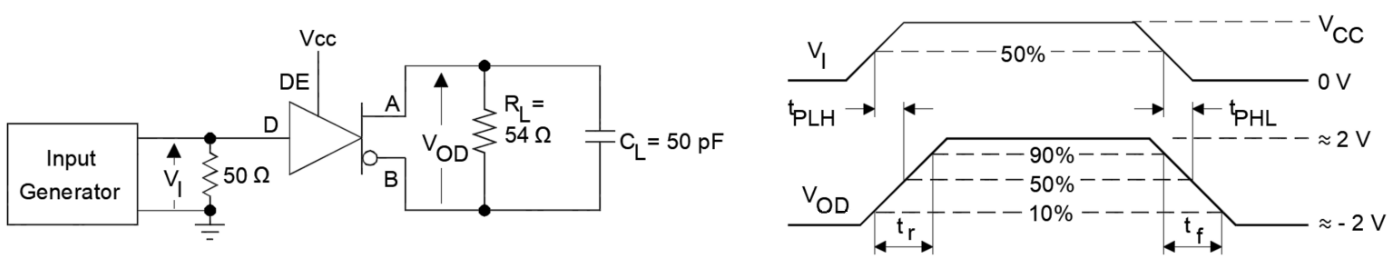



FIGURE 7. Measurement of driver differential output rise and fall times and propagation delays.

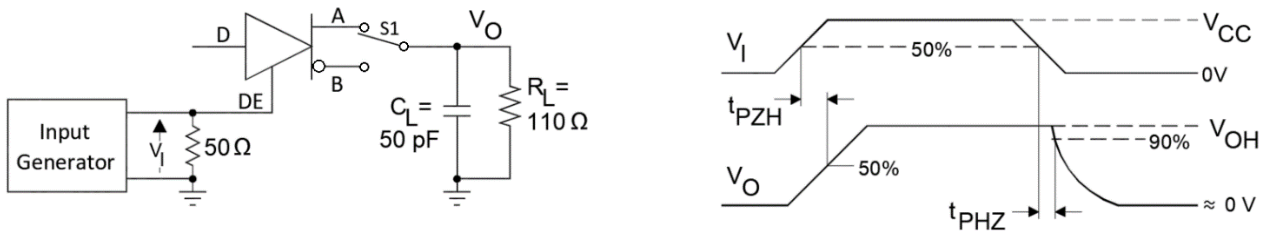



FIGURE 8. Measurement of driver enable and disable times with active high output and pull-down load.

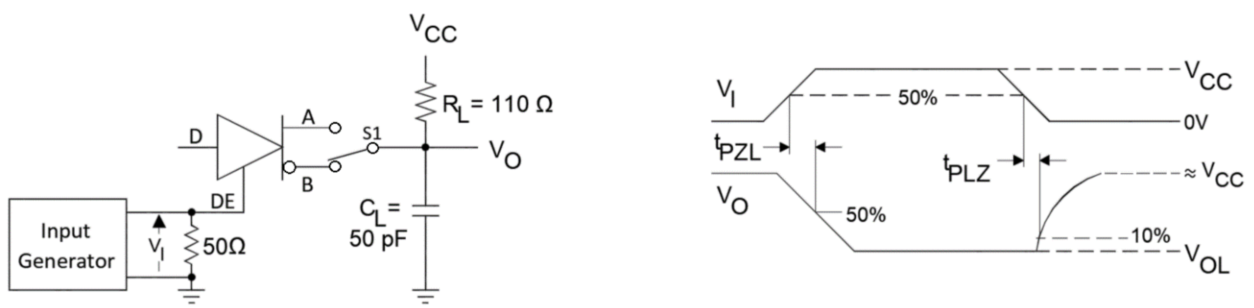



FIGURE 9. Measurement of driver enable and disable times with active low output and pull-up load.

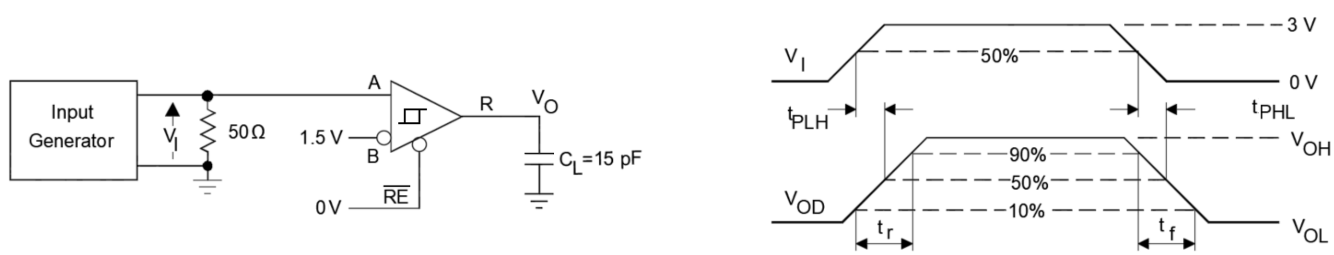



FIGURE 10. Measurement of receiver output rise and fall times and propagation delays.

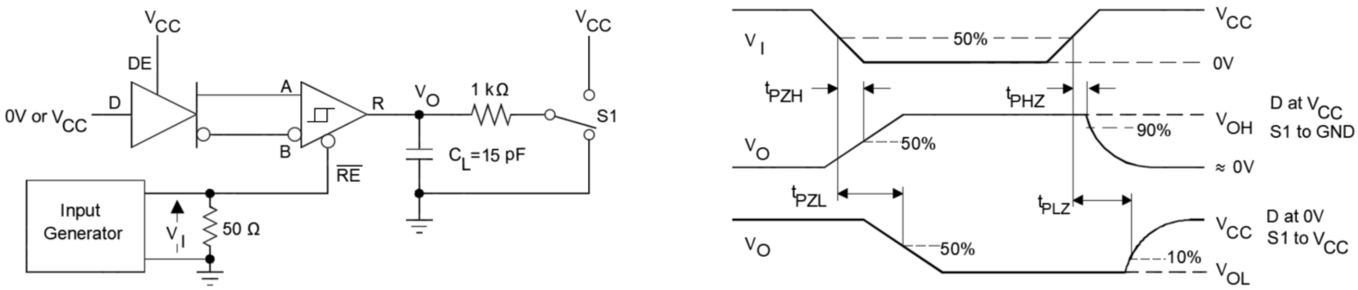



FIGURE 11. Measurement of receiver enable/disable times with driver enabled.

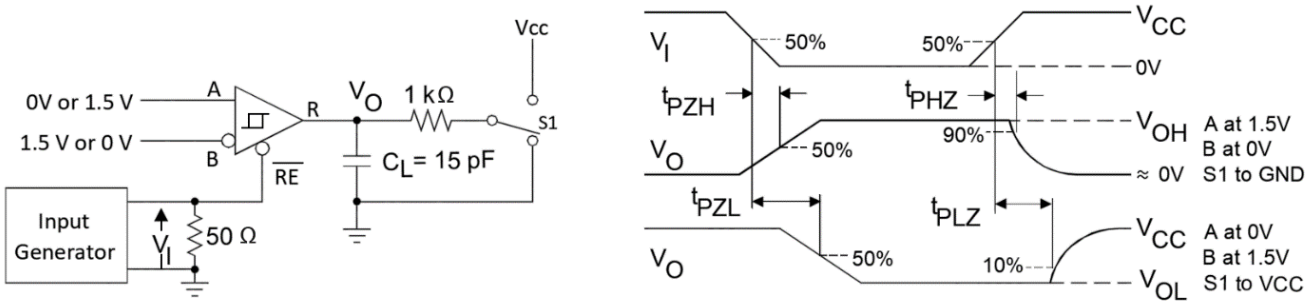



FIGURE 12. Measurement of receiver enable times with driver disabled.

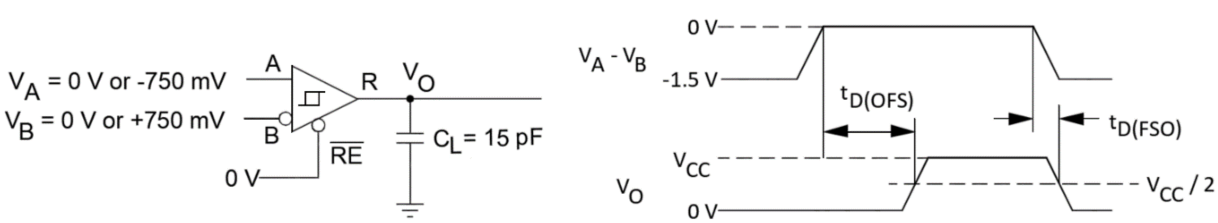



FIGURE 13. Measurement of fail-safe delay.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Manufacturer(s) performed devices electrostatic discharge sensitive rate with Human body model (HDM) and classified as ESDS class 1 minimum 2000 V and also performed ESDS rate with Charge device model (CDM) and classified as ESDS is 250 V.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Mode of transportation and quantity | Top side marking | Vendor part number |
|---|---|---|---|---|
| V6222613-01XE | 01295 | Reel, 5000 units | V2410 | THVD2410VDRCREP |
| V6222613-02XE | 01295 | Reel, 5000 units | V2450 | THVD2450VDRCREP |
| V6222613-03YE | 01295 | Reel, 5000 units | T2452V | THVD2452VDREP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments Inc.<br>12500 TI Blvd.<br>Dallas, TX 75243 |