REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-12-05	**CHECKED BY** RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, BiCMOS, HIGH PERFORMANCE, 15 GHz, WIDEBAND RF SYNTHESIZER WITH PHASE SYNCHRONIZATION, MONOLITHIC SILICON
	APPROVED BY JAMES R. ESCHMEYER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/19616**
	REV	**PAGE** 1 **OF** 21

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AMSC N/A

5962-V116-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 15 GHz wideband radio frequency (RF) synthesizer with phase synchronization microcircuit, with an operating temperature range of -55°C to +115°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	LMX2694-EP	15 GHz wideband radio frequency (RF) synthesizer with phase synchronization
02 1/	LMX2694-SEP	Radiation hardened 15 GHz wideband radio frequency (RF) synthesizer with phase synchronization

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	See figure 1	Quad flat non-leaded package (QFN)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1/ Device type 02 is radiation hardened per section 1.6.

1.3 Absolute maximum ratings. 2/

Power supply voltage range (V_{CC}) ..... -0.3 V to 3.6 V
IO input voltage ..... V_{CC} + 0.3 V maximum
Junction temperature range (T_J) ..... -55°C to +115°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM) per JEDEC JS-0001 ..... 2000 V 3/
Charge device model (CDM) per JEDEC JESD22-C101, all pins ..... 500 V 4/

1.4 Recommended operating conditions. 5/

Case temperature range (T_C) ..... -55°C to +115°C
Junction temperature range (T_J) ..... +125°C maximum

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	22.7	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	7.3	°C/W
Thermal resistance, junction-to-board	θ_{JB}	7.6	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOT)}$	1.0	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	2.2	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	7.4	°C/W

1.6 Radiation features.

Device type 02.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) ..... 20 krads(Si) 6/

Single event phenomenon (SEP):
No Single event latchup (SEL) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 7/

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ Device type 02 supplied to this drawing has been characterized for Enhanced Low Dose Rate Sensitivity (ELDRS) to 30 krad(Si) with testing at Low Dose Rate (LDR) and High Dose Rate (HDR) and was shown not to exhibit ELDRS per MIL-STD-883, method 1019. This device’s Radiation Lot Acceptance Testing is performed to 20 krads(Si) per method 1019, condition A (50 to 300 rad(Si)/s).
7/ For more information on SEP test results, customers are requested to contact the manufacturer (see SEP table IB).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 – Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels
JESD 204 – Serial Interface for Data Converters

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figures 4, 5, and 6.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Power supply								
Supply voltage	V_{CC}			+25°C	01, 02	3.3. typical		V
				-50°C to +115°C	01	3.2	3.45	
					02	3.15	3.45	
Supply current	I_{CC}	OUTA_PD = 0; OUTB_PD = 1, OUT_MUX = OUTB_MUX = 1, OUTA_PWR = 31, CPG = 7, $f_{OSC} = f_{PD}$ = 100 MHz, $f_{VCO} = f_{OUT}$ = 14.5 GHz		+25°C	01, 02	360 typical		mA
Power on reset current	I_{CC}	RESET = 1		+25°C	01, 02	289 typical		mA
Power down current	I_{CC}	POWERDOWN = 1		+25°C	01, 02	6 typical		mA
Output characteristics								
Single ended 4/ 5/ output power	p_{OUT}	50 Ω resistor pull up, OUTx_PWR = 31	f_{OUT} = 8 GHz	+25°C	01, 02	2 typical		dBm
			f_{OUT} = 15 GHz			0 typical		
Input signal path								
Reference input frequency	f_{OSC}	OSC_2X = 0		-50°C to +115°C	01, 02	5	1000	MHz
		OSC_2X = 1				5	200	
Reference input 6/ voltage	V_{OSC}	$f_{OSC} \geq$ 20 MHz		-50°C to +115°C	01, 02	0.4	2	V_{PP}
		10 MHz $\leq f_{OSC} <$ 20 MHz				0.8	2	
		5 MHz $\leq f_{OSC} <$ 10 MHz				1.6	2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Phase detector and charge pump								
Phase detector 7/ frequency	f_{PD}	MASH_ORDER = 0		-50°C to +115°C	01, 02	0.125	250	MHz
		MASH_ORDER > 0				5	200	
Charge pump leakage current	I_{CPOUT}	CPG = 0		+25°C	01, 02	20 typical		nA
Effective charge pump current	I_{CPOUT}	CPG = 0 to 7		+25°C	01, 02	3 to 15 typical		mA
Normalized PLL 1/f noise	$PN_{PLL\_1/f}$	f_{PD} = 100 MHz, 8/ f_{VCO} = 12 GHz		+25°C	01, 02	-129 typical		dBc/Hz
Normalized PLL noise floor	PN_{PLL_FOM}	f_{PD} = 100 MHz, 8/ f_{VCO} = 12 GHz		+25°C	01, 02	-236 typical		dBc/Hz
VCO characteristics								
VCO phase noise	PN_{VCO}	VCO1, f_{VCO} = 8.1 GHz	100 kHz	+25°C	01, 02	-106.5 typical		dBc/Hz
			1 MHz			-128 typical		
			10 MHz			-147.5 typical		
			100 MHz			-154 typical		
		VCO2, f_{VCO} = 9.3 GHz	100 kHz			-105 typical		
			1 MHz			-126.5 typical		
			10 MHz			-14.5 typical		
			100 MHz			-154 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
VCO characteristics – continued.								
VCO phase noise	PN_{VCO}	VCO3, f_{VCO} = 10.4 GHz	100 kHz	+25°C	01, 02	-103.5 typical		dBc/Hz
			1 MHz			-125.5 typical		
			10 MHz			-146 typical		
			100 MHz			-158 typical		
		VCO4, f_{VCO} = 11.4 GHz	100 kHz			-102.5 typical		
			1 MHz			-124.5 typical		
			10 MHz			-145 typical		
			100 MHz			-160 typical		
		VCO5, f_{VCO} = 12.5 GHz	100 kHz			-100.5 typical		
			1 MHz			-122.5 typical		
			10 MHz			-143.5 typical		
			100 MHz			-154.5 typical		
		VCO6, f_{VCO} = 13.6 GHz	100 kHz			-99.5 typical		
			1 MHz			-122 typical		
			10 MHz			-142.5 typical		
			100 MHz			-154 typical		
		VCO7, f_{VCO} = 14.7 GHz	100 kHz			-98 typical		
			1 MHz			-120.5 typical		
			10 MHz			-141.5 typical		
			100 MHz			-155 typical		
VCO calibration time	t_{VCOCAL}	Partial assist, switch across the entire frequency band; $f_{OSC} = f_{PD}$ = 100 MHz, f_{VCO} = 7.9 GHz, VCO_SEL = 7		+25°C	01, 02	650 typical		µs

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
VCO characteristics – continued.							
VCO gain	K_{VCO}	8.1 GHz	+25°C	01, 02	94 typical		MHz/V
		9.3 GHz			106 typical		
		10.4 GHz			122 typical		
		11.4 GHz			148 typical		
		12.5 GHz			185 typical		
		13.6 GHz			202 typical		
		14.7 GHz			233 typical		
Allowable temperature drift	$\lvert \Delta t_{CL} \rvert$	VCO not being re-calibrated	+25°C	01, 02	125 typical		°C
VCO second harmonic	H2	f_{VCO} = 8 GHz, divider disabled	+25°C	01, 02	-30 typical		dBc
VCO third harmonic	H3	f_{VCO} = 8 GHz, divider disabled	+25°C	01, 02	-25 typical		dBc
Digital interface							
High level input voltage	V_{IH}		-50°C to +115°C	01, 02	1.4		V
Low level input voltage	V_{IL}		-50°C to +115°C	01, 02		0.4	V
High level input current	I_{IH}		-50°C to +115°C	01, 02	-100	100	µA
Low level input current	I_{IL}		-50°C to +115°C	01, 02	-100	100	µA
High level output voltage	V_{OH}	Load current = -5 mA, MUXOUT pin	-50°C to +115°C	01, 02	V_{CC} -0.6		V
Low level output voltage	V_{OL}	Load current = 5 mA, MUXOUT pin	-50°C to +115°C	01, 02		0.6	V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Timing requirements.							
SYNC and SYSRREFREQ timing							
Setup time for pin relative to OSCIN rising edge	t_{SETUP}	See figure 4	-50°C to +115°C	01, 02	9		ns
Hold time for pin relative to OSCIN rising edge	t_{HOLD}	See figure 4	-50°C to +115°C	01, 02	4		ns
Digital interface write specifications							
SPI write speed	$f_{SPI\ Write}$	$t_{CWL} + t_{CWH} \geq 25$ ns	-50°C to +115°C	01, 02		40	MHz
Clock to enable low time	t_{CE}	See figure 5	-50°C to +115°C	01, 02	5		ns
Data to clock setup time	t_{CS}	See figure 5	-50°C to +115°C	01, 02	2		ns
Data to clock hold time	t_{CH}	See figure 5	-50°C to +115°C	01, 02	2		ns
Clock pulse width high	t_{CWH}	See figure 5	-50°C to +115°C	01, 02	5		ns
Clock pulse width low	t_{CWL}	See figure 5	-50°C to +115°C	01, 02	5		ns
Enable to clock setup time	t_{CES}	See figure 5	-50°C to +115°C	01, 02	5		ns
Enable pulse width high	t_{EWH}	See figure 5	-50°C to +115°C	01, 02	2		ns
Digital interface readback specification							
SPI readback speed	$f_{SPI\ Read\ back}$	See figure 6	-50°C to +115°C	01, 02		40	MHz
Clock to enable low time	t_{CE}	See figure 6	-50°C to +115°C	01, 02	5		ns
Clock to data wait time	t_{CS}	See figure 6	-50°C to +115°C	01, 02	2		ns
Clock to data hold time	t_{CH}	See figure 6	-50°C to +115°C	01, 02	2		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued.							
Digital interface readback specification – continued.							
Clock pulse width high	t_{CWH}	See figure 6	-50°C to +115°C	01, 02	10		ns
Clock pulse width low	t_{CWL}	See figure 6	-50°C to +115°C	01, 02	10		ns
Enable to clock setup time	t_{CES}	See figure 6	-50°C to +115°C	01, 02	5		ns
Enable pulse width high	t_{EWH}	See figure 6	-50°C to +115°C	01, 02	2		ns
Falling clock edge to data wait time	t_{CD}	See figure 6	-50°C to +115°C	01, 02		8	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Device type 02 supplied to this drawing has been characterized at 30 krad(Si) of irradiation. However, this device's radiation end point limits for the noted parameters are guaranteed to TID level 20 krad(Si) as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.6 herein).

3/ Unless otherwise specified, 3.2 V ≥ V_{CC} ≤ 3.45 V, -50°C ≤ T_C ≤ +115°C. Typical values are at V_{CC} = 3.3 V at +25°C.

4/ Single ended output power obtained after de-embedding microstrip trace losses and matching with a manual tuner. Unused port terminated to 50 Ω load.

5/ Output power, spurs, and harmonics can vary based on board layout and components.

6/ Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50 Ω resistor.

7/ For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.

8/ The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20 x log(f_{VCO}/f_{PD}) + 10 x log(f_{PD}/1 Hz).
PLL_flicker (offset) = PLL_1/f + 20 x log(f_{VCO}/1 GHz) - 10 x log(offset/10 kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 x log($10^{PLL\_Flat/10} + 10^{PLL\_flicker/10}$).

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_C)	V_{IN}	Effective linear energy transfer (LET)
02	No SEL	+125°C	3.45 V	$\leq$ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ SEE test shall be perform in accordance with ASTM F1192 .or JESD57. For more information on SEP test results, customers are requested to contact the manufacturer

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 02 and as specified in 1.6 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° $\leq$ angle $\leq$ 60°). No shadowing of the ion beam due to fixuring or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C $\pm$10%.

f. For SEL test limits, see table IB herein.

Case X

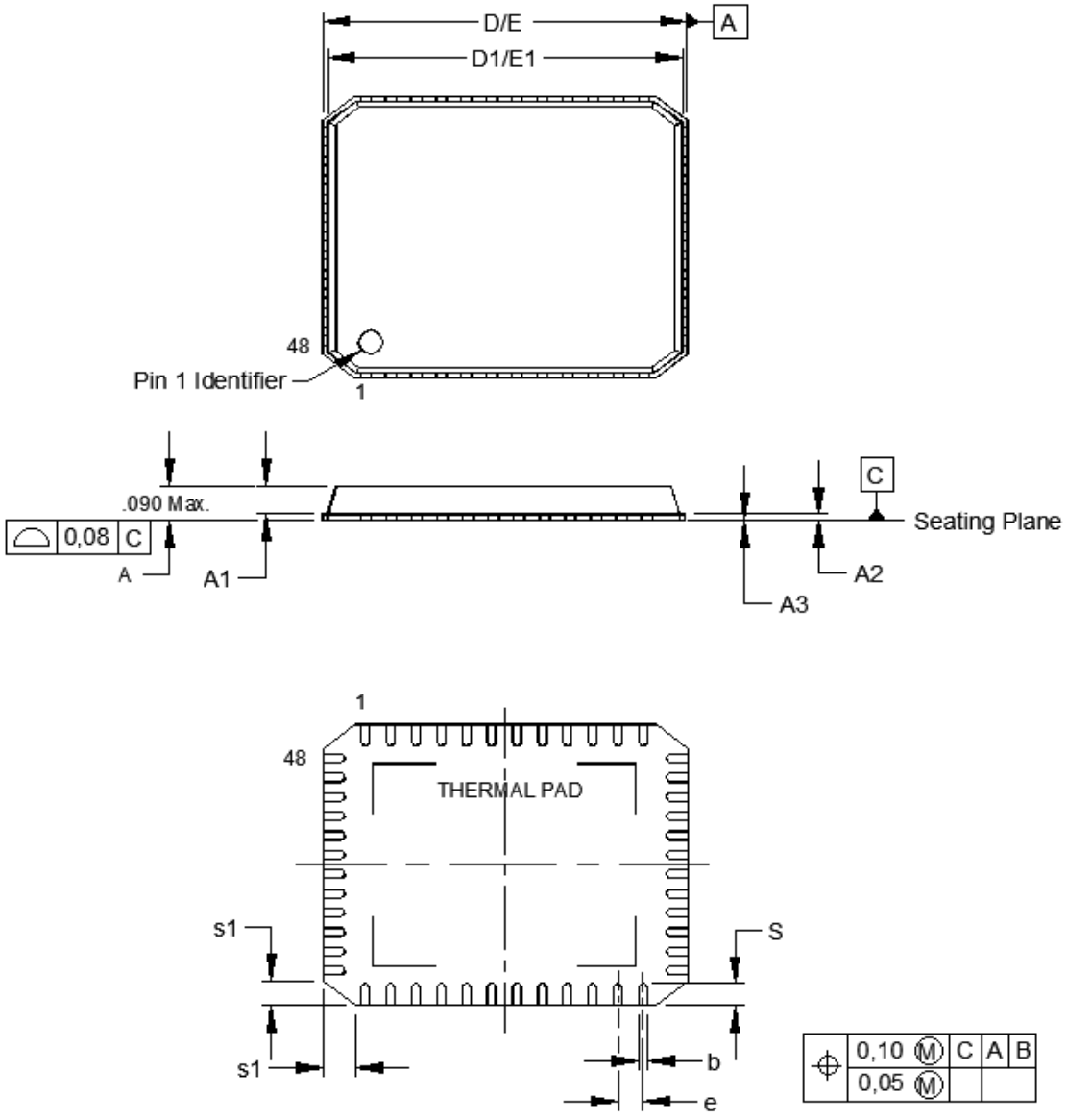

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/19616
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Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.035	---	0.90
A1	---	.027	---	0.70
A2	.008 REF		0.20 REF	
A3	.000	.002	0.00	0.05
b	.007	.012	0.18	0.30
D/E	.272	.279	6.90	7.10
D1/E1	.262	.270	6.65	6.85
e	.020 BSC		0.50 BSC	
S	.012	.020	0.30	0.50
s1	.009	.024	0.24	0.60

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance.
3. See additional figure in the manufacturer’s datasheet for details regarding thermal pad features and dimensions.

FIGURE 1. Case outline - Continued.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CE	25	RFOUTA_M
2	GND	26	RFOUTA_P
3	BIASVCO	27	GND
4	GND	28	CSB
5	SYNC	29	GND
6	GND	30	GND
7	VCCDIG	31	GND
8	OSCIN_P	32	GND
9	OSCIN_M	33	VCCVCO2
10	REGIN	34	BIASVCO2
11	GND	35	SYSREFREQ
12	GND	36	REFVCO2
13	VCCCP	37	GND
14	CPOUT	38	GND
15	GND	39	GND
16	GND	40	GND
17	VCCMASH	41	BIASVARAC
18	SCK	42	GND
19	SDI	43	VTUNE
20	GND	44	REFVCO
21	RFOUTB_M	45	VCCVCO
22	RFOUTB_P	46	REGVCO
23	MUXOUT	47	GND
24	VCCBUF	48	GND

FIGURE 2. Terminal connections.

Device type	01, 02			
Case outline	X			
Terminal symbol	Terminal number	I/O	Type	Description
BIASVARAC	41	—	Bypass	VCO varactor bias. Connect a 10 µF decoupling capacitor to ground.
BIASVCO	3	—	Bypass	VCO bias. Connect a 10 µF decoupling capacitor to ground. Place close to pin.
BIASVCO2	34	—	Bypass	VCO bias. Connect a 1 µF decoupling capacitor to ground. Place close to pin.
CE	1	I	—	Chip Enable. High impedance CMOS input. 1.8 V to 3.3 V logic. Active HIGH powers on the device.
CPOUT	14	O	—	Charge pump output. Recommend connecting C1 of loop filter close to this pin.
CSB	28	I	—	SPI latch. High impedance CMOS input. 1.8 V to 3.3 V logic.
GND	2, 4, 32, 40, 42, 47	—	Ground	VCO ground.
GND	6, 16, 48	—	Ground	Digital ground.
GND	15	—	Ground	Charge pump ground.
GND	27, 29	—	Ground	Buffer ground.
MUXOUT	23	O	—	Multiplexed output. Can output: lock detect, SPI readback and diagnostics.
NC	11, 12, 20, 30, 31, 37, 38, 39	—	No connect	Pins may be grounded or left unconnected.
OSCIN_M	9	I	—	Reference input clock (–). High impedance self-biasing pin. Requires AC-coupling capacitor. (0.1 µF recommended)
OSCIN_P	8	I	—	Reference input clock (+). High impedance self-biasing pin. Requires AC-coupling capacitor. (0.1 µF recommended)
REFVCO	44	—	Bypass	VCO supply reference. Connect a 10 µF decoupling capacitor to ground.
REFVCO2	36	—	Bypass	VCO supply reference. Connect a 10 µF decoupling capacitor to ground.
RECAL_EN	37	I	---	Enables the automatic re-calibration feature. High impedance CMOS input. 1.8 V to 3.3 V logic. Leave open if not being used.

FIGURE 2. Terminal connections - Continued.

Device types	01, 02			
Case outline	X			
Terminal symbol	Terminal number	I/O	Type	Description
REGIN	10	—	Bypass	Input reference path regulator decoupling. Connect a 1 µF decoupling capacitor to ground. Place close to pin.
REGVCO	46	—	Bypass	VCO regulator node. Connect a 1 µF decoupling capacitor to ground.
RFOUTA_M	25	O	—	Differential output A (–). Requires connecting 50 Ω resistor pullup to V_{CC} as close as possible to pin.
RFOUTA_P	26	O	—	Differential output A (+). Requires connecting 50 Ω resistor pullup to V_{CC} as close as possible to pin.
RFOUTB_M	21	O	—	Differential output B (–). Requires connecting 50 Ω resistor pullup to V_{CC} as close as possible to pin.
RFOUTB_P	22	O	—	Differential output B (+). Requires connecting 50 Ω resistor pullup to V_{CC} as close as possible to pin.
SCK	18	I	—	SPI clock. High impedance CMOS input. 1.8 V to 3.3 V logic.
SDI	19	I	—	SPI data. High impedance CMOS input. 1.8 V to 3.3 V logic.
SYNC	5	I	—	Phase synchronization input. Has programmable threshold. Connect to ground, if not being used.
SYSREFREQ	35	I	—	SYSREF request input for JESD204B support. Connect to ground if not being used.
VCCBUF	24	—	Supply	Output buffer supply. Connect to 3.3 V and a 0.1 µF decoupling capacitor to ground.
VCCCP	13	—	Supply	Charge pump supply. Connect to 3.3 V and a 0.1 µF decoupling capacitor to ground.
VCCDIG	7	—	Supply	Digital supply. Connect to 3.3 V and a 0.1 µF decoupling capacitor to ground.
VCCMASH	17	—	Supply	Digital supply. Connect to 3.3 V and a 1 µF decoupling capacitor to ground.
VCCVCO	45	—	Supply	VCO supply. Connect to 3.3 V and a 1 µF decoupling capacitor to ground.
VCCVCO2	33	—	Supply	VCO supply. Connect to 3.3 V and a 1 µF decoupling capacitor to ground.
VTUNE	43	I	—	VCO tuning voltage input. Connect a 1.5 nF or more capacitor to VCO ground. See manufacturer for details.

FIGURE 2. Terminal connections - Continued.

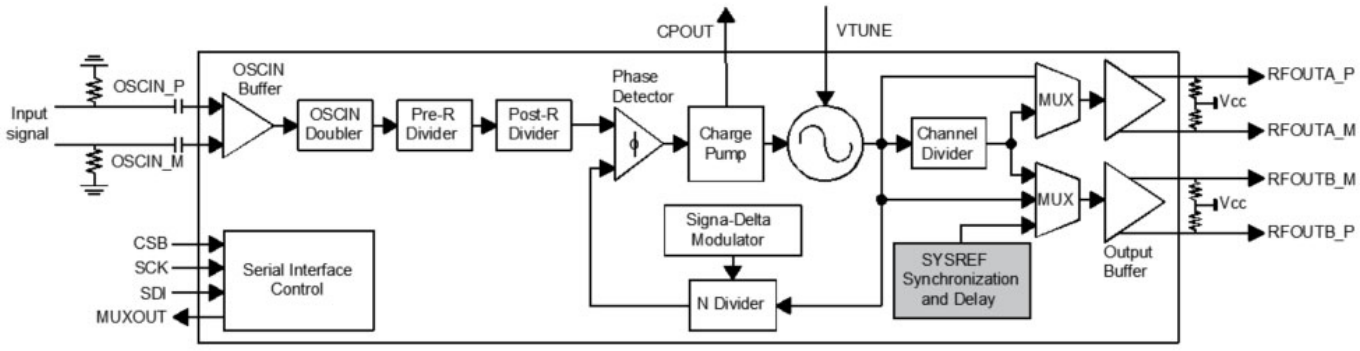


FIGURE 3. Functional block diagram.

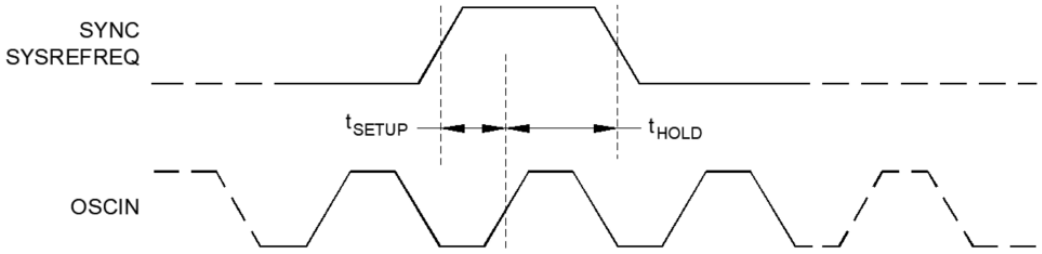
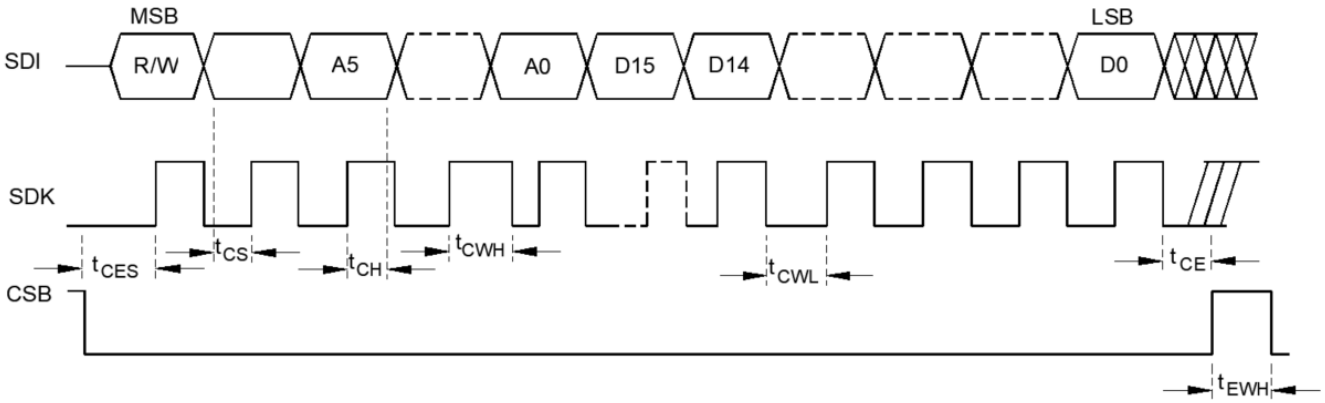


FIGURE 4. Trigger signals timing diagram.

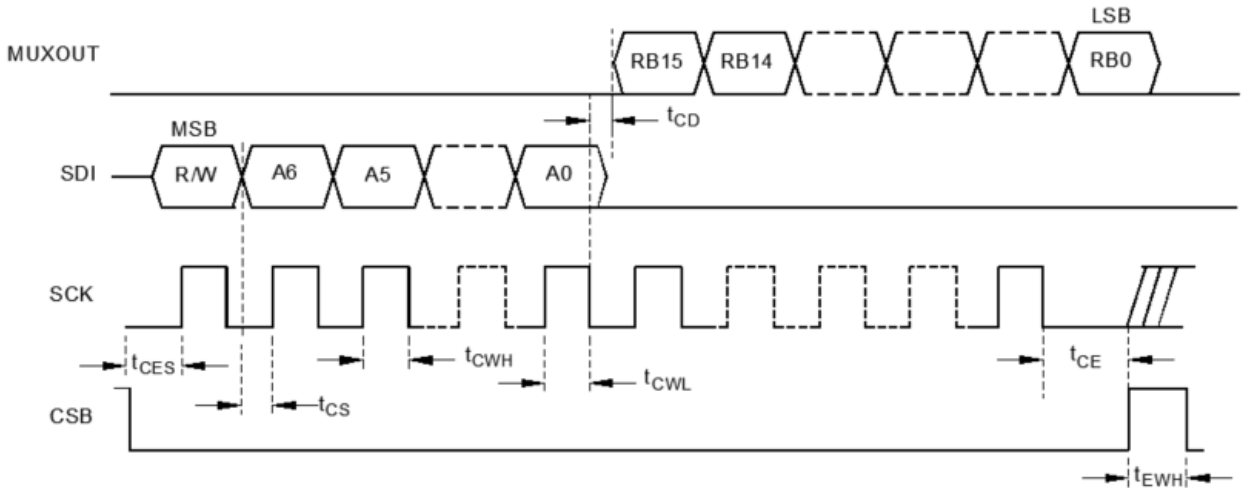


NOTES:

There are several other considerations for writing on the SPI:

1. The R/W bit must be set to 0.
2. The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
3. The CSB must be held low for data to be clocked. Device will ignore clock pulses if CSB is held high.
4. The CSB transition from high to low must occur when SCK is low.
5. When SCK and SDI lines are shared between devices, the manufacturer recommends to hold the CSB line high on the device that is not to be clocked.

FIGURE 5. Serial data input timing diagram.



NOTES:

There are several other considerations for SPI readback:

1. The R/W bit must be set to 1.
2. The MUXOUT pin will always be low for the address portion of the transaction.
3. The data on MUXOUT becomes available momentarily after the falling edge of SCK, and therefore, should be read back on the rising edge of SCK.
4. The data portion of the transition on the SDI line is always ignored.

FIGURE 6. Serial data readback timing diagram.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 (2000V) minimum per Human body model (HDM) per JEDEC JS-0001 and Charge device model (CDM) to ESDS to 500V (all pins) per JEDEC JESD22-C101.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/19616-01XE	01295	LMX2694-EP
V62/19616-02XE	01295	LMX2694-SEP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ This device has been RHA TID tested to 20 krads(Si) (see paragraph 1.6 herein).

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243