REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. - ro	25-02-27	LAURA LEEPER BRANHAM
B	Delete the words MONOLITHIC SILICON from the title block. Under paragraph 1.3, Electrostatic discharge (ESD) rating section. Charged Device Model (CDM) limit revised from ±750 V to ±500 V per request from manufacturer. - ro	25-04-01	JAMES R. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

Original date of drawing (YR-MO-DA)

24-12-20

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TITLE

MICROCIRCUIT, HALF BRIDGE GALLIUM NITRIDE (GaN), FET GATE DRIVERS

SIZE	CAGE CODE
A	16236

DWG NO. V62/24632

REV B

PAGE 1 OF 20

AMSC N/A

5962-V072-25

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance half bridge gallium nitride (GaN) field effect transistor (FET) gate drivers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/24632	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types.

Device type	Generic	Absolute maximum voltage	Recommended operating voltage	Circuit function
01	TPS7H6005-SEP	200 V	150 V	Half bridge GaN FET gate driver
02	TPS7H6015-SEP	60 V	45 V	Half bridge GaN FET gate driver
03	TPS7H6025-SEP	22 V	14 V	Half bridge GaN FET gate driver

1.2.2 Case outline. The case outline is as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	56	MO-153	Thin shrink small outline package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

VIN to AGND	-0.3 V to 16 V
BP7L to AGND	-0.3 V to 8 V
BP5L to AGND	-0.3 V to 7 V
BP5H to AGND	-0.3 V to 7 V
BOOT to SW	-0.3 V to [V_{SW} + 16] V
EN_HI	-0.3 V to 16 V
PWM_LI	-0.3 V to 16 V
DHL, DLH	-0.3 V to [V_{BP5L} + 0.3] V
LOH, LOL	-0.3 V to [V_{BP5L} + 0.3] V
HOH, HOL	[V_{SW} – 0.3] V to [V_{BP5H} + 0.3] V
PGOOD	-0.3 V to [V_{BP5L} + 0.3] V
SW to AGND:	
Device type 01	-10 V to 200 V
Device type 02	-10 V to 60 V
Device type 03	-10 V to 22 V
BOOT to AGND:	
Device type 01	0 V to 216 V
Device type 02	0 V to 76 V
Device type 03	0 V to 38 V
BST to AGND	-0.3 V to 16 V
BST current (3 µs transient pulse, non-repetitive)	4 A maximum
Junction temperature range (T_J)	-55°C to 150°C
Storage temperature range (T_{STG})	-65°C to 150°C
Thermal resistance, junction to ambient ($R\theta_{JA}$)	21.4°C/W
Thermal resistance, junction to case (top) ($R\theta_{JC(top)}$)	9.2°C/W
Thermal resistance, junction to case (bottom) ($R\theta_{JC(bot)}$)	0.4°C/W
Thermal resistance, junction to board ($R\theta_{JB}$)	5.4°C/W
Characterization parameter, junction to top (Ψ_{JT})	0.3°C/W
Characterization parameter, junction to board (Ψ_{JB})	5.3°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM), per JEDEC JS-001	±2000 V 2/
Charge device model (CDM), per JEDEC JS-002	±500 V 3/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

1.4 Recommended operating conditions. 4/

VIN to AGND	10 V to 14 V
EN_HI	0 V to 14 V
PWM_LI	0 V to 14 V
BOOT to SW	[V_{SW} + 8] V to [V_{SW} + 14] V
Device type 01	-10 V to 150 V
Device type 02	-10 V to 45 V
Device type 03	-10 V to 14 V
SW slew rate	100 V/ns maximum
VIN slew rate	0.03 V/µs maximum
PWM_LI, EN_HI slew rate	2 V/µs minimum
Operating junction temperature range (T_J)	-55°C to 125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s)	50 krad(Si) 5/
Heavy ion single event phenomenon (SEP):	
No Single event latch-up (SEL) occurs at effective LET_{eff} (see 4.3)	≤ 43 MeV/(mg/cm^2) 6/
No Single event burnout (SEB) occurs at LET_{eff} (see 4.3)	≤ 43 MeV/(mg/cm^2) 6/
No Single event gate rupture (SEGR) occurs at LETeff (see 4.3)	≤ 43 MeV/(mg/cm^2) 6/

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for products used beyond the stated limits.

5/ Device types 01, 02, and 03 supplied to this drawing have been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krad(Si) as specified herein.

6/ Heavy ion single event effects (SEE) test was performed using the 15-A MeV cocktail and K500 beam line at TAMU Cyclotron Institute Radiation Effects Facility. No single event latch-up (SEL) occurred under Silver (Ag) ions at Vmax supply voltage and operating temperature 125°C for SEL and for SEB/SEGR temperature 25°C corresponding to an effective LET of 43 MeV/(mg/cm^2). For more information on SEE test, please contact device manufacturer (see SEP table IB).

2. APPLICABLE DOCUMENTS

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) INTERNATIONAL

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

International Electrotechnical Commission

IEC 60664 – Insulation coordination for equipment within low voltage systems

(Copies of these documents are available online at https://www.iec.org.)

JEDEC Solid State Technology Association

JEDEC MO-153 – Plastic Dual Small Outline, Rectangular Family Package
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Block diagram. The block diagram shall be as shown in figure 4.

3.5.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SUPPLY VOLTAGE							
Low side quiescent current	I_{QLS}	MODE = PWM, EN = 0 V, VIN = 12 V, BOOT = 10 V	-55°C to +125°C	01, 02, 03		6.8	mA
					5 typical		
		MODE = IIM, LI = HI = 0 V, VIN = 12 V, BOOT = 10 V				8	
					5 typical		
High side quiescent current	I_{QHS}	MODE = PWM, EN = 0 V, VIN = 12 V, BOOT = 10 V	-55°C to +125°C	01, 02, 03		6.3	mA
					4 typical		
		MODE = IIM, LI = HI = 0 V, VIN = 12 V, BOOT = 10 V				6.3	
					4 typical		
BOOT to AGND quiescent	I_{QBG}	SW = 100 V, BOOT = 110 V	-55°C to +125°C	01	20 typical		µA
		SW = 28 V, BOOT = 38 V		02	15 typical		
		SW = 12 V, BOOT = 22 V		03	10 typical		
BOOT to AGND operating current	I_{OP_BG}	SW = 100 V, BOOT = 110 V	-55°C to +125°C	01	20 typical		µA
		SW = 28 V, BOOT = 38 V		02	15 typical		
		SW = 12 V, BOOT = 22 V		03	10 typical		
Low-side operating current	I_{OP_LS}	MODE = PWM, f = 500 kHz, no load for LOL and LOH	-55°C to +125°C	01, 02, 03		9	mA
					6 typical		
		MODE = PWM, f = 1 MHz, no load for LOL and LOH				11	
					8 typical		
		MODE = PWM, f = 2 MHz, no load for LOL and LOH				16	
					12 typical		
		MODE = PWM, f = 5 MHz, no load for LOL and LOH				30	
					20 typical		
		MODE = IIM, f = 500 kHz, no load for LOL and LOH				9	
					6 typical		
		MODE = IIM, f = 1 MHz, no load for LOL and LOH				12	
					8 typical		
		MODE = IIM, f = 2 MHz, no load for LOL and LOH				17	
					11 typical		
		MODE = IIM, f = 5 MHz, no load for LOL and LOH				30	
					20 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SUPPLY VOLTAGE – continued.							
High side operating current	I_{OP_HS}	MODE = PWM, f = 500 kHz, no load for HOL and HOH	-55°C to +125°C	01, 02, 03		6.5	mA
					5 typical		
		MODE = PWM, f = 1 MHz, no load for HOL and HOH				8	
					5.3 typical		
		MODE = PWM, f = 2 MHz, no load for HOL and HOH				10.5	
					7 typical		
		MODE = PWM, f = 5 MHz, no load for HOL and HOH				19	
					13 typical		
		MODE = IIM, f = 500 kHz, no load for HOL and HOH				6.5	
					4.5 typical		
		MODE = IIM, f = 1 MHz, no load for HOL and HOH				8	
					5.3 typical		
		MODE = IIM, f = 2 MHz, no load for HOL and HOH				10.5	
					7 typical		
		MODE = IIM, f = 5 MHz, no load for HOL and HOH				15	
					11.7 typical		
LOW SIDE TO HIGH SIDE CAPACITANCE							
Low side to high side capacitance		Low side pins shorted together and high side pins shorted together	+25°C	01, 02, 03	6 typical		pF
GATE DRIVER							
Low level output voltage	V_{OL}	I_{OL} = 100 mA	-55°C to +125°C	01, 02, 03		0.15	V
					0.07 typical		
High level output voltage	BP5x – V_{OH}	I_{OH} = 100 mA	-55°C to +125°C	01, 02, 03		0.3	V
					0.13 typical		
Peak source current	I_{OH}	HOH, LOH = 0 V, BP5x = 5 V	-55°C to +125°C	01, 02, 03	0.7	2.3	A
					1.3 typical		
Peak sink current	I_{OL}	HOL, LOL = 5 V, BP5x = 5 V	-55°C to +125°C	01, 02, 03	1.6	4.6	A
					2.5 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
INTERNAL REGULATORS							
Low side 5-V regulator output voltage	V_{BP5L}	C_{BP5L} = 1 µF	-55°C to +125°C	01, 02, 03	4.75 5.0 typical	5.175	V
Required BP5L 4/ output capacitor			-55°C to +125°C	01, 02, 03	1		µF
High side 5-V regulator output voltage	V_{BP5H}	C_{BP5H} = 1 µF	-55°C to +125°C	01, 02, 03	4.75 5.0 typical	5.175	V
Required BP5H 4/ output capacitor			-55°C to +125°C	01, 02, 03	1		µF
7 V regulator output voltage	V_{BP7L}		-55°C to +125°C	01, 02, 03	6.65 7 typical	7.35	V
Required BP7L 4/ output capacitor			-55°C to +125°C	01, 02, 03	1		µF
UNDERVOLTAGE PROTECTION							
BP5H UVLO rising threshold	$BP5H_R$	C_{BP5H} = 1 µF	-55°C to +125°C	01, 02, 03	4.0 4.25 typical	4.5	V
BP5H UVLO falling threshold	$BP5H_F$	C_{BP5H} = 1 µF	-55°C to +125°C	01, 02, 03	3.8 4.05 typical	4.3	V
BP5H UVLO hysteresis	$BP5H_H$	C_{BP5H} = 1 µF	-55°C to +125°C	01, 02, 03	0.2 typical		V
BP5L UVLO rising threshold	$BP5L_R$	C_{BP5L} = 1 µF	-55°C to +125°C	01, 02, 03	4.0 4.25 typical	4.5	V
BP5L UVLO falling threshold	$BP5L_F$	C_{BP5L} = 1 µF	-55°C to +125°C	01, 02, 03	3.8 4.05 typical	4.3	V
BP5L UVLO hysteresis	$BP5L_H$	C_{BP5L} = 1 µF	-55°C to +125°C	01, 02, 03	0.2 typical		V
BP7L UVLO rising threshold	$BP7L_R$	C_{BP7L} = 1 µF	-55°C to +125°C	01, 02, 03	6.2 6.5 typical	6.8	V
BP7L UVLO falling threshold	$BP7L_F$	C_{BP7L} = 1 µF	-55°C to +125°C	01, 02, 03	5.9 6.2 typical	6.5	V
BP7L UVLO hysteresis	$BP7L_H$	C_{BP7L} = 1 µF	-55°C to +125°C	01, 02, 03	0.3 typical		V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
UNDERVOLTAGE PROTECTION – continued.							
VIN UVLO rising threshold	VIN_R		-55°C to +125°C	01, 02, 03	8.0	9.0	V
					8.6 typical		
VIN UVLO falling threshold	VIN_F		-55°C to +125°C	01, 02, 03	7.5	8.5	V
					8.1 typical		
VIN UVLO hysteresis	VIN_H		-55°C to +125°C	01, 02, 03	0.5 typical		V
BOOT UVLO rising threshold	$BOOT_R$		-55°C to +125°C	01, 02, 03	6.6	7.4	V
					7.1 typical		
BOOT UVLO falling threshold	$BOOT_F$		-55°C to +125°C	01, 02, 03	6.2	7	V
					6.65 typical		
BOOT UVLO hysteresis	$BOOT_H$		-55°C to +125°C	01, 02, 03	0.45 typical		V
INPUT PINS							
Input rising edge threshold	V_{IR}		-55°C to +125°C	01, 02, 03	1.80	2.65	V
Input falling edge threshold	V_{IF}		-55°C to +125°C	01, 02, 03	1.15	1.85	V
Input hysteresis	V_{IHYS}		-55°C to +125°C	01, 02, 03	0.8 typical		V
Input pull-down resistance	R_{PD}	V = 2.15 V applied at input (EN_HI or PWM_LI)	-55°C to +125°C	01, 02, 03	100	400	kΩ
PROGRAMMABLE DEAD TIME							
LO off to HO on dead time	T_{DLH}	MODE = PWM, RLH = 3.32 kΩ, LO falling to HO rising (90% to 10%), f ≤ 2 MHz	-55°C to +125°C	01, 02, 03	0	10	ns
					4.5 typical		
		MODE = PWM, RLH = 11.8 kΩ, LO falling to HO rising (90% to 10%), f ≤ 2 MHz			8	15.5	
					12 typical		
		MODE = PWM, RLH = 21 kΩ, LO falling to HO rising (90% to 10%), f ≤ 2 MHz			15.5	24	
					21 typical		
		MODE = PWM, RLH = 52.3 kΩ, LO falling to HO rising (90% to 10%), f ≤ 2 MHz			36	59	
					50 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
PROGRAMMABLE DEAD TIME – continued.							
LO off to HO on dead time	T_{DLH}	MODE = PWM, RLH = 105 kΩ, LO falling to HO rising (90% to 10%), f ≤ 2 MHz	-55°C to +125°C	01, 02, 03	74	113.5	V
					97 typical		
HO off to LO on dead time	T_{DHL}	MODE = PWM, RHL = 7.87 kΩ, HO falling to LO rising (90% to 10%), f ≤ 2 MHz	-55°C to +125°C	01, 02, 03	0	10	V
					5 typical		
		MODE = PWM, RHL = 13.3 kΩ, HO falling to LO rising (90% to 10%), f ≤ 2 MHz			6	15	
					10.5 typical		
		MODE = PWM, RHL = 23.7 kΩ, HO falling to LO rising (90% to 10%), f ≤ 2 MHz			16	24.5	
					21 typical		
		MODE = PWM, RHL = 57.6 kΩ, HO falling to LO rising (90% to 10%), f ≤ 2 MHz			44	61	
					53 typical		
		MODE = PWM, RHL = 113 kΩ, HO falling to LO rising (90% to 10%), f ≤ 2 MHz			81	125	
					105 typical		
BOOTSTRAP DIODE SWITCH							
Bootstrap diode switch resistance	R_{BST_SW}	I_{BST_SW} = 100 mA	-55°C to +125°C	01, 02, 03	0.43 typical		Ω
Bootstrap diode switch parallel resistance		I_{BST_RP} = 1 mA	-55°C to +125°C	01, 02, 03	0.8	1.2	kΩ
					1 typical		
POWER GOOD							
Logic-low output		I_{FLT} = 1 mA	-55°C to +125°C	01, 02, 03		0.4	V
PGOOD internal resistance		BP5L = 5 V, BP7L = 7 V, VIN = 12 V	-55°C to +125°C	01, 02, 03	0.7	1.9	MΩ
					1 typical		
Minimum BP5L voltage for valid PGOOD output			-55°C to +125°C	01, 02, 03		2.85	V
					2 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SWITCHING CHARACTERISTICS							
LO turnoff propagation delay	t_{LPHL}	MODE = PWM, PWM rising to LOL falling	-55°C to +125°C	01, 02, 03		48	ns
					30 typical		
		MODE = IIM, LI falling to LOL falling				38	
					27 typical		
LO turnon propagation delay	t_{LPLH}	MODE = IIM, LI rising to LOH rising	-55°C to +125°C	01, 02, 03		38	ns
					24 typical		
HO turnoff propagation delay	t_{HPHL}	MODE = PWM, PWM falling to HOL falling	-55°C to +125°C	01, 02, 03		50	ns
					35 typical		
		MODE = IIM, HI falling to HOL falling				40	
					30 typical		
HO turnon propagation delay	t_{HPLH}	MODE = IIM, HI rising to HOH rising	-55°C to +125°C	01, 02, 03		40	ns
					26 typical		
Delay matching LO 5/ on and HO off	t_{MON}	MODE = IIM	-55°C to +125°C	01, 02, 03		12	ns
					5.5 typical		
Delay matching LO 5/ off and HO on	t_{MOFF}	MODE = IIM	-55°C to +125°C	01, 02, 03		4	ns
					1.5 typical		
HO rise time	t_{HRC}	C_L = 1000 pF, 10% to 90%	-55°C to +125°C	01, 02, 03		7.5	ns
					3.5 typical		
LO rise time	t_{LRC}	C_L = 1000 pF, 10% to 90%	-55°C to +125°C	01, 02, 03		7.5	ns
					3 typical		
HO fall time	t_{HFC}	C_L = 1000 pF, 90% to 10%	-55°C to +125°C	01, 02, 03		5.5	ns
					4 typical		
LO fall time	t_{LFC}	C_L = 1000 pF, 90% to 10%	-55°C to +125°C	01, 02, 03		5.5	ns
					3 typical		
Minimum input pulse width (turn- on)	t_{PW_IIM}	MODE = IIM	-55°C to +125°C	01, 02, 03		8	ns
					5 typical		
Minimum input pulse width (turn- off)	$t_{PW\_IIM\_OFF}$	MODE = IIM	-55°C to +125°C	01, 02, 03		12	ns
					8 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SWITCHING CHARACTERISTICS – continued.							
Minimum required 4/ input pulse width for targeted dead time	t_{PW_PWM}	MODE = PWM, RLH = 11.8 kΩ, RHL = 13.3 kΩ, DT reduction ≤ 2 ns	-55°C to +125°C	01, 02, 03	22 typical		ns
		MODE = PWM, RLH = 21 kΩ, RHL = 23.7 kΩ, DT reduction ≤ 3 ns			30 typical		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The devices supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krad(Si) as specified herein. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C

3/ Unless otherwise specified, VIN = 10 V to 14 V, V_{BP5L} = V_{BP5H} = 5 V, and no load on LOH, LOL, HOH, and HOL.

4/ Specified by design and not tested in production.

5/ Specification limits for this parameter are represented as an absolute value.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP/SEE	Temperature (T_C)	V_{IN}	Linear energy transfer (LET_{eff})
01, 02, 03	No SEL	125°C	14 V	$LET_{eff} \leq 43$ MeV/(mg/cm^2)
	No SEB	25°C	14 V	$LET_{eff} \leq 43$ MeV/(mg/cm^2)
	No SEGR	25°C	14 V	$LET_{eff} \leq 43$ MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ Heavy ion single event effects (SEE) test was performed using the 15 A MeV cocktail and K500 beam line at TAMU Cyclotron Institute Radiation Effects Facility. No single event latch-up (SEL) occurred under silver(Ag) ions at Vmax supply voltage and operating temperature 125°C for SEL and for SEB/SEGR temperature 25°C corresponding to an effective LET of 43 MeV/(mg/cm^2). For more information on SEE test, please contact device manufacturer (see SEP table IB).

Case X

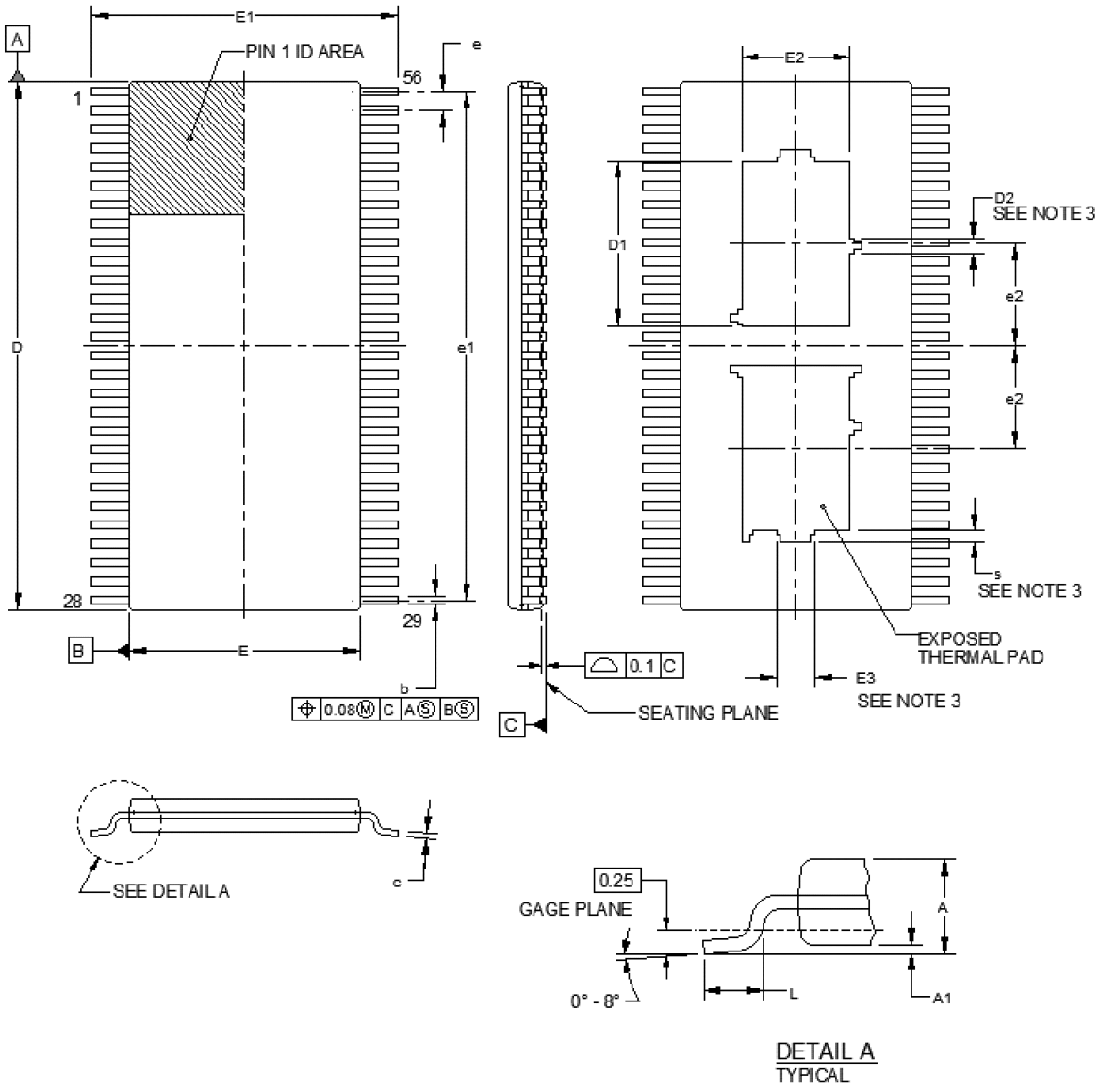

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/24632
		REV B	PAGE 13

Symbol	Dimensions			
	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	1.2	---	0.047
A1	0.05	0.15	0.002	0.006
b	0.17	0.27	0.007	0.011
c	0.15 TYP		0.006 TYP	
D	13.9	14.1	0.547	0.555
D1	4.04	4.70	0.159	0.185
D2	0.4 TYP		0.016 TYP	
E	6.0	6.2	0.236	0.244
E1	7.9	8.3	0.311	0.327
E2	2.54	3.20	0.1	0.126
E3	1.0 TYP		0.039 TYP	
e	0.50 BSC		0.020 BSC	
e1	13.5 BSC		0.531 BSC	
e2	2.71 BSC		0.107 BSC	
L	0.50	0.75	.020	.029
s	0.3 BSC		0.012 BSC	

NOTES:
1. Controlling dimensions are millimeters; inch dimensions are given for reference only.
2. Dimension D does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
3. Features may not be present.
4. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outline - Continued.

Device type	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O (SEE NOTE)	Description
1 - 7	NC	---	Not connected. Pins can be left unconnected or connected to the respective reference voltage (ASW) in order to avoid floating metal and prevent charge buildup.
8	BOOT	I	Input voltage supply of the high-side linear regulator. The external bootstrap capacitor is placed between BOOT and ASW. The cathode of the external bootstrap diode is connected to this pin. A Zener diode clamp may be needed between BOOT and ASW in order to not exceed the absolute maximum electrical rating.
9, 10, 11, 12, 13	ASW	---	High side driver signal return. ASW (pin 9) is internally connected to PSW and the high side thermal pad. Connect ASW (pins 10-13) to ASW externally.
14	NC	---	Not connected. Pin is recommended to be left unconnected in order to meet the requirements of IEC-60664 for creepage and clearance. Ultimately, the connections of pins 14 and 43 are left to the discretion of the user based on the specific creepage and clearance guidelines that are selected for the design.
15	AGND	---	Low side driver signal return. AGND (pin 15) and AGND (pin 19) are internally connected to PGND and the low-side thermal pad. Connect AGND (pin 25) to AGND externally.
16	BST	O	For bootstrap charging that utilizes the internal bootstrap switch, this pin serves as the bootstrap diode anode connection point. The external high side bootstrap capacitor can be charged through this pin using the input voltage applied to VIN, internal bootstrap switch, and external bootstrap diode(s).
17	BP7L	O	Low side 7 V linear regulator output. A minimum of 1 µF capacitance is required from BP7L to AGND.
18	VIN	O	Gate driver input voltage supply. Input voltage range is from 10 V to 14 V. This pin serves as the input to the low side linear regulators and the internal bootstrap switch. For bootstrap charging directly from the input voltage, VIN also serves as the bootstrap diode anode connection point.
19	AGND	---	Low side driver signal return. AGND (pin 15) and AGND (pin 19) are internally connected to PGND and the low side thermal pad. Connect AGND (pin 25) to AGND externally.

FIGURE 2. Terminal connections.

Device types	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O (SEE NOTE)	Description
20	DHL	I	High side to low-side dead time set. In PWM mode, a resistor from DHL to AGND sets the dead time between the high side turn off and low side turn-on. In independent input mode (IIM), DHL is used to configure the input interlock protection of the driver. DHL is connected to BP5L in IIM with interlock enabled. A resistor valued between 100 kΩ and 220 kΩ is connected from DHL to AGND for IIM with interlock disabled.
21	DLH	I	Low side to high-side dead time set. In PWM mode, a resistor from DLH to AGND sets the dead time between the low side turn off and high side turn-on. In independent input mode (IIM), DLH is used to configure the input interlock protection of the driver. A resistor valued between 100 kΩ and 220 kΩ is connected from DLH to AGND for IIM with interlock enabled. DLH is connected to BP5L in IIM with interlock disabled.
22	PGOOD	O	Power good pin. Asserts low when any of the low side internal linear regulators or VIN goes into undervoltage lockout. Requires a 10 kΩ pull-up resistor to BP5L.
23	EN_HI	I	Enable input or high-side driver control input. In PWM mode this is used as an enable pin. In independent input mode (IIM) this serves as the control input for the high side driver.
24	PWM_LI	I	PWM input or low-side driver control input. In PWM mode this is used as the PWM input to the gate driver. In independent input mode (IIM) this serves as the control input for the low side driver.
25	AGND	---	Low side driver signal return. AGND (pin 15) and AGND (pin 19) are internally connected to PGND and the low side thermal pad. Connect AGND (pin 25) to AGND externally.
26, 27, 28	NC	---	Not connected. Pins can be left unconnected or connected to the respective refence voltage (AGND) in order to avoid floating metal and prevent charge buildup.
29, 30, 31, 32	PGND	---	Low side power ground. Connect to the source of the low side GaN FET. Internally connected to AGND and low side thermal pad. Connect to AGND at printed circuit board level.
33, 34, 35	BP5L	O	Low side 5 V linear regulator output. A minimum of 1 µF capacitance is required from BP5L to PGND.
36, 37, 38	LOH	O	Low side driver source current output. Connect to the gate of low side GaN FET with short, low inductance path. A resistor between LOH and the gate of the GaN FET can be used to adjust the turn on speed.
39, 40, 41	LOH	O	Low side driver sink current output. Connect to the gate of the low side GaN FET with short, low inductance path. A resistor between LOL and the gate of the GaN FET can be used to adjust the turn off speed.

FIGURE 2. Terminal connections - continued.

Device types	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O SEE NOTE	Description
42	PGND	---	Low side power ground. Connect to the source of the low-side GaN FET. Internally connected to AGND and low side thermal pad. Connect to AGND at printed circuit board level.
43	NC	---	Not connected. Pin is recommended to be left unconnected in order to meet the requirements of IEC-60664 for creepage and clearance. Ultimately, the connections of pins 14 and 43 are left to the discretion of the user based on the specific creepage and clearance guidelines that are selected for the design.
44, 45, 46, 47	PSW	---	Switch node connection. Connect to the source of the high side GaN FET. Internally connected to ASW and high side thermal pad. Connect to ASW at printed circuit board level.
48, 49, 50	BP5H	O	High side 5 V linear regulator output. A minimum of 1 µF capacitance is required from BP5H to PSW.
51, 52, 53	HOH	O	High side driver source current output. Connect to the gate of the high side GaN FET with short, low inductance path. A resistor between HOH and the gate of the GaN FET can be used to adjust the turn-on speed.
54, 55, 56	HOL	O	High side driver sink current output. Connect to the gate of the high side GaN FET with short, low inductance path. A resistor between HOL and the gate of the GaN FET can be used to adjust the turn-off speed.
---	PSW PAD	---	High side thermal pad. Internally connected to ASW (pin 9) and PSW. Should be connected to ASW pins.
---	PGND PAD	---	Low side thermal pad. Internally connected to AGND (pin 15), AGND (pin 19) and PGND. Should be connected to AGND pins.

NOTE: I = Input, O = Output, I/O = Input or Output, --- = Other.

FIGURE 2. Terminal connections - continued.

Inputs		PWM mode		IIM Interlock disabled		IIM Interlock enabled	
EN_HI	PWM_LI	HO	LO	HO	LO	HO	LO
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1
1	0	0	1	1	0	1	0
1	1	1	0	1	1	0	0

FIGURE 3. Truth table.

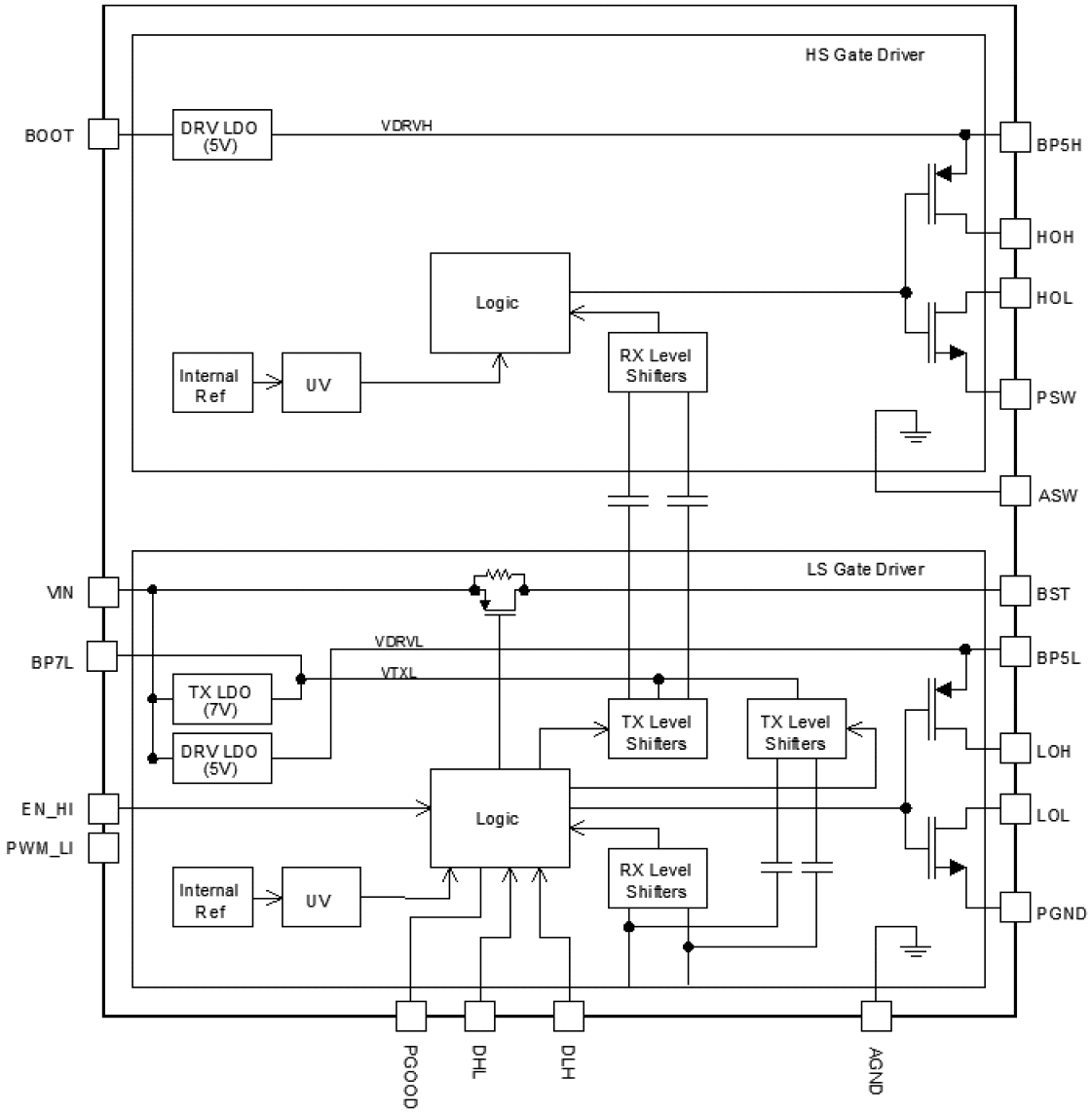

FIGURE 4. Block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for all device types and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +125°C $\pm$10% and for SEB/SEGR test temperature 25°C $\pm$10%.

f. For SEP test limits, see table IB herein.

g. For SEL test limits, see table IB herein.

h. For SEB test limits, see table IB herein.

i. For SEGR test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latch-up (SEL).

c. Occurrence of burnout (SEB).

d. Occurrence of gate rupture (SEGR)

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/24632-01XE	01295	Small tape and reel, 250 units	7H6005DCA	TPS7H6005MDCATSEP
V62/24632-02XE	01295	Small tape and reel, 250 units	7H6015DCA	TPS7H6015MDCATSEP
V62/24632-03XE	01295	Small tape and reel, 250 units	7H6025DCA	TPS7H6025MDCATSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. 12500 TI Blvd. Dallas, TX 75243