REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11											

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 5 V, OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/23618
REV		PAGE 1 OF 11

AMSC N/A

5962-V130-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 5 V, Octal Bus Transceivers with 3-State Outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AHCT245-EP	5 V, Octal Bus Transceivers with 3-State Outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-153	Plastic small-outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7.0 V
Input voltage range (V_I) (Control inputs)..... -0.5 V to 7.0 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Maximum Input clamp current (I_{IK}) (V_I < 0) (Control inputs) ..... -20 mA
Maximum Output clamp current (I_{OK}) (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Maximum Continuous output current (IO) ..... ±25 mA
Maximum Continuous current through V_{CC} or GND ..... ±75 mA
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Maximum Electrostatic discharge (V_{ESD}) rating:
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ..... ±2000 V 3/
Charge device model (CDM) per ANSI/ESDA/JEDEC JS-002 ..... ±1000 V 4/
Thermal information:

Thermal metric 5/	Case outline X	Units
Junction to ambient thermal resistance, $R_{\theta JA}$	102.8	°C/W
Junction to case (top) thermal resistance, $R_{\theta JCtop}$	36.8	°C/W
Junction to board thermal resistance, $R_{\theta JB}$	53.8	°C/W
Junction to top characterization parameter, $R_{\Psi JT}$	2.5	°C/W
Junction to board characterization parameter, $R_{\Psi JB}$	53.3	°C/W
Junction to case (bottom) thermal resistance, $R_{\theta JCbott}$	n/a	°C/W

1.4 Recommended operating conditions. 3/

Supply voltage (V_{CC}) ..... 4.5 V to 5.5 V
Minimum High level Input voltage (V_{IH}) ..... 2.0 V
Maximum Low level input voltage (V_{IL}) ..... 0.8 V
Input voltage (V_I) ..... 0 V to 5.5 V
Output voltage (V_O) ..... 0 V to V_{CC}
Maximum High level output current (I_{OH}) ..... -8 mA
Maximum low level output current (I_{OL}) ..... 8 mA
Maximum Input Transition rise and fall rate ($\Delta t/\Delta v$) ..... 20 ns/V
Operating free-air temperature range (T_A) ..... --55°C to +125°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability, functionality, performance, and shorten the device lifetime.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
5/ For more information about traditional and new thermal metrics, see manufacturer data report.
6/ Over operating free air temperature range (unless otherwise notice). All unused inputs of the device must be held at V_{CC} or GND for proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JEDEC JS-002	–	Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal Connections. The Terminal Connections shall be as shown in figure 2.

3.5.3 Terminal Functions. The Terminal Functions shall be as shown in figure 3.

3.5.4 Truth Table. The Truth Table shall be as shown in figure 4.

3.5.4 Functional Block diagram. The Functional Block diagram shall be as shown in figure 5.

3.5.5 Load Circuit and Voltage Waveforms. The Load Circuit and Voltage Waveforms shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

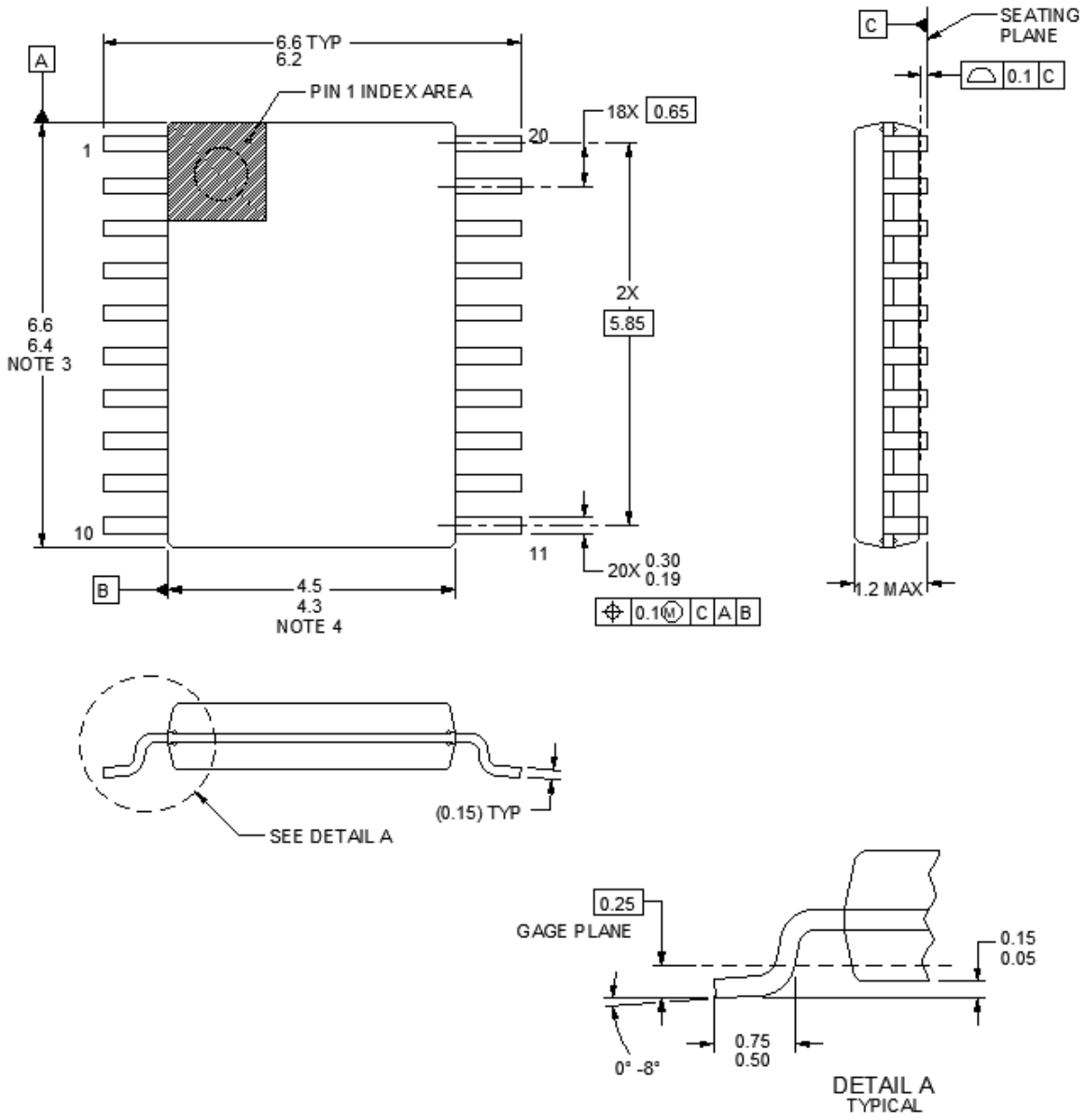
Test		Symbol	Conditions 2/	V_{CC}	Limits				Unit
					T_A = 25°C		-55° C to 125°C		
					Min	Max	Min	Max	
High level output voltage		V_{OH}	I_{OH} = -50 µA	4.5 V	4.4		4.4		V
			I_{OH} = -8 mA		3.94		3.7		
Low level output voltage		V_{OL}	I_{OL} = 50 µA			0.1		0.1	
			I_{OL} = 8 mA			0.36		0.44	
Input current	$\overline{OE}$ or DIR	I_I	V_I = 5.5 V or GND	0 to 5.5 V		±0.1		±1	µA
Three state output leakage current	A or B inputs 2/	I_{OZ}	V_O = V_{CC} or GND	5.5 V		±25		±2.5	
Quiescent supply current		I_{CC}	V_I = 5.5 V or GND I_O = 0	5.5 V		4		40	µA
Quiescent supply current delta 3/		ΔI_{CC}	One intput at 3.4 V, Other input at V_{CC} or GND			1.35		1.5	mA
Input capacitance	$\overline{OE}$ or DIR	C_I	V_I = V_{CC} or GND	5.5 V		10			pF
I/O capacitance	A or B inputs	C_{IO}	V_I = V_{CC} or GND		4 TYP				
Propagation delay									
From input A or B to B or A		t_{PLH}	C_L = 15 pF	5 V		7.7	1	10	ns
		t_{PHL}		±0.5 V		7.7	1	10	
From input $\overline{OE}$ to A or B		t_{PZH}				13.8	1	16	
		$t_{P\backslash ZL}$				13.8	1	16	
		t_{PHZ}				14.4	1	16.5	
		$t_{P\backslash LZ}$				14.4	1	16.5	
From input A or B to B or A		t_{PLH}	C_L = 50 pF			8.7	1	11	
		t_{PHL}				8.7	1	11	
From input $\overline{OE}$ to A or B		t_{PZH}				14.8	1	17	
		$t_{P\backslash ZL}$				14.8	1	17	
		t_{PHZ}				15.4	1	17.5	
		$t_{P\backslash LZ}$				15.4	1	17.5	
		$t_{sk(0)}$				1			
Noise Characteristics									
Quiet output, minimum dynamic V_{OH}			C_L = 50 pF	5 V	4 TYP				V
High level dynamic input voltage					2				
Low level dynamic input voltage						0.8			
Operating Characteristics									
Power dissipation capacitance			No load, f = 1 MHz	5 V	13 TYP				pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature ranges. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2// Over recommended operating free-air temperature range (unless otherwise noted).
3/ For I/O ports, the parameter IOZ includes the input leakage current.
4/ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or VCC.

Case X



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153

FIGURE 1. Case outline.

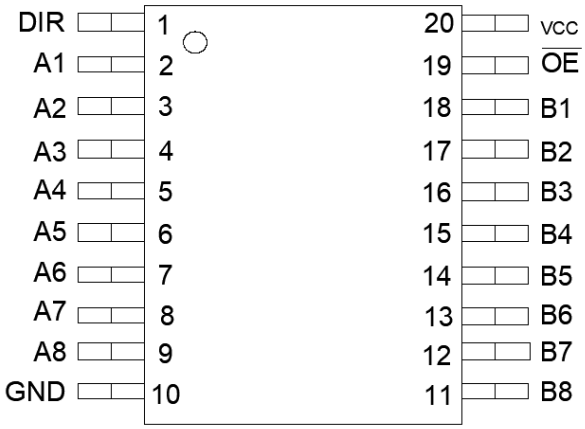


FIGURE 2. Terminal Connections.

Terminal number	Terminal symbol	Type	Description
1	DIR	I	Direction Pin
2	A1	I/O	A1 Input/Output
3	A2	I/O	A2 Input/Output
4	A3	I/O	A3 Input/Output
5	A4	I/O	A4 Input/Output
6	A5	I/O	A5 Input/Output
7	A6	I/O	A6 Input/Output
8	A7	I/O	A7 Input/Output
9	A8	I/O	A8 Input/Output
10	GND	G	Ground Pin
11	B8	I/O	B1 Input/Output
12	B7	I/O	B2 Input/Output
13	B6	I/O	B3 Input/Output
14	B5	I/O	B4 Input/Output
15	B4	I/O	B5 Input/Output
16	B3	I/O	B6 Input/Output
17	B2	I/O	B7 Input/Output
18	B1	I/O	B8 Input/Output
19	$\overline{OE}$	I	Output Enable
20	VCC	P	Power Pin

FIGURE 3. Terminal Functions.

(Each Transceiver)

Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Don't care

FIGURE 4. Truth Table.

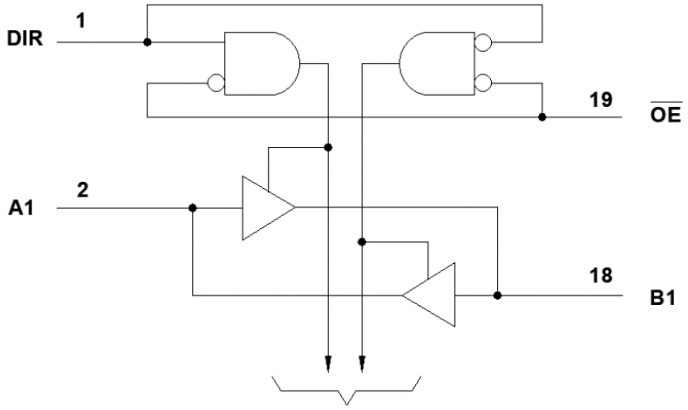
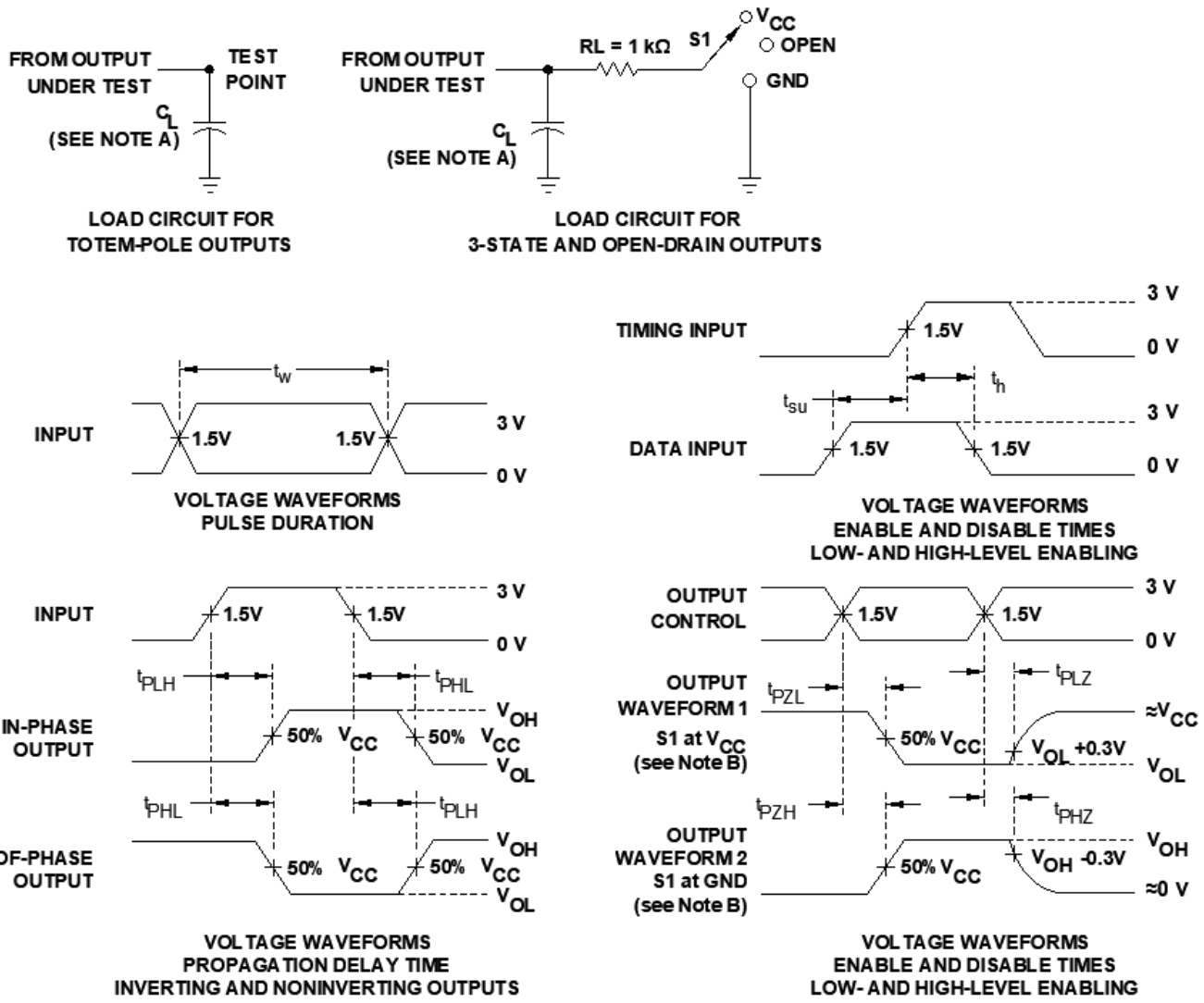


FIGURE 5. Functional Block diagram.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, tr ≤ 3 ns, t_f ≤ 3 ns .
4. The output are measured one at a time, with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 6. Load Circuit and Voltage Waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.4 Suggested source of supply. Identification of the suggested source of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/23618-01XE	01295	SN74AHCT245-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199