| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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Prepared in accordance with ASME Y14.24

Vendor Item Drawing

| Revision Status of Sheets | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | | | | | |

**PMIC N/A**

Original date of drawing

YY-MM-DD
23-09-12

**PREPARED BY**
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**CHECKED BY**
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**APPROVED BY**
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**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/landandmaritime**

**TITLE**
MICROCIRCUIT, RADIATION HARDENED, ACTIVE INPUT HIGH SPEED DIGITAL ISOLATOR, MONOLITHIC SILICON

| SIZE | CAGE CODE |
|---|---|
| A | 16236 |

**DWG NO.**
**V62/23615**

**REV**

**PAGE 1 OF 17**

AMSC N/A

5962-V124-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Radiation Hardened Active Input High Speed Digital Isolator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/23615 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | ISL71710SLHM | Radiation Hardened Active Input High Speed Digital Isolator |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | Package style |
|---|---|---|
| X | 8 | Narrow Body Small Outline Plastic Package |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range ($V_{DD1}$ to GND1) | -0.5 V to +7 V |
| Supply voltage range ($V_{DD2}$ to GND2) | -0.5 V to +7 V |
| In-Beam Supply Voltage $V_{DD1}$ to GND1 | -0.5 V to +7 V |
| In-Beam Supply Voltage $V_{DD2}$ to GND2 | -0.5 V to +7 V |
| IN Voltage | -0.5 V to $V_{DD1}$ + 0.5 V |
| $\overline{OE}$ Voltage | -0.5 V to $V_{DD2}$ + 0.5 V |
| OUT Voltage | -0.5 V to $V_{DD2}$ + 0.5 V |
| Maximum Output Current Drive | 10 mA |
| Maximum Power dissipation ($P_D$) | 675 mW |
| Maximum Junction temperature range ($T_J$) | +150°C |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Thermal resistance, Case outline X: | |
| Junction to ambient ($\theta_{JA}$) | 60°C /W 2/ |
| Junction to case (Top) ($\theta_{JC}$): | 61°C /W |
| Junction to case (Bottom) ($\theta_{JC}$): | 37°C /W 3/ |
| Characterization parameter, junction-to-top ($\psi_{JT}$) | 10°C /W |
| Electrostatic discharge (ESD) rating: | |
| Human body model (HBM) | 1.2 kV 4/ |
| Charge device model (CDM) | 1.5 kV 5/ |
| Charge device model (CDM) | |
| Field induced charged device model (FICDM) | |

1.4 Recommended operating conditions. 6/

| | |
|---|---|
| Supply voltage ($V_{DD1}$, $V_{DD2}$) | 3.0 V to 5.5 V |
| IN Logic High Voltage | 2.4 V to $V_{DD1}$ |
| IN Logic Low Voltage | 0 V to 0.8 V |
| $\overline{OE}$ Logic High Voltage | 2.4 V to $V_{DD1}$ |
| $\overline{OE}$ Logic Low Voltage | 0 V to 0.8 V |
| Maximum Input Signal Rise and Fall Time | 1 µs |
| Ambient Operating temperature ($T_A$) | -55°C to +125°C |

1.5 Radiation Features.

Maximum total dose available (low dose rate = 0.01 rad(Si)/s) ..... 75 krad(Si) 7/

Heavy ion single event phenomenon (SEP):
No single event latch-up (SEL) occurs at effective LET ( see 4.3)..... ≤ 86 MeV/(mg/cm$^2$) 8/

_____

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ $\theta_{JA}$ is measured with the component soldered to double-sided board; free air.
3/ For $\Psi_{JT}$ characterization parameter, the package top temperature is measured at the top center of the mounted package.
4/ Tested per AEC-Q100-002.
5/ Tested per AEC-Q100-011.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 75 krads(Si).
8/ Tested per JESD-57; Class 2, Level A at +125°C, for more information on SEE test, please contact manufacturer.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD78 – IC Latch-Up test

(Copies of these documents are available online at https://www.jedec.org.)

AUTOMOTIVE ELECTRONICS COUNCIL

AEC-Q11-002 - Human Body Model Electrostatic Discharge Test
AEC Q100-011 - Charged Device Model Electrostatic Discharge Test

(Copies of these documents are available online at https://www.aecouncil.org.)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.4 herein and as follows:

A. Part is not marked with the Manufacturer's name, CAGE code, or logo due to small size of package, and space limitation. This information will be maintained by the device manufacturer and included with product shipment.
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Functional block diagram. The Functional block diagram shall be as shown in figure 2.

3.5.3 Pin connections. The Pin connections shall be as shown in figure 3.

3.5.4 Pin descriptions. The Pin descriptions shall be as shown in figure 4.

3.5.5 Timing diagram. The Timing diagram shall be as shown in figure 5.

3.5.6 Input Quiescent Supply Current vs Temperature vs VDD1 Voltage. The Input Quiescent Supply Current vs Temperature vs VDD1 Voltage shall be as shown in figure 6.

3.5.7 Output Quiescent Supply Current vs Temperature vs VDD2 Voltage. The Output Quiescent Supply Current vs Temperature vs VDD2 Voltage shall be as shown in figure 7.

3.5.8 Propagation Delay (High-to-Low) vs Temperature vs VDD Voltage. The Propagation Delay (High-to-Low) vs Temperature vs VDD Voltage shall be as shown in figure 8.

3.5.9 Propagation Delay (Low-to-High) vs Temperature vs VDD Voltage. The Propagation Delay (Low-to-High) vs Temperature vs VDD Voltage shall be as shown in figure 9.

3.5.10 Output Rise Time vs Temperature vs VDD Voltage. The Output Rise Time vs Temperature vs VDD Voltage shall be as shown in figure 10.

3.5.11 Output Fall Time vs Temperature vs VDD Voltage. The Output Fall Time vs Temperature vs VDD Voltage shall be as shown in figure 11.

3.5.12 5.5V Pulse-Width Distortion vs Temperature vs VDD Voltage. The 5.5V Pulse-Width Distortion vs Temperature vs VDD Voltage shall be as shown in figure 12.

3.5.13 Dynamic Power Consumption vs Temperature. The Dynamic Power Consumption vs Temperature shall be as shown in figure 13.

3.5.14 Logic Low Output Voltage vs Temperature. The Logic Low Output Voltage vs Temperature shall be as shown in figure 14.

3.5.15 Logic High Output Voltage vs Temperature. The Logic High Output Voltage vs Temperature shall be as shown in figure 15.

3.5.16 Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature. The Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature shall be as shown in figure 16.

3.5.17 Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature. The Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature shall be as shown in figure 17.

3.5.18 Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature. The Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature shall be as shown in figure 18.

3.5.19 Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature. The Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature shall be as shown in figure 19.

3.5.20 Cross-Axis Field Direction. The Cross-Axis Field Direction shall be as shown in figure 20.

TABLE IA. Electrical performance characteristics 1/.

| Test | Symbol | Conditions 2/ | Limits 3/ | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **3.3 V Electrical Specifications** | | | | | |
| Input Quiescent Supply Current | $I_{DD1}$ | See Figure 6 | | 40 | µA |
| | | Post Radiation 75 krad(Si) | | 2.8 | mA |
| Output Quiescent Supply Current | $I_{DD2}$ | See Figure 7 | | 1.75 | mA |
| Logic Input Current | $I_I$ | | -10 | 10 | µA |
| Logic High Output Voltage | $V_{OH}$ | $I_O$ = -20 µA, $V_I$ = $V_{IH}$ See Figure 14 | $V_{DD}$ – 0.1 | | V |
| | | $I_O$ = -4 mA, $V_I$ = $V_{IH}$ | 0.8 x $V_{DD}$ | | V |
| Logic Low Output Voltage | $V_{OL}$ | $I_O$ = 20 µA, $V_I$ = $V_{IL}$ See Figure 15 | | 0.1 | V |
| | | $I_O$ = 4 mA, $V_I$ = $V_{IL}$ | | 0.8 | V |
| **Switching Specifications ($V_{DD}$ = 3.3 V)** | | | | | |
| Maximum Data Rate | | $C_L$ = 15 pF | 130 | | Mbps |
| Pulse Width 4/ | PW | 50% Points, $V_O$ | 10 | | ns |
| Propagation Delay Input to Output (High-to-Low). See Figure 8 | $t_{PHL}$ | $C_L$ = 15 pF | | 18 | ns |
| Propagation Delay Input to Output (Low-to-High). See Figure 9 | $t_{PLH}$ | $C_L$ = 15 pF | | 18 | ns |
| Propagation Delay Enable to Output (High-to-High Impedance) See Figure 16 | $t_{PHZ}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (Low-to-High Impedance) See Figure 17 | $t_{PLZ}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (High Impedance-to-High) See Figure 18 | $t_{PZH}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (High Impedance-to-Low) See Figure 19 | $t_{PZL}$ | $C_L$ = 15 pF | | 7 | ns |
| Pulse-Width Distortion 5/ See Figure 12 | PWD | $C_L$ = 15 pF | | 4 | ns |
| Pulse Jitter 6/ | $t_J$ | $C_L$ = 15 pF | 100 TYP | | ps |
| Propagation Delay Skew 7/ | $t_{PSK}$ | $C_L$ = 15 pF | | 6 | ns |
| Output Rise Time (10% to 90%) See Figure 10 | $t_R$ | $C_L$ = 15 pF | | 5 | ns |
| Output Fall Time (10% to 90%) See Figure 11 | $t_F$ | $C_L$ = 15 pF | | 5 | ns |
| Common-Mode Transient Immunity (Output Logic High or Logic Low) 8/ | $\|CH_H\|,\|CM_L\|$ | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25 ns | 30 | | kV/µs |
| Dynamic Power Consumption 9/, | | | | 240 | µA/Mbps |
| See Figure 13 | | Post Radiation 75 krad(Si) | | 450 | µA/Mbps |
| **Magnetic Field Immunity** 10/ **($V_{DD2}$ = 3 V, 3 V < $V_{DD1}$ < 5.5 V)** | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | 1000 | | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_p$ = 8 µs | 1800 | | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz – 1MHz | 1800 | | A/m |
| Cross-Axis Immunity Multiplier[9] | $K_X$ | | 2.5 TYP | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions 2/ | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **5 V Electrical Specifications** | | | | | |
| Input Quiescent Supply Current | $I_{DD1}$ | See Figure 6 | | 75 | µA |
| | | Post Radiation 75krad(Si) | | 3.4 | mA |
| Output Quiescent Supply Current | $I_{DD2}$ | See Figure 7 | | 2.5 | mA |
| Logic Input Current | $I_I$ | | -10 | 10 | µA |
| Logic High Output Voltage | $V_{OH}$ | $I_O$ = -20 µA, $V_I = V_{IH}$ See Figure 14 | $V_{DD}$ – 0.1 | | V |
| | | $I_O$ = -4 mA, $V_I = V_{IH}$ | 0.8 x $V_{DD}$ | | V |
| Logic Low Output Voltage | $V_{OL}$ | $I_O$ = 20 µA, $V_I = V_{IL}$ See Figure 15 | | 0.1 | V |
| | | $I_O$ = 4 mA, $V_I = V_{IL}$ | | 0.8 | V |
| **Switching Specifications ($V_{DD}$ = 5 V)** | | | | | |
| Maximum Data Rate | | $C_L$ = 15 pF | 130 | | Mbps |
| Pulse Width 4/ | PW | 50% Points, $V_O$ | 10 | | ns |
| Propagation Delay Input to Output (High-to-Low) See Figure 8 | $t_{PHL}$ | $C_L$ = 15 pF | | 16 | ns |
| Propagation Delay Input to Output (Low-to-High) See Figure 9 | $t_{PLH}$ | $C_L$ = 15 pF | | 16 | ns |
| Propagation Delay Enable to Output (High-to-High Impedance) See Figure 16 | $t_{PHZ}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (Low-to-High Impedance) See Figure 17 | $t_{PLZ}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (High Impedance-to-High) See Figure 18 | $t_{PZH}$ | $C_L$ = 15 pF | | 7 | ns |
| Propagation Delay Enable to Output (High Impedance-to-Low) See Figure 19 | $t_{PZL}$ | $C_L$ = 15 pF | | 7 | ns |
| Pulse-Width Distortion 5/ See Figure 18 | PWD | $C_L$ = 15 pF | | 4 | ns |
| Propagation Delay Skew 7/ | $t_{PSK}$ | $C_L$ = 15 pF | | 6 | ps |
| Output Rise Time (10% to 90%) See Figure 10 | $t_R$ | $C_L$ = 15 pF | | 4 | ns |
| Output Fall Time (10% to 90%) See Figure 11 | $t_F$ | $C_L$ = 15 pF | | 4 | ns |
| Common-Mode Transient Immunity (Output Logic High or Logic Low) 8/ | $\|CM_H\|,\|CM_L\|$ | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25 ns | 30 | | kV/µs |
| Dynamic Power Consumption 9/, | | | | 340 | µA/Mbps |
| See Figure 13 | | Post Radiation 75krad(Si) | | 530 | µA/Mbps |
| **Magnetic Field Immunity 10/ ($V_{DD2}$ = 5 V, 3 V < $V_{DD1}$ < 5.5 V)** | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | 2800 | | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_p$ = 8 µs | 4000 | | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz – 1MHz | 4000 | | A/m |
| Cross-Axis Immunity Multiplier[9] | $K_X$ | | 2.5 TYP | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature ranges. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Unless otherwise noted, VDD1 VDD2 = 3V - 5.5V; OUT and OE are open, VDD1 and VDD2 are bypassed to GND with a 47nF X7R capacitor; $T_A = T_J = +25°C$. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated.
3/ Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
4/ Minimum pulse width is the minimum value at which specified PWD is ensured.
5/ PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
6/ 66535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800ps transition time.
7/ $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ between devices at +25°C.
8/ CMH is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CML is the maximum common-mode input voltage that can be sustained while maintaining $V_O < 0.8V$. The common-mode voltage slew rate apply to both rising and falling common-mode voltage edges.
9/ Dynamic power consumption is calculated per channel and is supplied by the input side power supply of the channel.
10/ The relevant test and measurement methods are given in manufacturer data Electromagnetic Compatibility.
11/ External magnetic field immunity is improved by this factor if the field direction is end-to-end rather than pin-to-pin (See Figure 20).

TABLE IB. SEP test limits. 1/ 2/ 3/

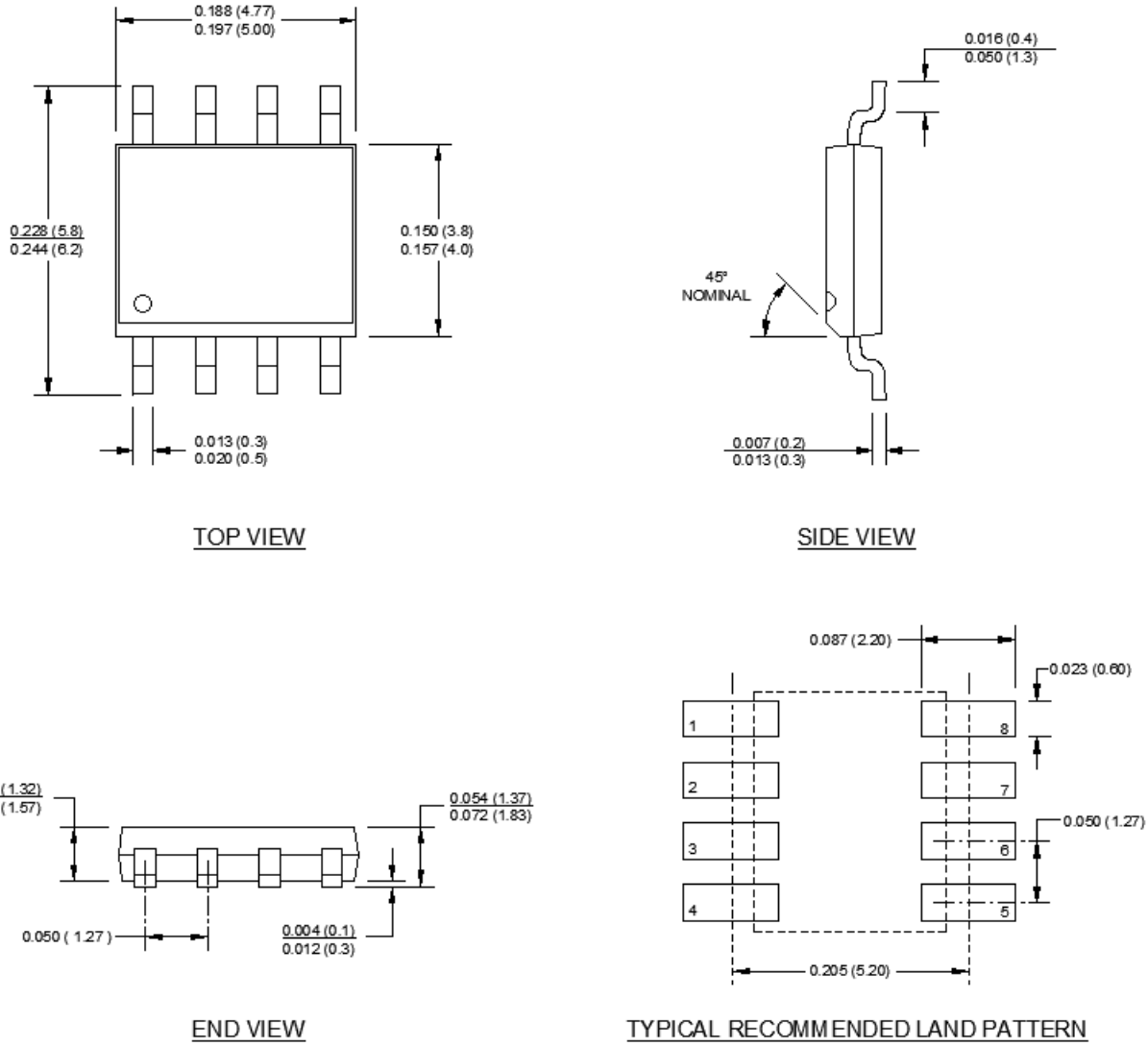
| Device type | SEP/SEE | Temperature ($T_C$) | $V_{IN}$ | Effective linear energy transfer (LET) |
|---|---|---|---|---|
| 01 | No SEL | 125°C | 6.5 V | $\leq$ 86 MeV/(mg/cm$^2$) |

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ SEE test shall be performed in accordance with JESD57. For more information on SEP test results, customers are requested to contact the manufacturer.

Case X




NOTES:
1. Dimensions are in inch (mm); Scale = approximately 5X.
2. Pin spacing is a BASIC dimension, tolerances do not accumulates

FIGURE 1. Case outline.

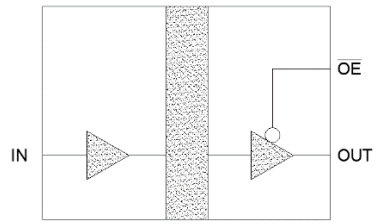



FIGURE 2. Functional Block Diagram.

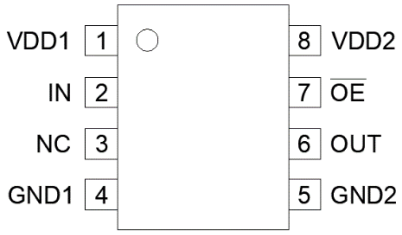
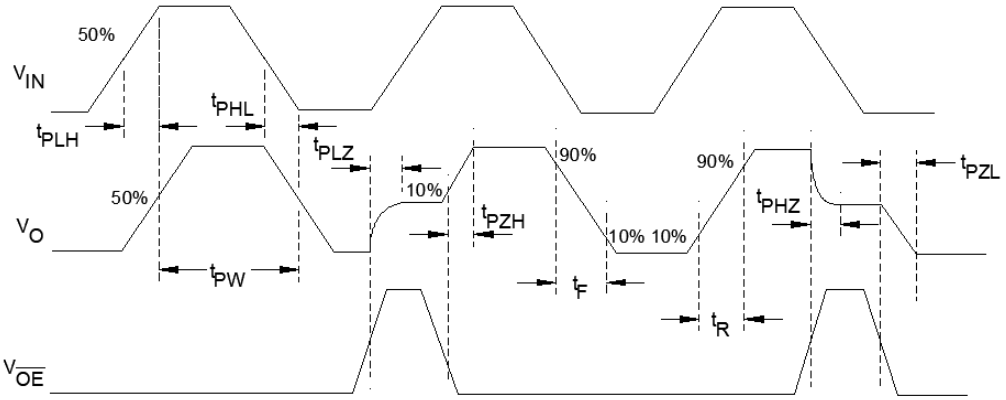



FIGURE 3. Pin Connections.

| Pin number | Pin Name | Description |
|---|---|---|
| 1 | VDD1 | Supply voltage |
| 2 | IN | Data in |
| 3 | NC | No internal connection. Leave this pin floating or connect it to VDD1 or GND1. |
| 4 | GND1 | Ground return for VDD1 |
| 5 | GND2 | Ground return for VDD2 |
| 6 | OUT | Data output |
| 7 | $\overline{\text{OE}}$ | Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected. |
| 8 | VDD2 | Supply voltage |

FIGURE 4. Pin Descriptions.




Notes:

| | |
|---|---|
| $t_{PLH}$ | Propagation Delay, Low-to-High |
| $t_{PHL}$ | Propagation Delay, High-to-Low |
| $t_{PW}$ | Minimum Pulse Width |
| $t_{PLZ}$ | Propagation Delay, Low-to-High Impedance |
| $t_{PZH}$ | Propagation Delay, High Impedance-to-High |
| $t_{PHZ}$ | Propagation Delay, High-to-High Impedance |
| $t_{PZL}$ | Propagation Delay, High Impedance-to-Low |
| $t_R$ | Rise Time |
| $t_F$ | Fall Time |

FIGURE 5. Timing Diagram.

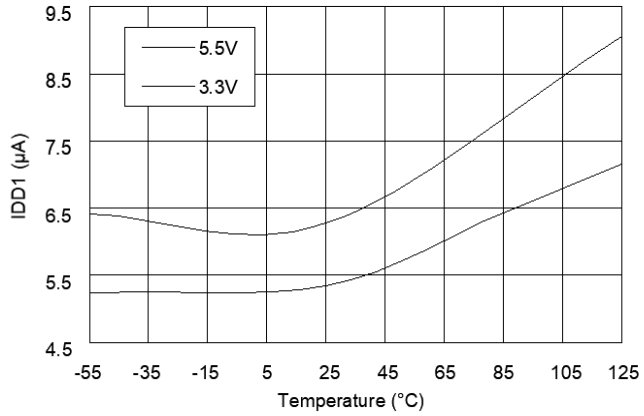



Figure 6. Input Quiescent Supply Current vs Temperature vs VDD1 Voltage

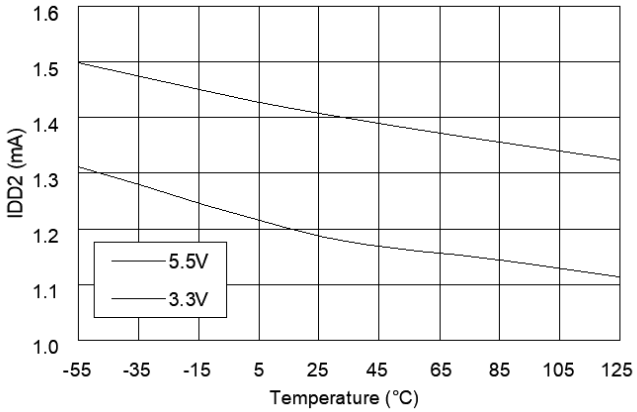



Figure 7. Output Quiescent Supply Current vs Temperature vs VDD2 Voltage

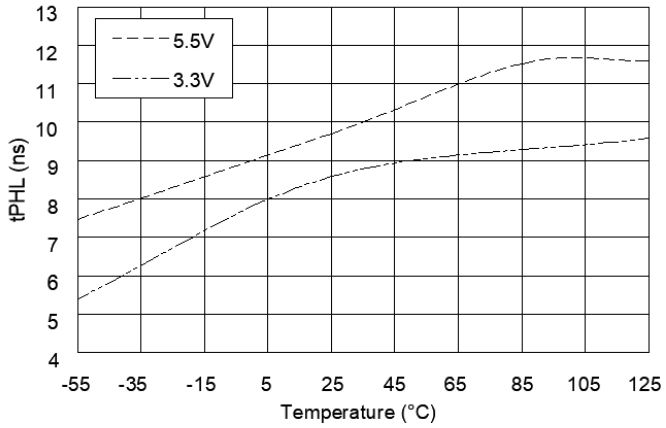



Figure 8 Propagation Delay (High-to-Low) vs Temperature vs VDD Voltage

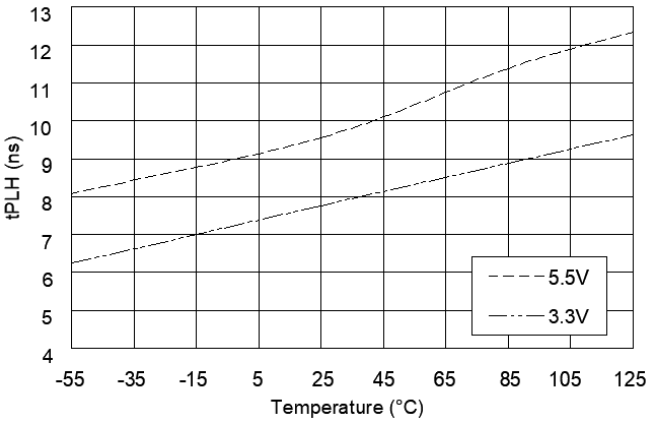



Figure 9 Propagation Delay (Low-to-High) vs) Temperature vs VDD Voltage

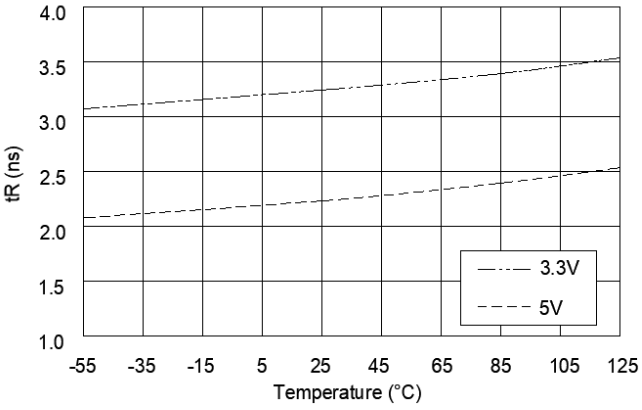



Figure 10 Output Rise Time vs Temperature vs VDD Voltage

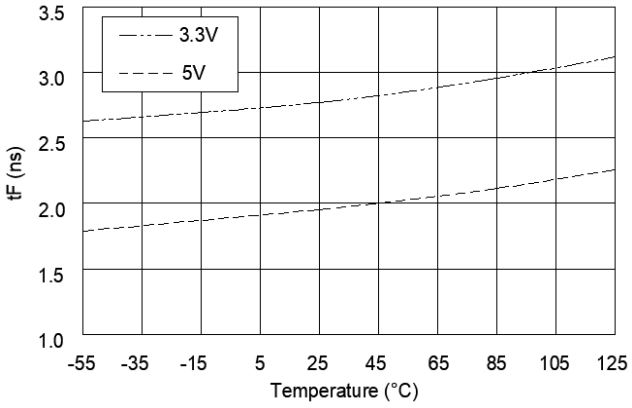



Figure 11 Output Fall Time vs Temperature vs VDD Voltage

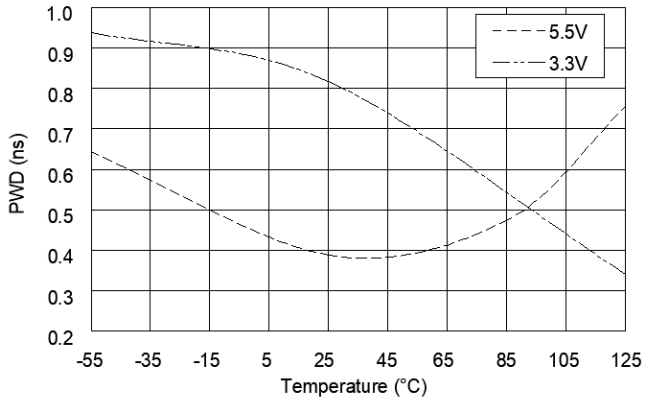



Figure 12 5.5V Pulse-Width Distortion vs Temperature vs VDD Voltage

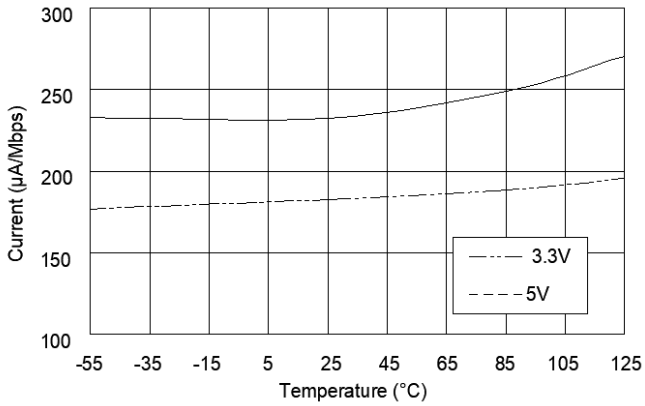



Figure 13 Dynamic Power Consumption vs Temperature

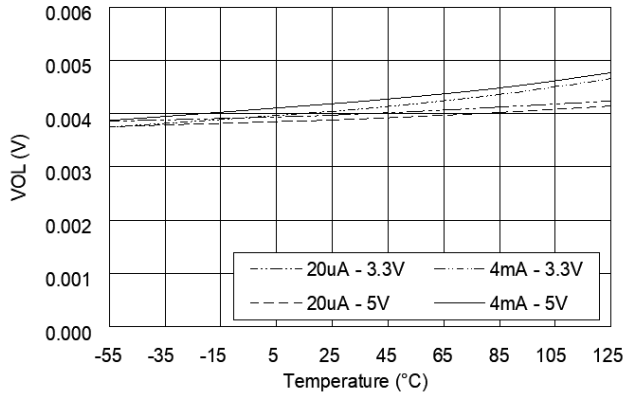



Figure 14 Logic Low Output Voltage vs Temperature

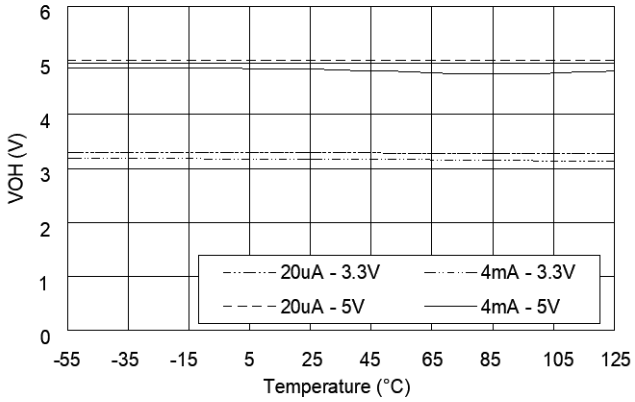



Figure 15 Logic High Output Voltage vs Temperature

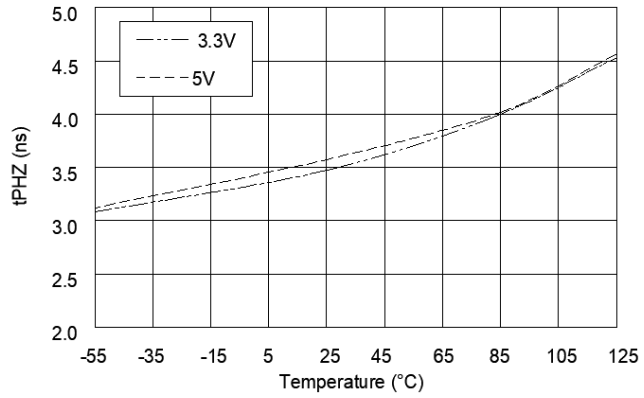



Figure 16 Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature

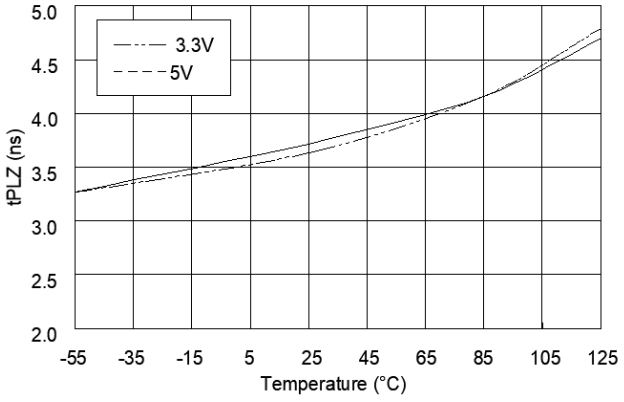



Figure 17 Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature

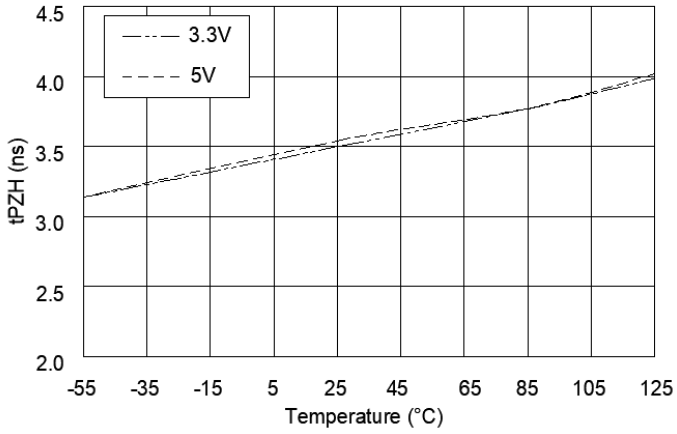



Figure 18 Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature

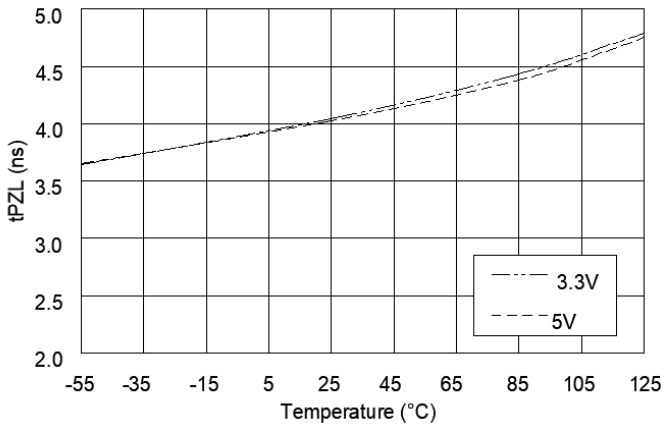



Figure 19 Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature

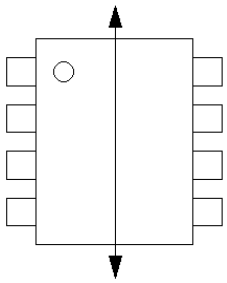


Figure 20 Cross-Axis Field Direction

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D for all device types and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/cm$^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C $\pm$10% for SEL.

f. For SEP test limits, see table IB herein.

g. For SEL test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latch-up (SEL).

6.4 Suggested source of supply. Identification of the suggested source of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Mode of transportation and quantity | Top side marking | Vendor part number |
|---|---|---|---|---|
| V62/23615-01XE | 34371 | Tray | 71710MBZ | ISL71710SLHMBZ |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 34371 | Renesas Electronics America, Inc<br>1650 Robert J. Conlan Blvd.<br>Palm Bay, FL 32905-3406 |