REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing

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TITLE

MICROCIRCUIT, LINEAR, 6 V, 4 A, STEP DOWN DC / DC CONVERTER WITH ADJUSTABLE FREQUENCY, MONOLITHIC SILICON, NEXT GENERATION ENHANCED PRODUCT (NEP)

SIZE	CAGE CODE	DWG NO.
A	**16236**	**V62/23613**

REV

AMSC N/A

5962-V124-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 6 volt, 4 amp step down direct current (DC) / DC converter with adjustable frequency microcircuit, with an operating temperature range of -55°C to +150°C. The next generation enhanced products (NEP) within this drawing contain the following: 1/

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types.

Device type	Generic	Output current	Circuit function
01	TPS62810-EP	4 amps	6 volt, 4 amp step down DC/DC converter with adjustable frequency
02	TPS62811-EP	1 amp	6 volt, 1 amp step down DC/DC converter with adjustable frequency
03	TPS62812-EP	2 amps	6 volt, 2 amp step down DC/DC converter with adjustable frequency
04	TPS62813-EP	3 amps	6 volt, 3 amp step down DC/DC converter with adjustable frequency

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	9	See figure 1	Very thin quad flat non-leaded package (VQFN)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium 2/
F	Tin-lead alloy (BGA/CGA)
S	SAC solder alloy of Sn Ag Cu
Z	Other

1/ Next Generation products contain high tin (Sn) content up to 97% and have flip chip technology with lead (Pb) free die bumps. Contact the manufacturer for details.
2/ The lead finish marking E of the NEP products is SAC solder compatible. The composition of alloy is NiPdAu.

1.3 Absolute maximum ratings. 3/

Pin voltage range: 4/	
Power supply input (VIN)	-0.3 V to 6.5 V
Switch pin of the converter (SW)	-0.3 V to V_{IN} + 0.3 V
SW (transient for less than 10 ns)	-3 V to 10 V
Voltage feedback input (FB)	-0.3 V to 4 V
Open drain power good output (PG), Soft start / Tracking (SS/TR), Device compensation and frequency set input (COMP/FSET)	-0.3 V to V_{IN} + 0.3 V
Pin voltage range: 4/	
Enable (EN), (MODE / SYNC)	-0.3 V to 6.5 V
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient ($R_{\theta JA}$)	71.1°C/W
Thermal resistance, junction to case top ($R_{\theta JC(top)}$)	37.2°C/W
Thermal resistance, junction to board ($R_{\theta JB}$)	16.4°C/W
Characterization parameter, junction to top (ψ_{JT})	0.9°C/W
Characterization parameter, junction to board (ψ_{JB})	16.1°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM), per AEC Q100-002	±2000 V 5/
Charge device model (CDM), per AEC Q100-011	±750 V

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{IN})	2.75 V to 6 V
Output voltage (V_{OUT})	0.6 V to 5.5 V
Effective inductance for a switching frequency of 1.8 MHz to 3.5 MHz (L)	0.32 µH to 0.9 µH 0.47 µH nominal
Effective inductance for a switching frequency of 3.5 MHz to 4 MHz (L)	0.25 µH to 0.9 µH 0.33 µH nominal
Effective output capacitance for 1 A and 2 A version (C_{OUT}) 7/	15 µF to 470 µF 22 µF nominal
Effective output capacitance for 3 A and 4 A version (C_{OUT}) 7/	27 µF to 470 µF 47 µF nominal
Effective input capacitance (C_{IN}) 7/	5 µF minimum 10 µF nominal
Compensation and frequency selection resistor (R_{CF})	4.5 kΩ to 100 kΩ
Junction temperature range (T_J)	-55°C to +150°C

3/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4/ While switching.

5/ AEC Q100-002 indicates that HBM stressing shall be in accordance with the JEDEC JS-001 specification.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

7/ The values given for the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Check the manufacturers DC bias curves for the effective capacitance versus DC voltage applied. Further restrictions may apply. See the feature description for COMP/FSET about the output capacitance versus compensation setting and output voltage.

2. APPLICABLE DOCUMENTS

AUTOMOTIVE ELECTRONICS COUNCIL

AEC Q100-002 – Human Body Model Electrostatic Discharge Test
AEC Q100-011 – Charged Device Model Electrostatic Discharge Test

(Copies of these documents are available from https://www.aecouncil.com.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Wire bonds. There are no wire bonds in this device, these are flip chip devices.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits Min	Limits Max	Unit
Supply							
Operating quiescent current	I_Q	EN = high, I_{OUT} = 0 mA, device not switching	+125°C	01, 02, 03, 04		21	μA
		EN = high, I_{OUT} = 0 mA, device not switching	-55°C to +150°C			30	
			+25°C		15 typical		
Shutdown current	I_{SD}	EN = 0 V	+125°C	01, 02, 03, 04		18	μA
			+150°C			26	
			+25°C		1.5 nominal		
Undervoltage lockout threshold		Rising input voltage	-55°C to +150°C	01, 02, 03, 04	2.5	2.75	V
			+25°C		2.6 typical		
		Falling input voltage	-55°C to +150°C		2.25	2.6	
			+25°C		2.5 typical		
Thermal shutdown temperature	T_{SD}	Rising junction temperature		01, 02, 03, 04	170 typical		°C
Thermal shutdown hysteresis	T_{SD}			01, 02, 03, 04	15 typical		°C
Control (EN, SS/TR, PG, MODE)							
High level input voltage for MODE pin	V_{IH}		-55°C to +150°C	01, 02, 03, 04	1.1		V
Low level input voltage for MODE pin	V_{IL}		-55°C to +150°C	01, 02, 03, 04		0.3	V
Frequency range on MODE pin for synchronization	f_{SYNC}	Requires a resistor from COMP/FSET to GND, see application section	-55°C to +150°C	01, 02, 03, 04	1.8	4	MHz
Duty cycle of synchronization signal at MODE pin			-55°C to +150°C	01, 02, 03, 04	40%	60%	
			+25°C		50% typical		
Time to lock to external frequency			+25°C	01, 02, 03, 04	50 typical		μs
Input threshold voltage for EN pin; rising edge	V_{IH}		-55°C to +150°C	01, 02, 03, 04	1.06	1.15	V
			+25°C		1.1 typical		
Input threshold voltage for EN pin; falling edge	V_{IL}		-55°C to +150°C	01, 02, 03, 04	0.96	1.05	V
			+25°C		1.0 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Control (EN, SS/TR, PG, MODE) - continued.							
Input leakage current for EN, MODE/SYNC	I_{LKG}	$V_{IH} = V_{IN}$ = or V_{IL} = GND	-55°C to +150°C	01, 02, 03, 04		150	nA
Resistance from COMP/FSET to GND for logic low		Internal frequency setting with f = 2.25 MHz	-55°C to +150°C	01, 02, 03, 04	0	2.5	kΩ
Voltage on COMP/FSET for logic high		Internal frequency setting with f = 2.25 MHz	+25°C	01, 02, 03, 04	V_{IN} typical		V
UVP power good threshold voltage; dc level	V_{TH_PG}	Rising (%/V_{FB})	-55°C to +150°C	01, 02, 03, 04	92%	98%	
			+25°C		95% typical		
		Falling (%/V_{FB})	-55°C to +150°C		87%	93%	
			+25°C		90% typical		
OVP power good threshold voltage; dc level	V_{TH_PG}	Rising (%/V_{FB})	-55C to +150°C	01, 02, 03, 04	107%	113%	
			+25°C		110% typical		
		Falling (%/V_{FB})	-55°C to +150°C		104%	111%	
			+25°C		107% typical		
Power good de-glitch time		For a high level to low level transition on power good	+25°C	01, 02, 03, 04	40 typical		μs
Power good output low voltage	V_{OL_PG}	I_{PG} = 2 mA	-55°C to +150°C	01, 02, 03, 04		0.3	V
			+25°C		0.07 typical		
Input leakage current (PG)	I_{LKG_PG}	V_{PG} = 5 V	-55°C to +150°C	01, 02, 03, 04		100	nA
SS/TR pin source current	$I_{SS/TR}$		-55°C to +150°C	01, 02, 03, 04	2.1	2.8	μA
			+25°C		2.5 typical		
Tracking gain		V_{FB} / $V_{SS/TR}$	+25°C	01, 02, 03, 04	1 typical		
Tracking offset		Feedback voltage with V_{FB} / $V_{SS/TR}$ = 0 V	+25°C	01, 02, 03, 04	17 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Power switch							
High-side MOSFET ON-resistance		$V_{IN} \geq 5$ V	-55°C to +150°C	01, 02, 03, 04		60	mΩ
			+25°C		37 typical		
Low-side MOSFET ON-resistance		$V_{IN} \geq 5$ V	-55°C to +150°C	01, 02, 03, 04		35	mΩ
			+25°C		15 typical		
High-side MOSFET leakage current		V_{IN} = 6 V, V(SW) = 0 V	-55°C to +150°C	01, 02, 03, 04		30	μA
Low-side MOSFET leakage current		V(SW) = 6 V	-55°C to +150°C	01, 02, 03, 04		55	μA
SW leakage		V(SW) = 0.6 V; current into SW pin	-55°C to +150°C	01, 02, 03, 04	-0.025	30	μA
High-side MOSFET current limit	I_{LIMH}	dc value, V_{IN} = 3 V to 6 V	-55°C to +150°C	01	4.8	6.65	A
			+25°C		5.6 typical		
			-55°C to +150°C	02	2.0	3.35	
			+25°C		2.6 typical		
			-55°C to +150°C	03	2.8	4.3	
			+25°C		3.4 typical		
			-55°C to +150°C	04	3.9	5.35	
			+25°C		4.5 typical		
Negative valley current limit	I_{LIMNEG}	dc, value	+25°C	01, 02, 03, 04	-1.8 typical		A
PWM switching frequency range	f_S		-55°C to +150°C	01, 02, 03, 04	1.8	4	MHz
			+25°C		2.25 typical		
PWM switching frequency	f_S	With COMP/FSET tied to VIN or GND	-55°C to +150°C	01, 02, 03, 04	2.025	2.475	MHz
			+25°C		2.25 typical		
PWM switching frequency tolerance		Using a resistor from COMP/FSET to GND, f_S = 1.8 MHz to 4 MHz	-55°C to +150°C	01, 02, 03, 04	-19%	18%	
Minimum on-time of HS FET	$t_{on,min}$	V_{IN} = 3.3 V	-40°C to +125°C	01, 02, 03, 04		75	ns
			+25°C		50 typical		
Minimum on-time of LS FET	$t_{on,min}$	V_{IN} = 3.3 V	+25°C	01, 02, 03, 04	30 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Output							
Feedback voltage	V_{FB}		+25°C	01, 02, 03, 04	0.6 typical		V
Input leakage current (FB)	I_{LKG_FB}	V_{FB} = 0.6 V	-55°C to +150°C	01, 02, 03, 04		70	nA
			+25°C		1 typical		
Feedback voltage accuracy	V_{FB}	$V_{IN} \geq V_{OUT}$ + 1 V, PWM mode	-55°C to +150°C	01, 02, 03, 04	-1%	1%	
		$V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.5 V, PFM mode; Co,eff ≥ 22 µF, L = 0.47 µH			-1%	2%	
		1 V ≤ V_{OUT} ≤ 1.5 V, PFM mode; Co,eff ≥ 47 µF, L = 0.47 µH			-1%	2.5%	
Feedback voltage accuracy with voltage tracking	V_{FB}	$V_{IN} \geq V_{OUT}$ + 1 V, $V_{SS/TR}$ = 0.3 V, PWM mode	-55°C to +150°C	01, 02, 03, 04	-1%	7%	
Load regulation		PWM mode operation	+25°C	01, 02, 03, 04	0.05 typical		% / A
Line regulation		PWM mode operation, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V	+25°C	01, 02, 03, 04	0.02 typical		% / V
Output discharge resistance			-55°C to +150°C	01, 02, 03, 04		50	Ω
Start up delay time	t_{delay}	I_{OUT} = 0 mA, time from EN = high to start switching; V_{IN} applied already	-55°C to +150°C	01, 02, 03, 04	135	650	µs
			+25°C		250 typical		
Ramp time; SS/TR pin open	t_{ramp}	I_{OUT} = 0 mA, time from first switching pulse until 95% of nominal output voltage; device not in current limit	-55°C to +150°C	01, 02, 03, 04	100	200	µs
			+25°C		150 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, operating junction temperature (T_J = -55°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C.

Case X

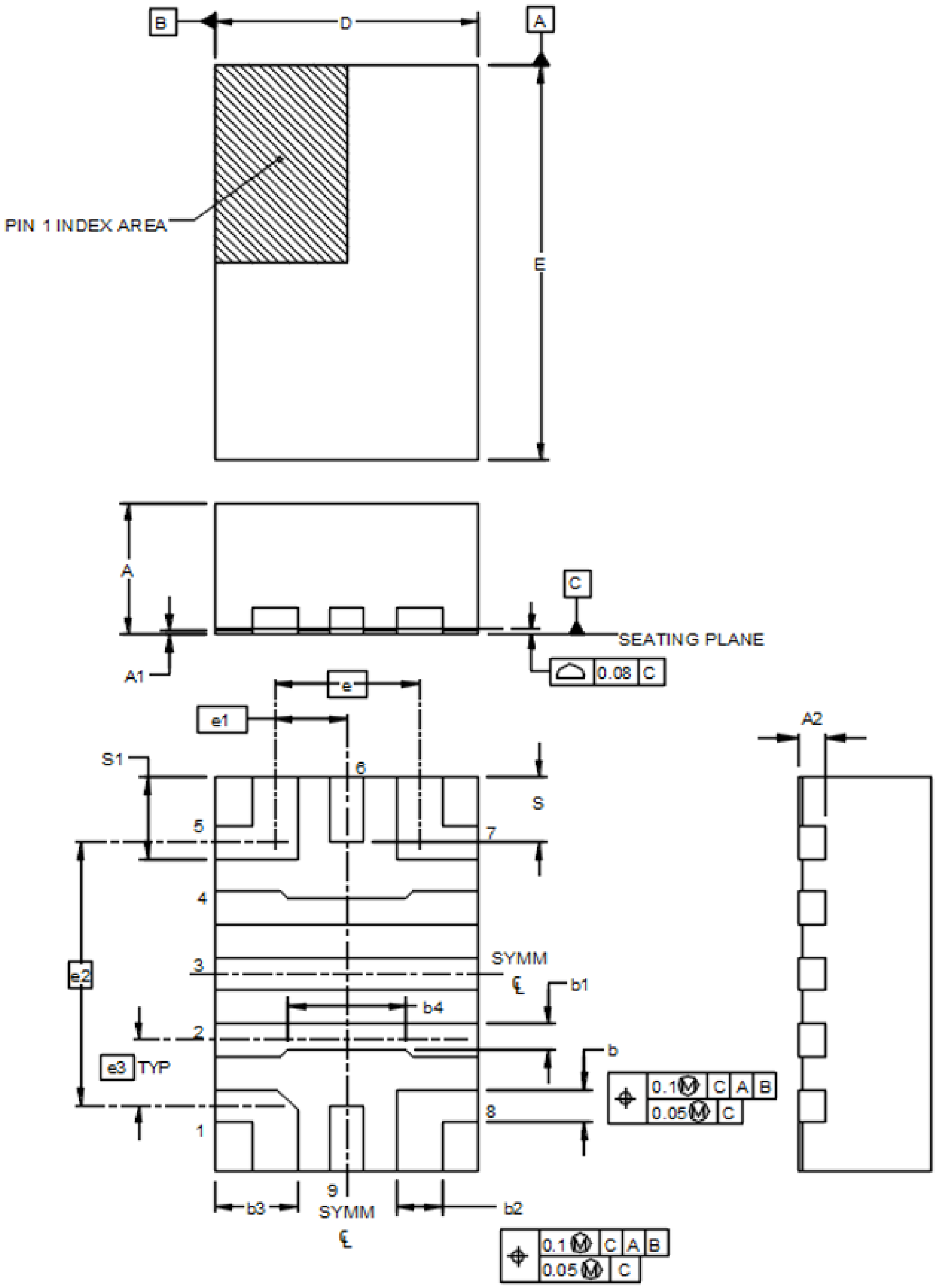

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.031	.039	0.8	1.0
A1	.000	.002	0.00	0.05
A2	OPTION 1	.004 TYP	OPTION 1	0.1 TYP
A2	OPTION 2	.008 TYP	OPTION 2	0.2 TYP
b	.008	.012	0.2	0.3
b1	.006	.010	0.15	0.25
b2	.012	.016	0.3	0.4
b3	.023	.026	0.575	0.675
b4	.035 REF		0.9 REF	
D	.075	.083	1.9	2.1
E	.114	.122	2.9	3.1
e	.043 BSC		1.1 BSC	
e1	.022 BSC		0.55 BSC	
e2	.078 BSC		2 BSC	
e3	.020 TYP		0.5 TYP	
S	.018	.022	0.45	0.55
S1	.023	.026	0.575	0.675

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The lead finish marking E of the NEP products is SAC solder compatible. The composition of alloy is NiPdAu.
3. This package is designed to be soldered to thermal pads on the board.
4. Dimension A2 has two different measurement options for the side wall metal thickness.

FIGURE 1. Case outline - Continued.

TOP VIEW

BOTTOM VIEW

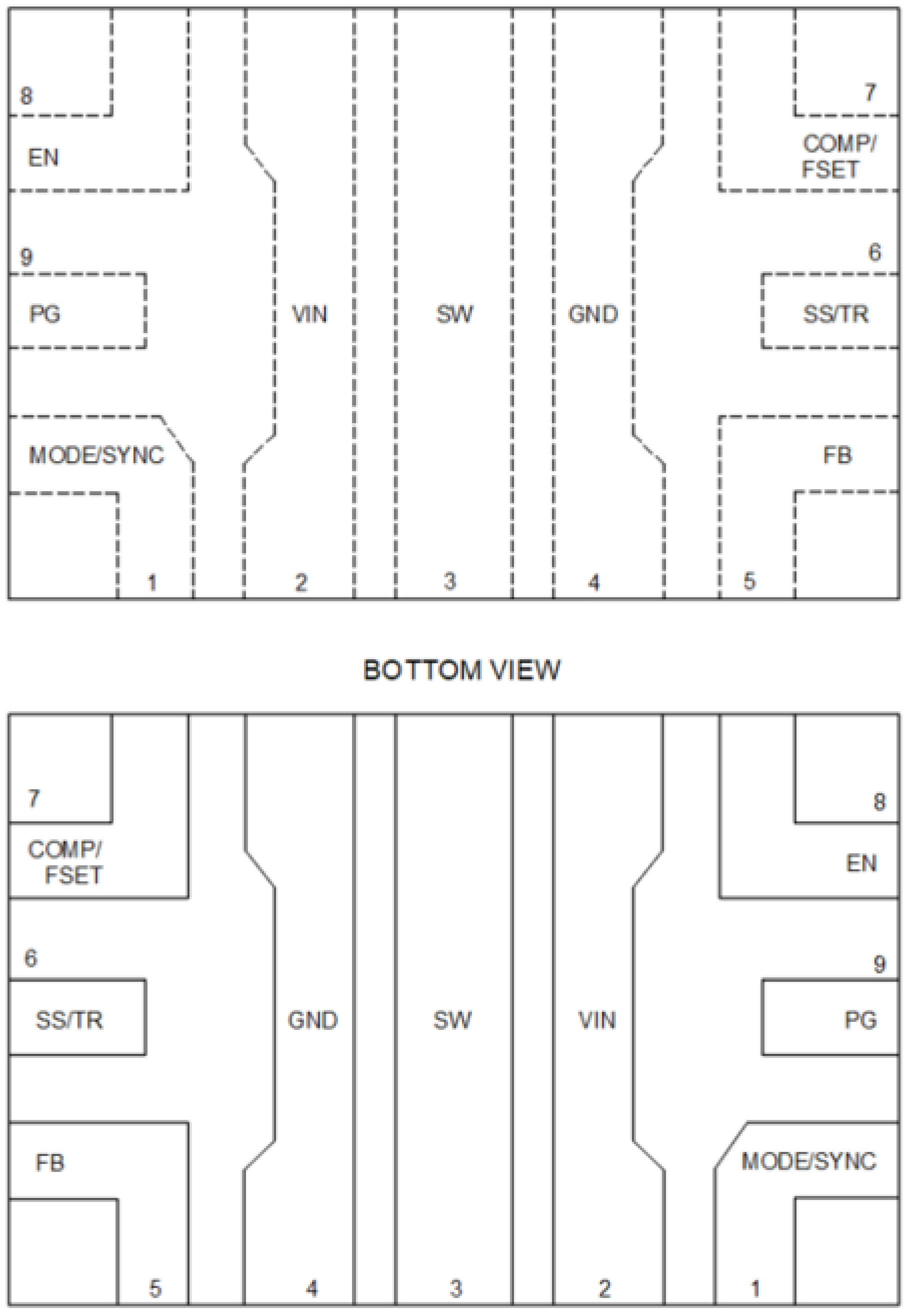

FIGURE 2. Terminal connections.

Device types	01, 02, 03, 04		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	MODE/SYNC	I	The device runs in either pulse frequency modulation (PFM) or in pulse width modulation (PWM) mode depending on the load current when this pin is pulled low. If the pin is pulled high, the device runs in forced PWM mode regardless of the load current. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See manufacturer's datasheet for the detailed specification of the digital signal applied to this pin for external synchronization.
2	VIN	---	Power supply input. Connect the input capacitor as close as possible between the VIN pin and GND.
3	SW	---	Switch pin of the converter.
4	GND	---	Ground pin.
5	FB	I	Voltage feedback input. Connect the resistive output voltage divider to this pin. For the fixed voltage versions, connect the FB pin directly to the output voltage.
6	SS/TR	I	Soft Start / Tracking pin. A capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing; see manufacturer's datasheet.
7	COMP/FSET	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. If the pin is tied to GND or VIN, the switching frequency is set to 2.25 MHz. Do not leave this pin unconnected.
8	EN	I	This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
9	PG	O	Open-drain power-good output. Low impedance when not "power good", high impedance when "power good". This pin can be left open or be tied to GND when not used.

FIGURE 2. Terminal connections - Continued.

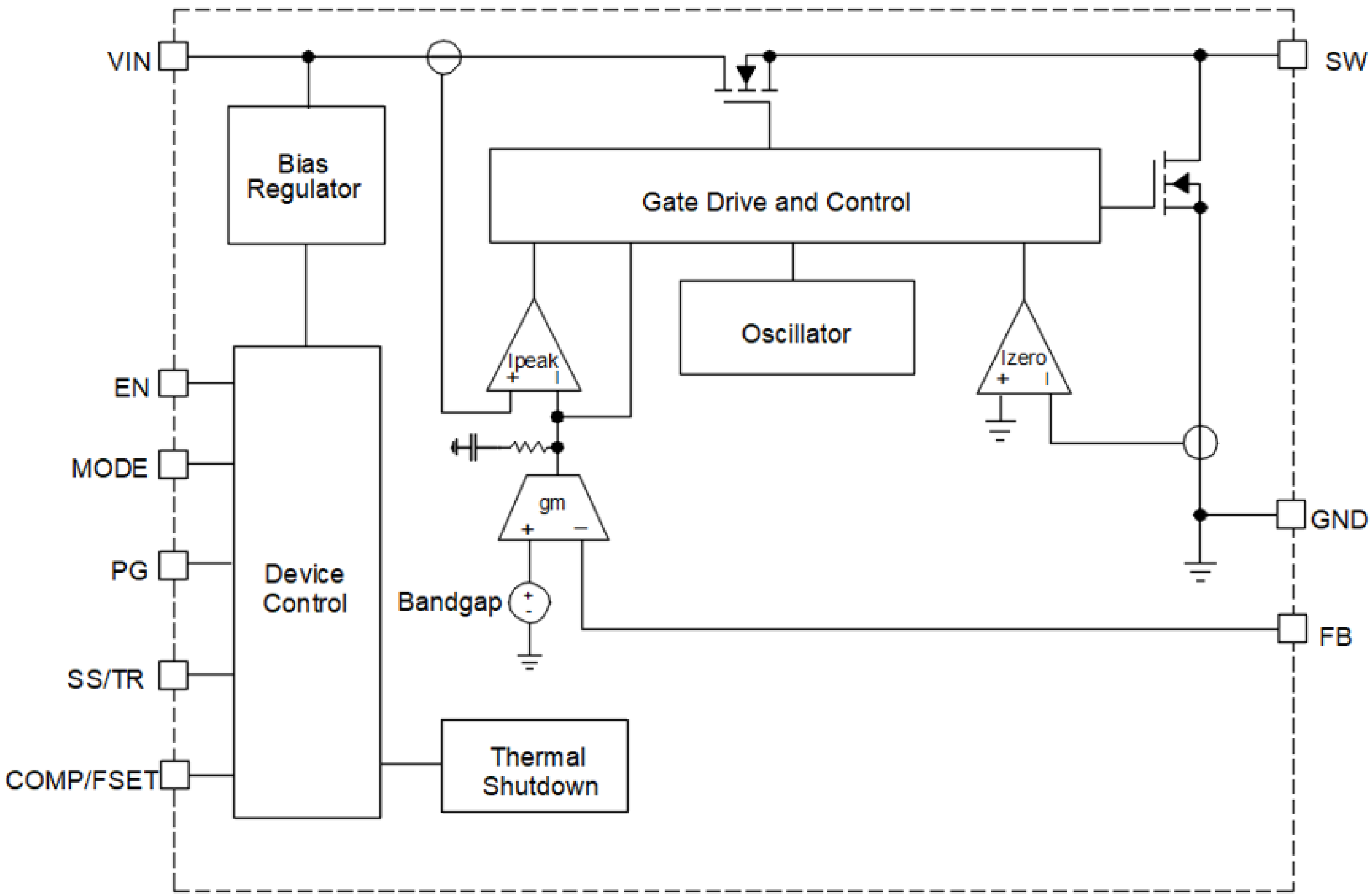

FIGURE 3. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/23613-01XE	01295	Small reel, 250 units	10EP	TPS62810MRWYRNEP
V62/23613-02XE	01295	Small reel, 250 units	11EP	TPS62811MRWYRNEP
V62/23613-03XE	01295	Small reel, 250 units	12EP	TPS62812MRWYRNEP
V62/23613-04XE	01295	Small reel, 250 units	13EP	TPS62813MRWYRNEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The lead finish marking E of the NEP products is SAC solder compatible.
The composition of alloy is Ni Pd Au.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated 12500 TI Blvd. Dallas, TX 75243