REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

Original date of drawing

YY-MM-DD

24-02-27

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TITLE
MICROCIRCUIT, LINEAR, BiCMOS, RADIATION-TOLERANT 14 V, 3.5 A CONTINUOUS SWITCH CURRENT eFUSE, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. **V62/23609**

REV

PAGE 1 OF 19

AMSC N/A

5962-V106-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance radiation-tolerant 14 V, 3.5 A maximum continuous switch current eFuse microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23609	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H2211-SEP	Radiation hardness assurance (RHA) 3.5 A maximum continuous switch current eFuse

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	See figure 1	TSSOP – Thin Shrink Small Outline Package with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Input voltage pins range (VIN) ..... -0.5 V to 16 V
Output voltage pins range (VOUT) ..... -0.5 V to 16 V
Soft start pin range (SS) ..... -0.3 V to 16 V
Enable and over voltage protection pins range (EN, OVP) ..... -0.3 V to 7.5 V
Maximum continuous switch current (I_{IN}, I_{OUT}) ..... 5.4 A
Maximum pulsed switch current (t≤5µs) (I_{IN_PLS}, I_{OUT_PLS}) ..... 30 A
Junction temperature range (T_J) ..... -55°C to 150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM), per ANSI/ESDA/JEDEC JS-001, all pins ..... ±2000 V 3/
Charge device model (CDM) per ANSI/ESDA/JEDEC JS-002, all pins ..... ±500 V 4/

1.4 Recommended operating conditions.

Input voltage pins range (VIN) ..... 4.5 V to 14 V
Output voltage pins range (VOUT) ..... 0.0 V to 14.0 V 5/
Enable and overvoltage pins range (EN, OVP) ..... 0.0 V to 7.0 V
Maximum input voltage slew rate (VIN_{SR}) ..... 0.015 V/µs
Maximum continuous switch current (I_{IN}, I_{OUT}) ..... 3.5 A
Operating junction temperature range (T_J) ..... -55°C to +125°C 6/

Thermal characteristics: 7/

Package Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	$R_{\theta JA}$	23.5	°C/W
Thermal resistance, junction-to-case (top)	$R_{\theta JC(top)}$	11.2	°C/W
Thermal resistance, junction-to-board	$R_{\theta JB}$	5.4	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.1	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	5.4	°C/W
Thermal resistance, junction-to-case (bottom)	$R_{\theta JC(bot)}$	0.5	°C/W

1/ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Over operating free-air temperature range (unless otherwise noted); all voltages referenced to GND.
3/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
4/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.
5/ This maximum VOUT voltage is only applicable when the device is disabled (EN = Low). When the device is enabled (EN = High), the maximum VOUT voltage is the input voltage, VIN.
6/ In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.
7/ For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

1.5 Radiation Features.

Maximum total ionizing dose (TID) available (dose rate = 50 – 300 rad(Si)/s).....	50 krads(Si) 8/
Heavy ion single event phenomenon (SEP):	
No SEL occurs at effective linear energy transfer (LET) (see 4.3).....	≤ 48 MeV·cm^2/mg 9/
No SEB observe at effective LET (see 4.3)	≤ 48 MeV·cm^2/mg 9/
No SEGR observe at effective LET (see 4.3)	≤ 48 MeV·cm^2/mg 9/

8/ Device type 01 supplied to this drawing have been tested total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krads(Si) as specified herein. For more information on TID test report, please contact the manufacturer.

9/ Heavy ion single event effects (SEE) test was performed using the 15-A MeV cocktail and K500 beam line at TAMU Cyclotron Institute Radiation Effects Facility. No single event latch-up (SEL) was occurred under Ag ions at Vmax supply voltage and operating temperature 125°C corresponding to an effective LET of 48 Mev-cm^2/mg. For more information on SEE/SEP test please contact device manufacturer.

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS
MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels
JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components

(Copies of these documents are available online at https://www.jedec.org.)

ASTM INTERNATIONAL (ASTM)
ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org/.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Reverse current protection enter (V_{RCP_ENTER}) test waveforms. The reverse current protection enter (VRCP_ENTER) test waveforms shall be as shown in figure 4.

3.5.5 Reverse current protection exit (V_{RCP_EXIT}) test waveforms. The reverse current protection exit (VRCP_EXIT) test waveforms shall be as shown in figure 5.

3.5.6 EN signal low time to restart device (t_{LOW_OFF}). The EN signal low time to restart device (t_{LOW_OFF}) shall be as shown in figure 6.

3.5.7 Turn-on time (tON), turn-off time (tOFF), and VOUT fall time (tF) waveforms. The turn-on time (tON), turn-off time (tOFF), and VOUT fall time (tF) waveforms shall be as shown in figure 7.

3.5.8 OVP assert (tASSERT) and OVP deassert (tDEASSERT) waveforms. The OVP assert (tASSERT) and OVP deassert (tDEASSERT) waveforms shall be as shown in figure 8.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Power supplies and currents								
Internal VIN UVLO rising	VIN_{UVLOR}			1, 2, 3	All	3.2	3.8	V
Internal VIN UVLO falling	VIN_{UVLOF}			1, 2, 3	All	2.6	3.2	V
Internal VIN UVLO hysteresis	$HYST_{VIN-UVLO}$			1, 2, 3	All		0.75	V
Quiescent current	I_Q	I_{OUT} = 0 mA, EN = 7 V		1, 2, 3			10	mA
VIN to VOUT forward leakage current	I_F	EN = 0 V, VOUT = 0 V, measured VOUT current	VIN = 14 V	1, 2, 3	All		1.3	mA
			VIN = 12 V				0.94	
			VIN = 9 V				0.49	
			VIN = 4.5 V				0.23	
VIN off-state supply current	I_{SD} VIN	EN = 0 V, VOUT = 0 V, measured VIN current	VIN = 14 V	1, 2, 3	All		10	mA
			VIN = 12 V				9.5	
			VIN = 9 V				8	
			VIN = 4.5 V				7	
Reverse current protection enter voltage 3/	V_{RCP_ENTER}	EN = 7 V, see Figure 4	VIN = 4.5 V	1	All	390 typical		mV
			VIN = 14 V			363 typical		
Reverse current protection exit voltage 3/	V_{RCP_EXIT}	EN = 7 V, see Figure 5	VIN = 4.5 V	1	All	264 typical		mV
			VIN = 14 V			249 typical		
Reverse current protection response time 3/	t_{RCP}	EN = 7 V, see Figure 4	VIN = 4.5 V	9	All	208 typical		µs
			VIN = 14 V			247 typical		
Reverse current protection leakage current	I_{RCP}	EN = 0 V, VOUT = 0 V to 14 V, and VOUT > VIN		1, 2, 3	All		250	µA
		EN = 7 V, VIN = 0 V, VOUT = 0 V to 14 V					240	
Soft start								
Soft start charge current	I_{SS}			1, 2, 3			83	µA
Enable (EN) input								
EN threshold voltage, rising	V_{IHEN}			1, 2, 3	All	0.59	0.67	V
EN threshold voltage, falling	V_{ILEN}			1, 2, 3	All	0.49	0.55	V
EN hysteresis voltage	$HYST_{EN}$			1, 2, 3	All	95	116	mV
VIN percentage for enable 4/	VIN_{EN}			1, 2, 3	All	75		%
EN pin input leakage current	I_{EN}	EN = 7 V, VIN = 14 V		1, 2, 3	All		12	nA
EN signal low time during cycling	t_{LOW_OFF}	VOUT falls to < 90%, see Figure 6		9, 10, 11	All	47		µs
Overvoltage protection (OVP)								
OVP pin input leakage current	I_{OVP}	OVP = 7 V		1, 2, 3	All		12	nA
OVP threshold voltage, rising	V_{OVPR}			1, 2, 3	All	1.07	1.22	V
OVP threshold voltage, falling	V_{OVPF}			1, 2, 3	All	1.04	1.19	V
OVP hysteresis voltage	$HYST_{OVP}$	4.6 V < VIN < 14 V		1, 2, 3	All	24	33	mV

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Current limit								
Internal current limit trip point	I_{L_trip}	VIN = 12 V, C_{SS} = 2 nF		1	01	8 typical		A
Fast trip off current limit peak	I_{L_peak}	VIN = 12 V, 10 Ω to 10 mΩ short in 1 µs, switch inductance = 270 nH		1	01	25 typical		A
Fast trip off response time	t_{ftr}			9	01	2.3 typical		µs
Fast trip off off-time	t_{fto}	VIN = 12 V, C_{SS} = 2 nF		9	01	51 typical		µs
Thermal shutdown								
Thermal shutdown					01	155 typical		°C
Thermal shutdown hysteresis					01	20 typical		°C
Resistance characteristics								
On-state resistance, lead length ≈ 2.5 mm	R_{ON}	VIN = 14 V, I_{OUT} = 3.5 A	-55°C	3	01		37	mΩ
			-40°C			37.5 typical		
			25°C	1			46	
			85°C			53.7 typical		
			125°C	2			60	
		VIN = 12 V, I_{OUT} = 3.5 A	-55°C	3	01		37	mΩ
			-40°C			37.3 typical		
			25°C	1			46	
			85°C			53.4 typical		
			125°C	2			59	
		VIN = 9 V, I_{OUT} = 3.5 A	-55°C	3	01		36	mΩ
			-40°C			37 typical		
			25°C	1			45	
			85°C			53 typical		
			125°C	2			58	
		VIN = 6 V, I_{OUT} = 3.5 A	-55°C	3	01		36	mΩ
			-40°C			37 typical		
			25°C	1			45	
			85°C			53 typical		
			125°C	2			58	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Resistance characteristics - continued								
On-state resistance, lead length ≈ 2.5 mm	R_{ON}	VIN = 4.5 V, I_{OUT} = 3.5 A	-55°C	3	01		39	mΩ
			-40°C			40 typical		
			25°C	1			49	
			85°C			58 typical		
			125°C	2			63	
Switching characteristics: VIN = 5 V								
Turn-on time	t_{ON}	R_{LOAD} = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF See Figure 7		9	All	107 typical		µs
Turn-off time	t_{OFF}				All	56 typical		µs
VOUT fall time	t_F				All	167 typical		µs
OVP assert time	t_{ASSERT}	R_{LOAD} = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF See Figure 8		9	All	8 typical		µs
OVP deassert time	$t_{DEASSERT}$				All	41 typical		µs
Switching characteristics: VIN = 12 V								
Turn-on time	t_{ON}	R_{LOAD} = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF See Figure 7		9	All	220 typical		µs
Turn-off time	t_{OFF}				All	41 typical		µs
VOUT fall time	t_F				All	139 typical		µs
OVP assert time	t_{ASSERT}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF See Figure 8		9	All	6 typical		µs
OVP deassert time	$t_{DEASSERT}$				All	63 typical		µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating ambient temperature range T_A = -55°C to 125°C, VIN = 4.5 V to 14 V, C_{OUT} = 10 µF, and all voltages referenced to GND (unless otherwise noted); includes group E radiation testing at TA = 25°C for RHA devices.

3/ This parameter is not referenced to GND; it is referenced from VOUT to VIN.

4/ VIN must be ≥ 75 % of its final value before EN is asserted only if VIN_{SR} > $VOUT_{SR}$.

5/ This parameter is not referenced to GND; it is referenced from VOUT to VIN.

Table IB. SEP test limit. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (TC)	VIN	Effective linear energy transfer (LET)
01	No SEL	125°C	14 V	LET_{eff} ≤ 48 MeV·cm^2/mg
01	No SEB/SEGR	25°C	14 V	LET_{eff} ≤ 48 MeV·cm^2/mg

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Heavy ion single event effects (SEE) test was performed at TAMU Cyclotron Institute Radiation Effects Facility in accordance with ASTM F1192 or JESD57. No single event latch-up (SEL), single event burn-out (SEB) and single event gate rupture (SEGR) were observed under ^{109}Ag ions at Vmax supply voltage (14.0 V), flux of 10^5 ions/cm^2·s, fluences of 10^7 ions/cm^2 corresponding to an effective LET of 48 Mev·cm^2/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

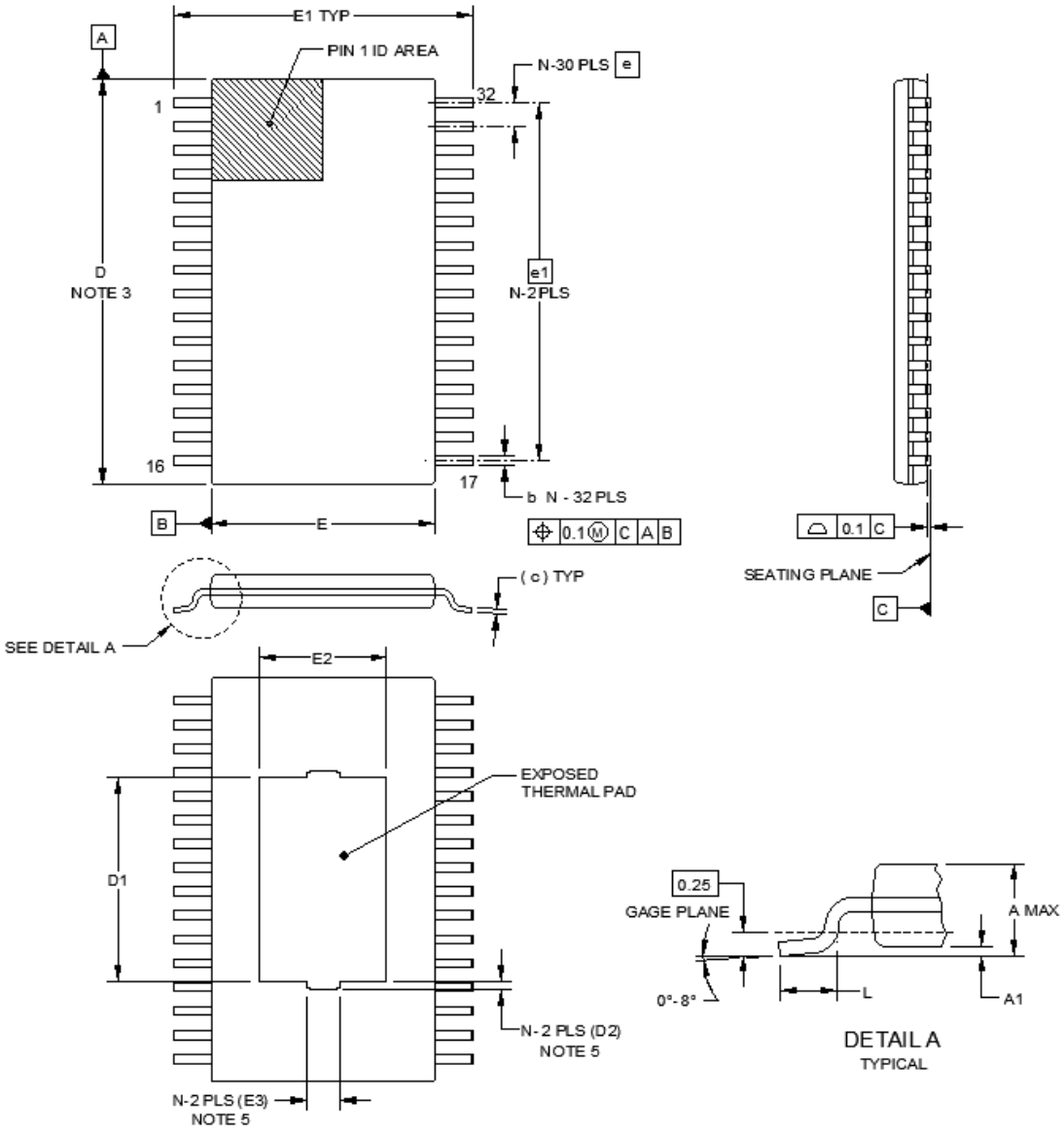

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/23609
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Dimensions				
Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A		1.20		0.0472
A1	0.05	0.15	0.0020	0.0059
b	0.19	0.30	0.0075	0.0118
c	0.15 TYP		0.0059 TYP	
D	10.90	11.10	0.4291	0.4370
D1	5.10	6.00	0.2008	0.2362
D2	0.2 TYP		0.0079 TYP	
E	7.90	8.30	0.3110	0.3268
E1	6.00	6.20	0.2362	0.2441
E2	3.00	3.90	0.1181	0.1535
E3	0.90 TYP		0.0354 TYP	
e	0.65 BSC		0.0256 BSC	
e1	9.75 BSC		0.3839 BSC	
L	0.50	0.75	0.0197	0.0295

NOTES:
1. All linear dimensions are in millimeters, inch dimensions are given for reference only. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

FIGURE 1. Case outline - Continued.

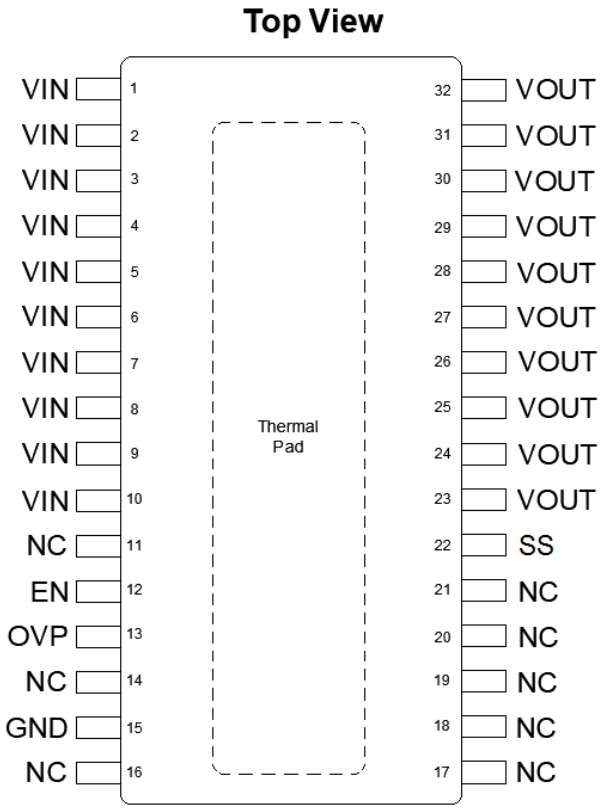


FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	**Terminal symbol**	**I/O 1/**	**Description**
1-10	VIN	I	Switch input. An input bypass capacitor recommended for minimizing V_{IN} dip.
11	NC	–	NC – No connect. These pins are not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
12	EN	I	Active high switch control input. Do not float this pin.
13	OVP	I	Overvoltage protection. Set using an external resistor divider. If no OVP is desired, connect this pin to GND. Do not float this pin.
14	NC	I	NC – No connect. These pins are not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
15	GND	–	Device ground. 2/
16-21	NC	–	NC – No connect. These pins are not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
22	SS	I/O	Soft start (switch slew rate control). If this functionality is not desired, the SS pin must be left disconnected (floating).
23-32	VOUT	O	Switch output. A minimum 10-µF output capacitor is recommended.
	Thermal pad	–	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND
	Metal Lid	–	The lid is internally connected to the thermal pad and GND through the seal ring.

1/ I = Input, O = Output, I/O = Input or Output, – = Other
2/ Thermal pad is internally connected to the seal ring.

FIGURE 2. Terminal connections – Continued.

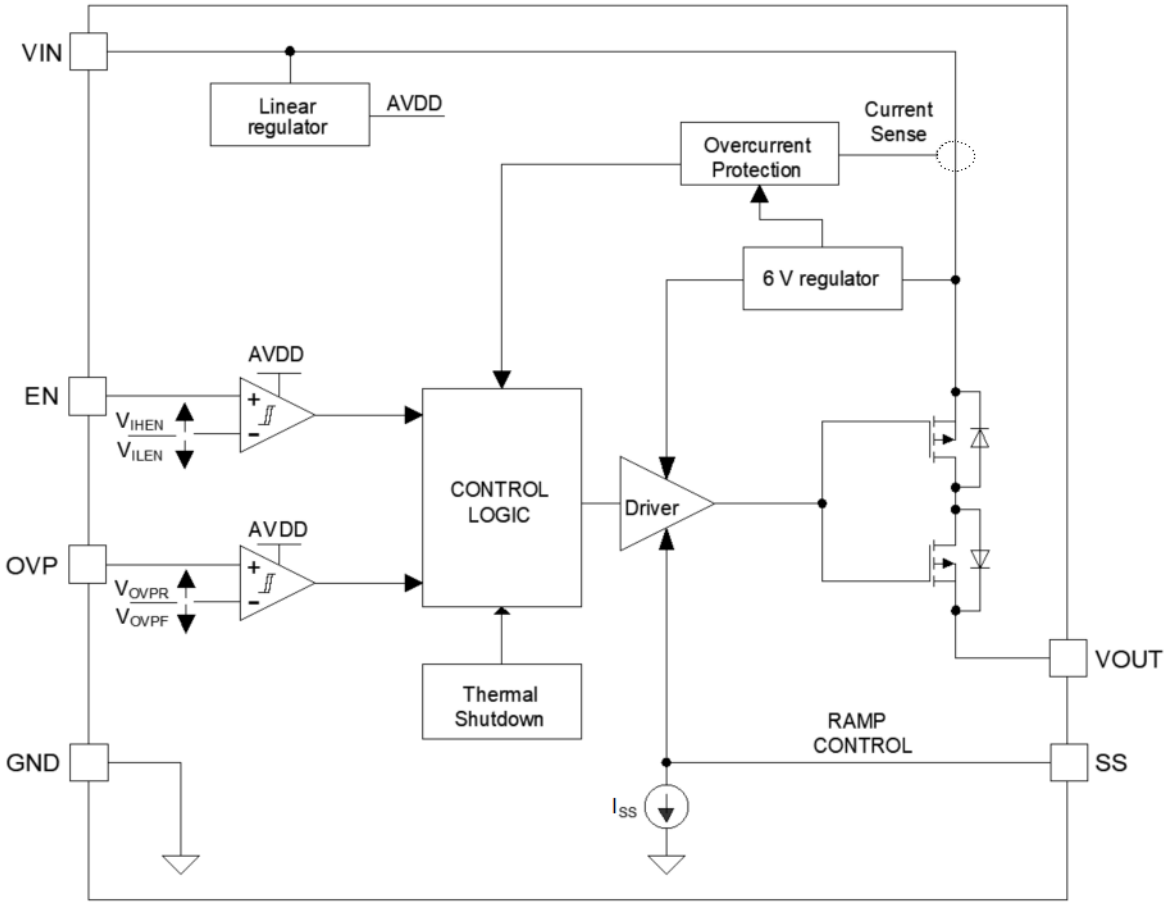
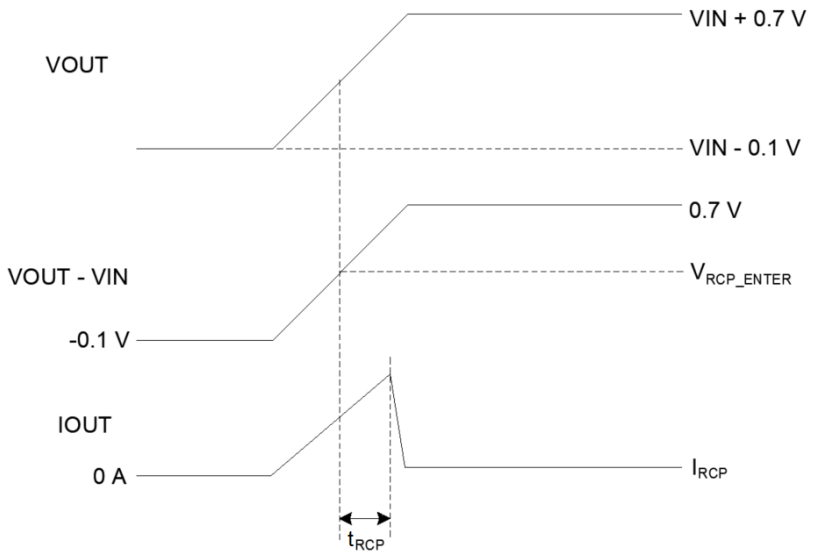
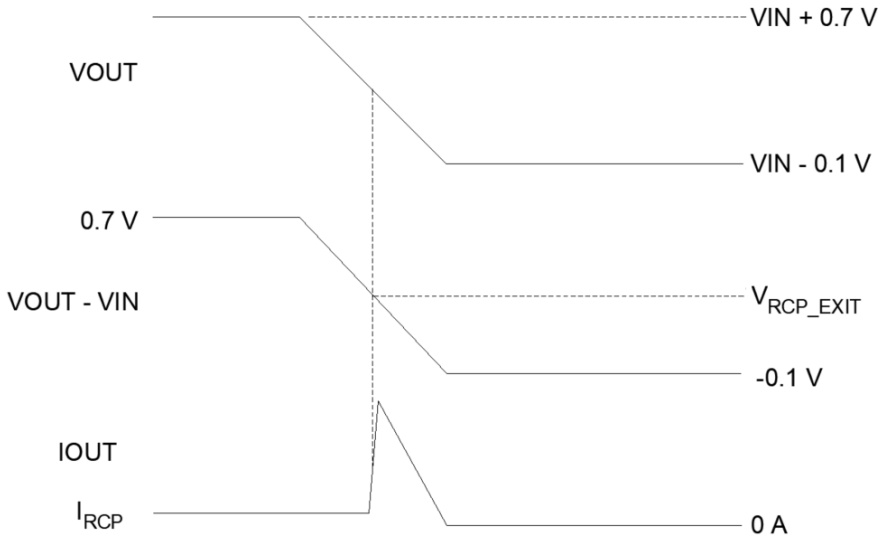


FIGURE 3. Functional block diagram.



NOTES:
1. VIN is held constant during the test.
2. VRCP_ENTER is referenced from VOUT to VIN. It is the threshold that, when reached, will turn-off the main switch FETs to prevent reverse current flow.

FIGURE 4. Reverse current protection enter (V_{RCP_ENTER}) test waveforms.



NOTES:
1. VIN is held constant during the test.
2. VRCP_EXIT is referenced from VOUT to VIN. It is the threshold that, when reached, will turn-off the reverse current protection feature.

FIGURE 5. Reverse current protection exit (V_{RCP_EXIT}) test waveforms.

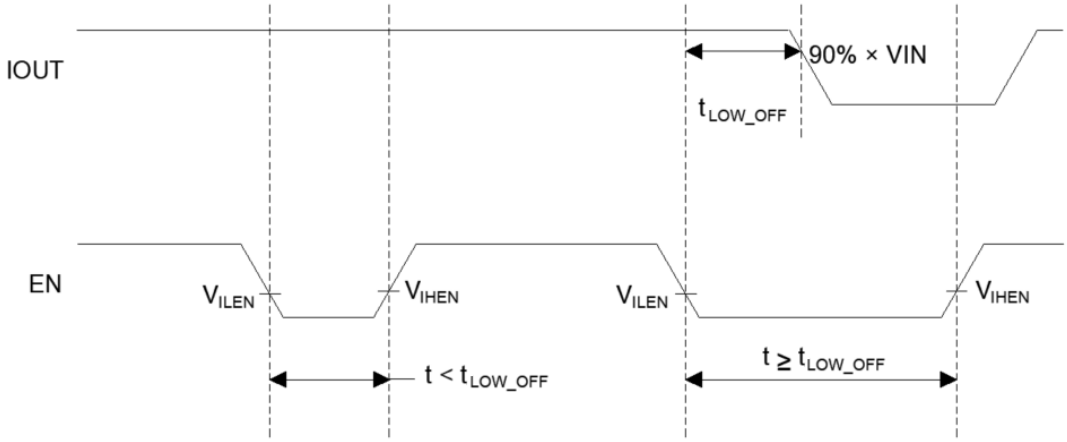


FIGURE 6. EN signal low time to restart device (t_{LOW_OFF}).

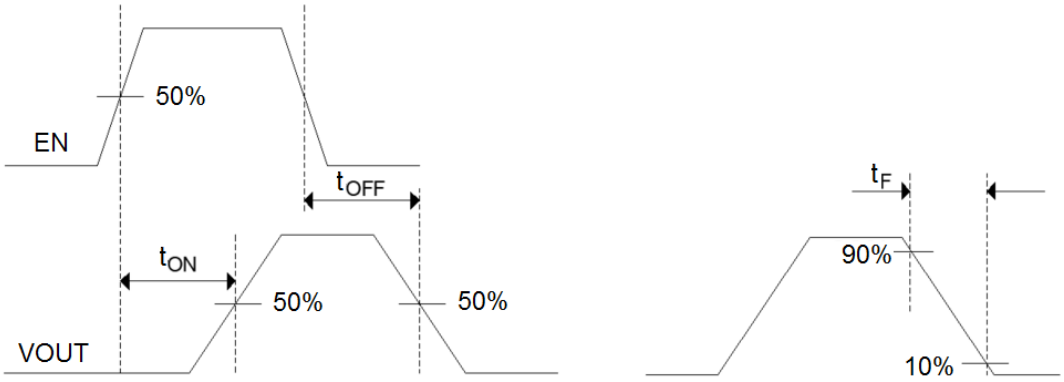
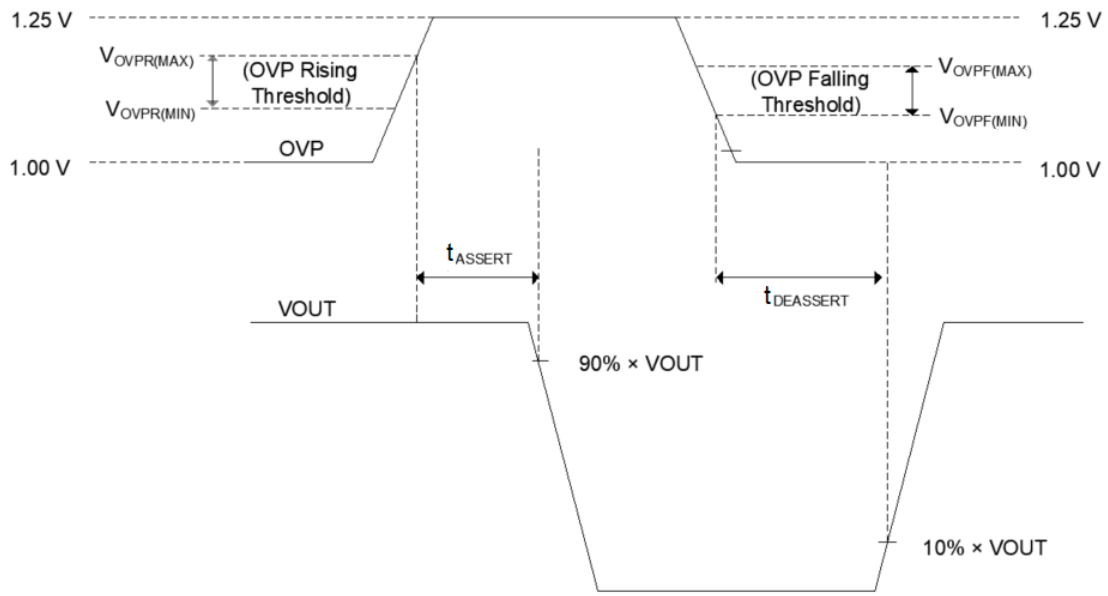


FIGURE 7. Turn-on time (t_{ON}), turn-off time (t_{OFF}), and VOUT fall time (T_F) waveforms.



NOTE:
1. The OVP test signal uses a typical rise time and fall time of 30 ns.

FIGURE 8. OVP assert (t_{ASSERT}) and OVP deassert ($t_{DEASSERT}$) waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition E for device type 01 and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0°≤angle≤60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ± 10% for SEL.

f. For SEP test limits, see table IB

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Manufacturers performed devices electrostatic discharge sensitive rate with Human body model (HDM) and classified as ESDS class 1 minimum 2000 V and also performed ESDS rate with Charge device model (CDM) and classified as ESDS is 250 V.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/23609-01XE	01295	Small tape and reel, 250 units	TPS7H2211	TPS7H2211MDAPTSEP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ This device has been marked RHA TID level 50 krads(Si) with L level (see paragraph 1.5 herein).

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243