REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

Original date of drawing

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TITLE
MICROCIRCUIT, LINEAR, BiCMOS, RADIATION-TOLERANT 1.5 V TO 7 V, 6 A CONTINUOUS SWITCH CURRENT eFUSE, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. **V62/23608**

REV

PAGE 1 OF 20

AMSC N/A

5962-V105-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance radiation-tolerant 1.5 V to 7 V, 6 A maximum continuous switch current eFuse microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23608	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H2201-SEP	Radiation hardness assurance (RHA) 6 A maximum continuous switch current eFuse

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	See figure 1	TSSOP – Thin Shrink Small Outline Package with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Input voltage range (VIN) ..... -0.3 V to 7.5 V
Output voltage range (VOUT) ..... -0.3 V to 7.5 V
Enable and over voltage protection pins (EN, OVP) ..... -0.3 V to 7.5 V
Current sense, current limit timer, retry timer, current limit and
soft start pins (CS, ILTIMER, RTIMER, IL, SS) ..... -0.3 V to VIN + 0.3 V
Maximum continuous switch current (I_{MAX}) ..... 9.0 A
Maximum pulsed switch current (t≤5µs) (I_{PLS}) ..... 45 A
Maximum junction temperature range (T_J) ..... -55°C to 150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM), per ANSI/ESDA/JEDEC JS-001, all pins ..... ±4000 V 3/
Charge device model (CDM) per JEDEC JESD22-C101, all pins ..... ±750 V 4/

1.4 Recommended operating conditions.

Input voltage range (VIN) ..... 1.5 V to 7.0 V
Maximum input voltage slew rate (SR_{VIN}) ..... 0.01 V/µs
Output voltage range (VOUT) ..... 0.0 V to 7.0 V 5/
Maximum continuous switch current (I_{MAX}) ..... 6.0 A
Operating junction temperature range (T_J) ..... -55°C to +125°C 6/

Thermal characteristics: 7/

Package Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	$R_{\theta JA}$	23.5	°C/W
Thermal resistance, junction-to-case (top)	$R_{\theta JC(top)}$	11.2	°C/W
Thermal resistance, junction-to-board	$R_{\theta JB}$	5.4	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.1	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	5.4	°C/W
Thermal resistance, junction-to-case (bottom)	$R_{\theta JC(bot)}$	0.5	°C/W

1/ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to network ground pin.
3/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
4/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.
5/ This maximum V_{OUT} voltage is only applicable when the device is disabled (EN = Low). When the device is enabled (EN = High), the maximum VOUT voltage is the input voltage, VIN.
6/ In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.
7/ For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

1.5 Radiation Features.

Maximum total ionizing dose (TID) available (dose rate = 50 – 300 rad(Si)/s)	50 krads(Si) 8/
Heavy ion single event phenomenon (SEP):	
No SEL occurs at effective linear energy transfer (LET) (see 4.3)	≤ 48 MeV·cm^2/mg 9/
No SEB observe at effective LET (see 4.3)	≤ 48 MeV·cm^2/mg 9/
No SEGR observe at effective LET (see 4.3)	≤ 48 MeV·cm^2/mg 9/

8/ Device type 01 supplied to this drawing have been tested total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krads(Si) as specified herein. For more information on TID test report, please contact the manufacturer.

9/ Heavy ion single event effects (SEE) test was performed using the 15-A MeV cocktail and K500 beam line at TAMU Cyclotron Institute Radiation Effects Facility. No single event latch-up (SEL) was occurred under Ag ions at Vmax supply voltage and operating temperature 125°C corresponding to an effective LET of 48 Mev-cm^2/mg. For more information on SEE/SEP test please contact device manufacturer.

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS
MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels
JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components

(Copies of these documents are available online at https://www.jedec.org.)

ASTM INTERNATIONAL (ASTM)
ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org/.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 EN signal low time to restart device diagram. The EN signal low time to restart device diagram shall be as shown in figure 4.

3.5.5 Turn-on (t_{ON}), turn-off (t_{OFF}) and VOUT fall time (t_F) waveforms diagram. The turn-on (t_{ON}), turn-off (t_{OFF}) and VOUT fall time (t_F) waveforms diagram shall be as shown in figure 5.

3.5.6 OVP assert (t_{ASSERT}) and OVP deassert ($t_{DEASSERT}$) waveforms diagram. The OVP assert (t_{ASSERT}) and OVP deassert ($t_{DEASSERT}$) waveforms diagram shall be as shown in figure 6.

3.5.7 t_{CSEN} waveforms diagram. The t_{CSEN} waveforms diagram shall be as shown in figure 7.

3.5.8 Internal ILTIMER waveforms diagram. The internal ILTIMER waveforms diagram shall be as shown in figure 8.

3.5.9 VOUT current to CS change delay time diagram. The VOUT current to CS change delay time diagram shall be as shown in figure 9.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Power supplies and currents								
Internal VIN UVLO voltage, rising	VIN_{HUVLO}				01	1.32 typical		V
Internal VIN UVLO voltage, falling	VIN_{LUVLO}				01	1.23 typical		V
Internal VIN UVLO hysteresis	$HYST_{VIN-UVLO}$				01	92 typical		mV
Quiescent current	I_Q	I_{OUT} = 0 mA, V_{IN} = EN = 5 V, CS resistor of 20 kΩ to GND		1, 2, 3	01		6.5	mA
VIN to VOUT forward leakage current	I_F	EN = VOUT = GND, measured V_{OUT} current	1.5 V≤ VIN ≤ 7 V	1, 2, 3	01		250	µA
			VIN = 1.5 V			3.27 typical		
			VIN = 1.8 V			3.35 typical		
			VIN = 3.3 V			3.62 typical		
			VIN = 5.0 V			4.11 typical		
			VIN = 7.0 V			6.82 typical		
VIN off-state supply current	I_{SD} VIN	EN = GND, IOUT = 0 mA, measured VIN current	VIN = 5.0 V	1, 2, 3	01		3	mA
			VIN = 3.3 V				3	
			VIN = 1.8 V				3	
			After TID = 100 krads, VIN = 1.8 V, 3.3 V, and 5 V	1			3.1	
Reverse current protection leakage current	I_{RCP}	EN = 0 V, VIN = 0 V to 7 V, VOUT = 0 V to 7 V for VOUT > VIN		1, 2, 3	01		2.5	mA
		EN = 7 V, VIN = 0 V, VOUT = 0 V to 7 V						
Soft start								
Soft start charge current	I_{SS}	1 V on SS pin		1, 2, 3	01		83	µA
Soft start slew rate	SR_{SS}	SS pin floating, COUT = 10 µF			01	295 typical		mV/µs

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Enable and undervoltage lockout (EN/UVLO) input								
EN/UVLO threshold voltage, rising	V_{IHEN}			1, 2, 3	01	0.56	0.65	V
EN/UVLO threshold, voltage, falling	V_{ILEN}			1, 2, 3	01	0.47	0.55	V
EN/ULVO hysteresis voltage	$HYST_{EN}$			1, 2, 3	01		124	mV
EN signal low time during cycling	t_{LOW}	RTIMER = GND, IL = 1 A, I_{VOUT} = 2 A	See Figure 6	9, 10, 11	01	20		µs
VIN percentage for enable 3/	VIN_{EN}			4, 5, 6	01	75		%
EN pin input leakage current	I_{EN}	EN = VIN = 5 V		1, 2, 3	01		12	nA
Overvoltage protection (OVP)								
OVPR threshold voltage, rising	V_{OVPR}			1, 2, 3	01	0.52	0.63	V
OVPF threshold voltage, falling	V_{OVPF}			1, 2, 3	01	0.50	0.59	V
OVP hysteresis voltage	$HYST_{OVP}$	1.6 V < VIN < 7 V		1, 2, 3	01		55	mV
OVP pin input leakage current	I_{OVP}			1, 2, 3	01		15	nA
Current limit and current sense								
Time for valid CS output after enable	t_{CSEN}	C_{SS} = 120 nF		9, 10, 11	01		5	ms
Minimum VOUT current for valid CS output				1, 2, 3	01	750		mA
VOUT current change to CS change delay time		0.5-A rising step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V		9, 10, 11	01		74	µs
VOUT current change to CS change delay time		0.5-A falling step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V		9, 10, 11	01		73	µs
CS pin accuracy		0.75 A ≤ I_{VOUT} ≤ 7.5 A		4, 5, 6	01	-10	10	%
CS pin voltage		0.75 A ≤ I_{VOUT} ≤ 7.5 A, no OCP		1, 2, 3	01		VIN – 0.4	V
Current limit setting	I_{IL}	I_{VOUT} ≤ 1 A		1, 2, 3	01	I_{VOUT} + 0.5		A
		1 A < I_{VOUT} ≤ 3 A				I_{VOUT} + 1		
		I_{VOUT} > 3 A				I_{VOUT} + 1.5		
Programmable current limit accuracy		1.5 V ≤ VIN ≤ 7 V		4, 5, 6	01	-20	20	%
Fast trip off current limit		VIN = 5 V, 10 mΩ short in 10 µs			01	22 typical		A

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Timers								
ILTIMER charge current	$I_{ILTIMER}$			1, 2, 3	01	0.7	1.38	µA
ILTIMER internal pull-down resistance	$PD_{ILTIMER}$	40 mV on ILTIMER pin		1, 2, 3	01		153	Ω
RTIMER charge current	I_{RTIMER}			1, 2, 3	01	0.7	1.38	µA
RTIMER internal pull-down resistance	PD_{RTIMER}	40 mV on RTIMER pin		1, 2, 3	01		153	Ω
Thermal shutdown								
Thermal shutdown		VIN = 5 V			01	175 typical		°C
Thermal shutdown hysteresis		VIN = 5 V			01	20 typical		°C
Current limit and current sense								
Fast trip off off-time		VIN = 5 V, C_{SS} = 2.7 nF		9, 10, 11	01	61 typical		µs
Internal current limit timer (fast trip off current limit)		VIN = 5 V, IVOUT = 3 A, IL = 6 A, ILTIMER = VIN, 10-mΩ short in 10 µs		9, 10, 11		15 typical		
Resistance characteristics								
ON-state resistance, lead length = 2.5 mm	R_{ON}	VIN = 7 V, I_{IL} = 7.5 A	-55°C	1, 2, 3	01		17	mΩ
			-40°C			16.9 typical		
			25°C				21	
			85°C			22.9 typical		
			125°C				27	
		VIN = 5 V, I_{IL} = 7.5 A	-55°C	1, 2, 3	01		18	
			-40°C			18 typical		
			25°C				23	
			85°C			24.8 typical		
			125°C				29	
		VIN = 3.3 V, I_{IL} = 7.5 A	-55°C	1, 2, 3	01		21	
			-40°C			20.4 typical		
			25°C				26	
			85°C			28.5 typical		
			125°C				33	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		Subgroup	Device type	Limits		Unit
						Min	Max	
Resistance characteristics - Continued								
ON-state resistance, lead length = 2.5 mm		VIN = 1.8 V, I_{IL} = 7.5 A	-55°C	1, 2, 3	01		29	mΩ
			-40°C			28.7 typical		
			25°C				37	
			85°C			41 typical		
			125°C				48	
		VIN = 1.5 V, I_{IL} = 7.5 A	-55°C	1, 2, 3	01		36	
			-40°C			35 typical		
			25°C				46	
			85°C			46.2 typical		
			125°C				59	
Switching characteristics: VIN = EN = 5 V, T_A = 25°C (unless otherwise noted)								
Turn-on time	t_{ON}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	208 typical		µs
Turn-off time	t_{OFF}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	60 typical		µs
VOUT fall time	t_F	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	90 typical		µs
OVP assert time	t_{ASSERT}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	4.5 typical		µs
OVP deassert time	$t_{DEASSERT}$	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	9.6 typical		µs
Switching characteristics: VIN = EN = 1.5 V, TA = 25°C (unless otherwise noted)								
Turn-on time	t_{ON}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	173 typical		µs
Turn-off time	t_{OFF}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	64 typical		µs
VOUT fall time	t_F	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	70 typical		µs
OVP assert time	t_{ASSERT}	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	2.65 typical		µs
OVP deassert time	$t_{DEASSERT}$	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9, 10,11	01	6.56 typical		µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over operating free-air temperature range (unless otherwise noted).
3/ VIN must be ≥ 75 % of its final value before EN is asserted only if VIN_{SR} > $VOUT_{SR}$.

Table IB. SEP test limit. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (TC)	VIN	Effective linear energy transfer (LET)
01	No SEL	125°C	7 V	$LET_{eff} \leq 48$ MeV·cm^2/mg
	No SEB/SEGR	25°C	7 V	$LET_{eff} \leq 48$ MeV·cm^2/mg

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Heavy ion single event effects (SEE) test was performed at TAMU Cyclotron Institute Radiation Effects Facility in accordance with ASTM F1192 or JESD57. No single event latch-up (SEL), single event burn-out (SEB) and single event gate rupture (SEGR) were observed under ^{109}Ag ions at Vmax supply voltage (7.0 V), flux of 10^5 ions/cm^2·s, fluences of 10^7 ions/cm^2 corresponding to an effective LET of 48 Mev·cm^2/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

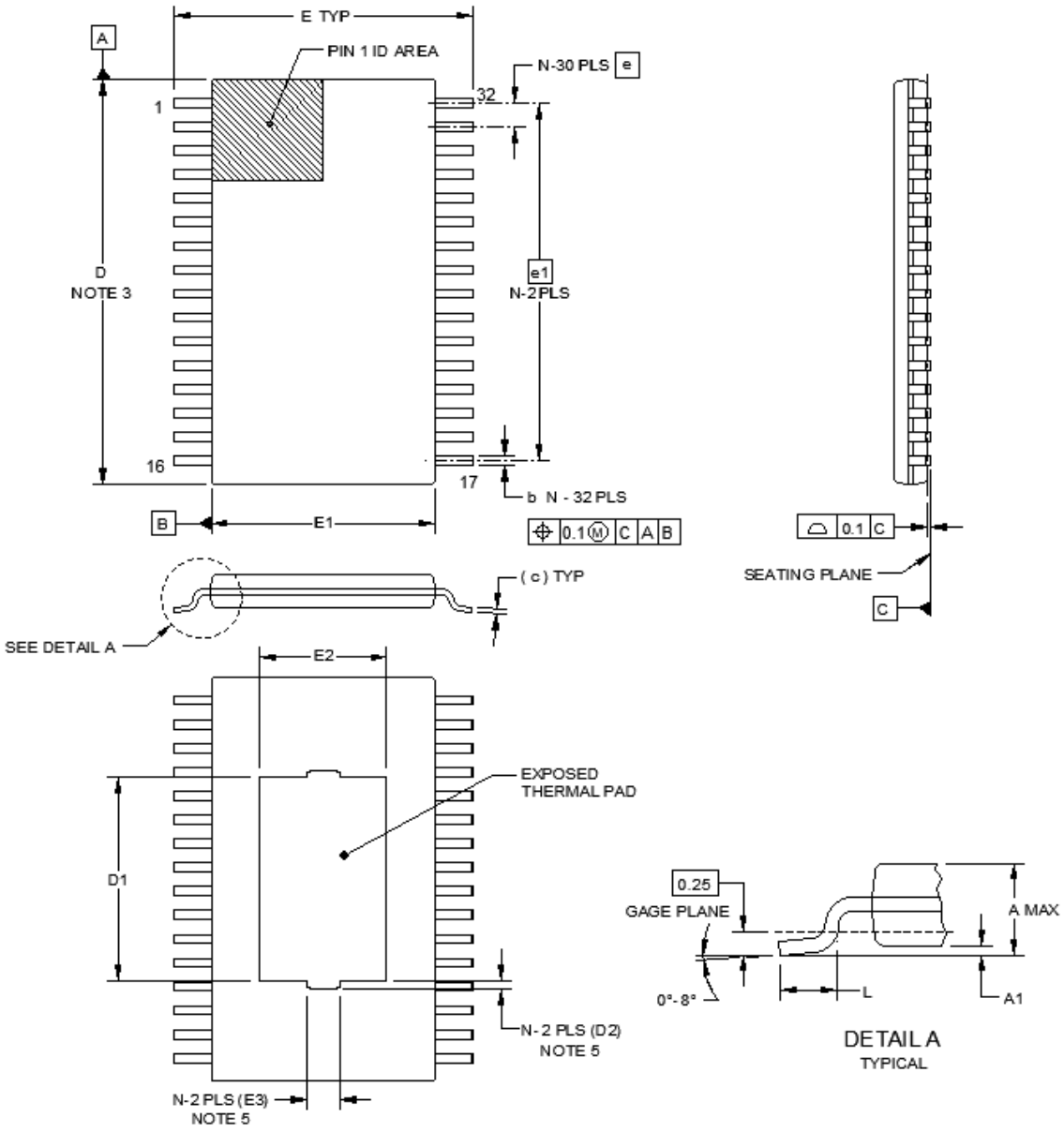

FIGURE 1. Case outline.

Dimensions				
Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A		1.20		0.0472
A1	0.05	0.15	0.0020	0.0059
b	0.19	0.30	0.0075	0.0118
c	0.15 TYP		0.0059 TYP	
D	10.90	11.10	0.4291	0.4370
D1	5.10	6.00	0.2008	0.2362
D2	0.2 TYP		0.0079 TYP	
E	7.90	8.30	0.3110	0.3268
E1	6.00	6.20	0.2362	0.2441
E2	3.00	3.90	0.1181	0.1535
E3	0.90 TYP		0.0354 TYP	
e	0.65 BSC		0.0256 BSC	
e1	9.75 BSC		0.3839 BSC	
L	0.50	0.75	0.0197	0.0295

NOTES:
1. All linear dimensions are in millimeters, inch dimensions are given for reference only. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

FIGURE 1. Case outline - Continued.

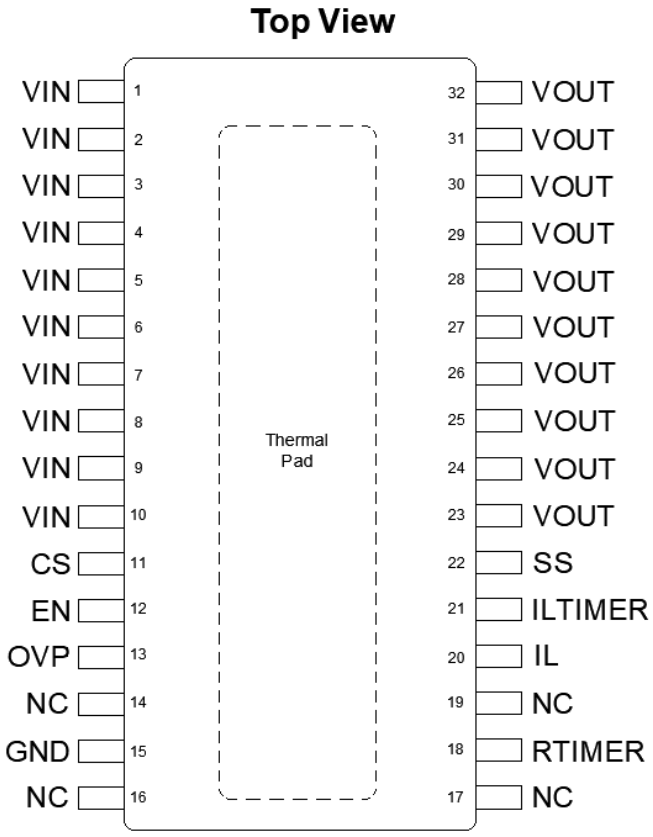

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	**Terminal symbol**	**I/O 1/**	**Description**
1-10	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip.
11	CS	O	Current sense pin proportional to output current. Connect a resistor to GND.
12	EN	I	Active high switch control input. Do not leave floating.
13	OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
14	NC	–	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
15	GND	–	Device ground. 2/
16, 17	NC	–	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
18	RTIMER	I/O	Capacitor programmed fault timer control during disable and retry mode. Connecting this pin to GND holds the switch disable until the EN pin is cycled. Do not float this pin or connect it to VIN.
19	NC	–	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
20	IL	I/O	Current limiter control. Programmable using an external resistor to GND. Do not float this pin
21	ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device will remain at programmed current limit indefinitely in the event of a short without going into retry mode. Do not float this pin.
22	SS	I/O	Switch slew rate control.
23-32	VOUT	O	Switch output. A minimum 10-µF output capacitor is recommended.
–	Thermal pad	–	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND

1/ I = Input, O = Output, I/O = Input or Output, – = Other
2/ Thermal pad is internally connected to the seal ring.

FIGURE 2. Terminal connections – Continued.

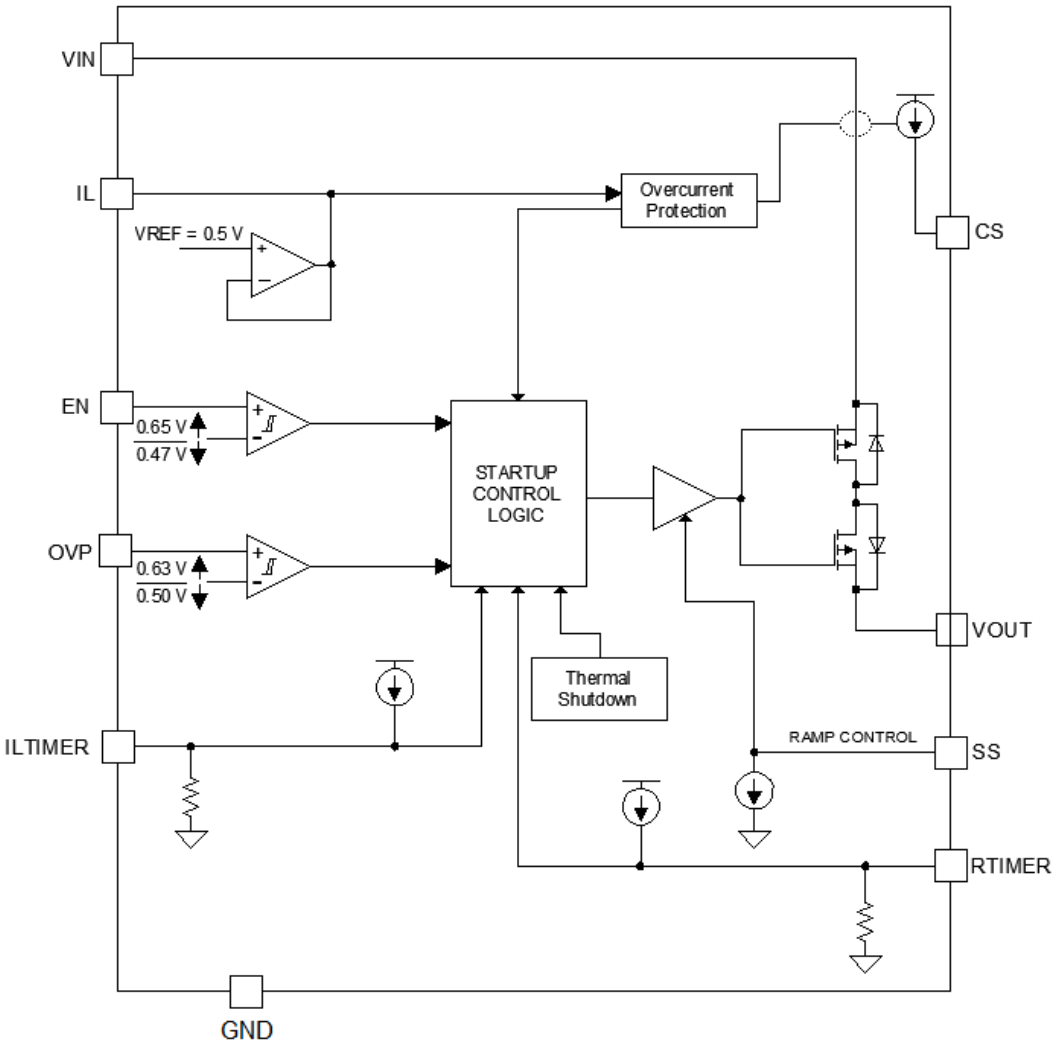

FIGURE 3. Functional Block diagrams.

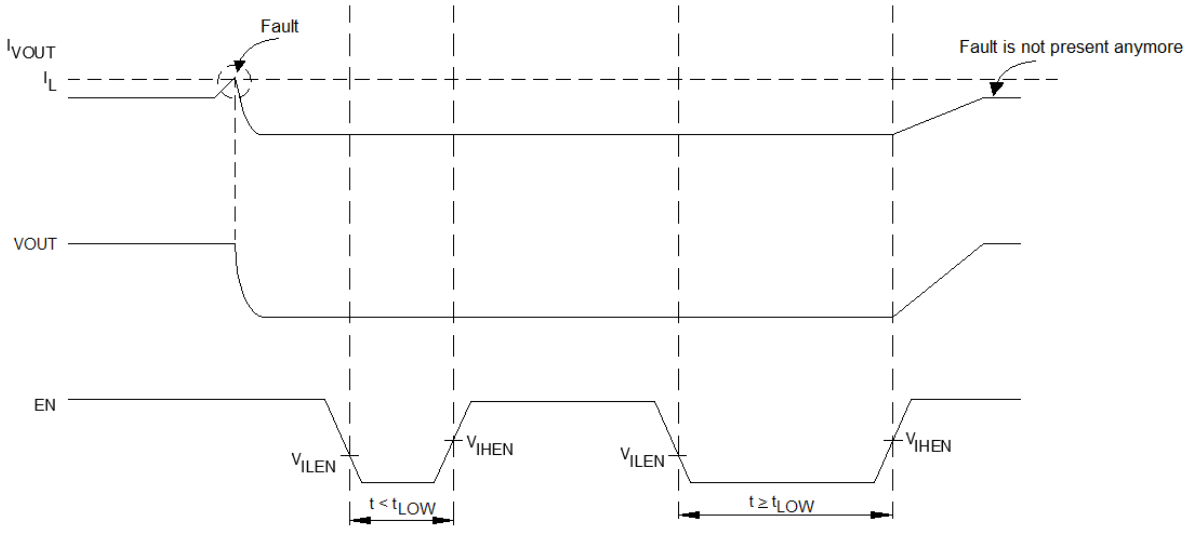

FIGURE 4. EN signal low time to restart device (t_{LOW}).

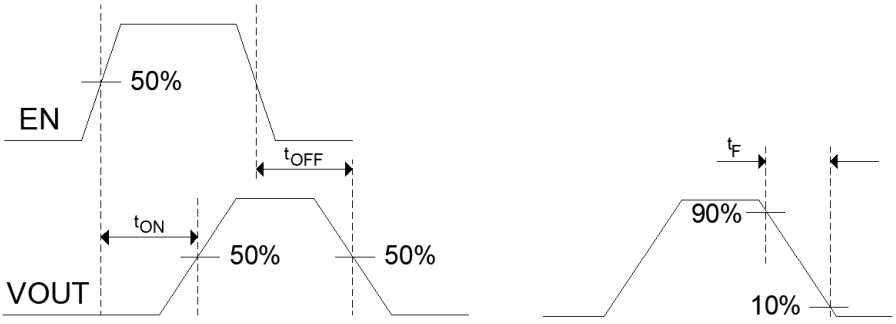

FIGURE 5. Turn-on (t_{ON}), turn-off (t_{OFF}) and VOUT fall time (t_F) waveforms.

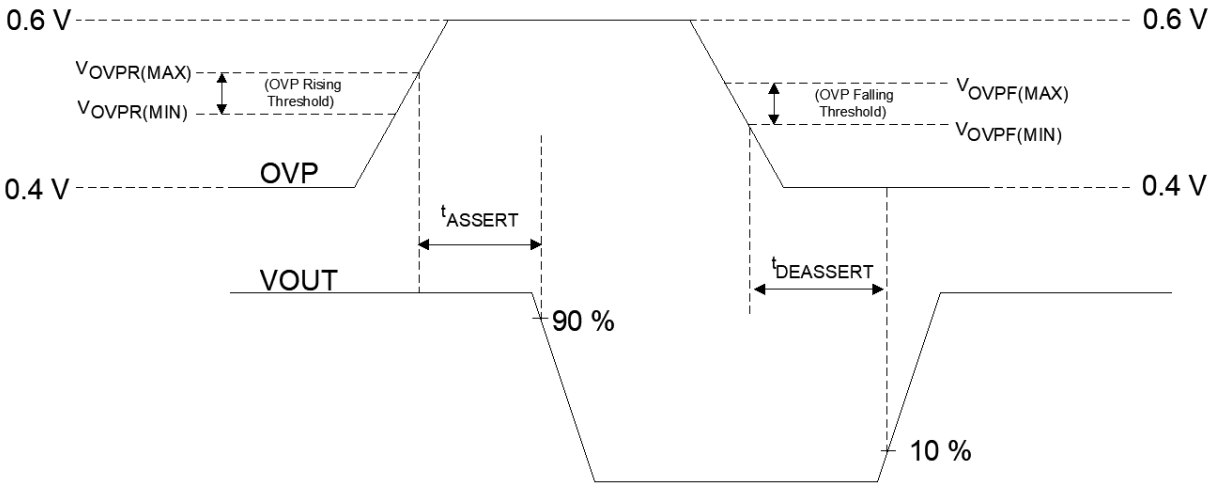

FIGURE 6. OVP assert (tASSERT) and OVP deassert (tDEASSERT) waveforms.

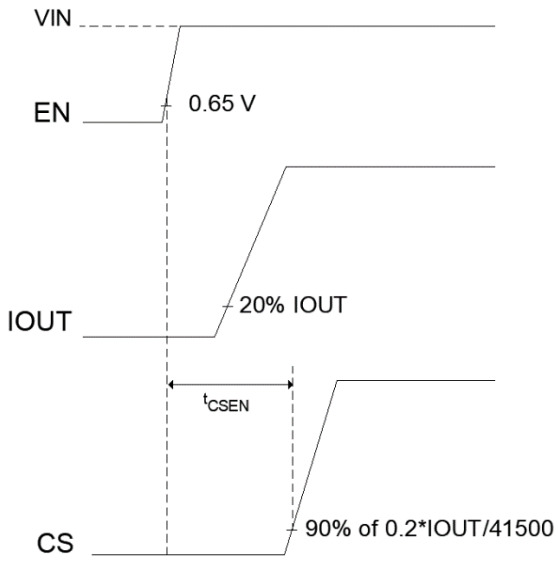

FIGURE 7. tCSEN waveforms.

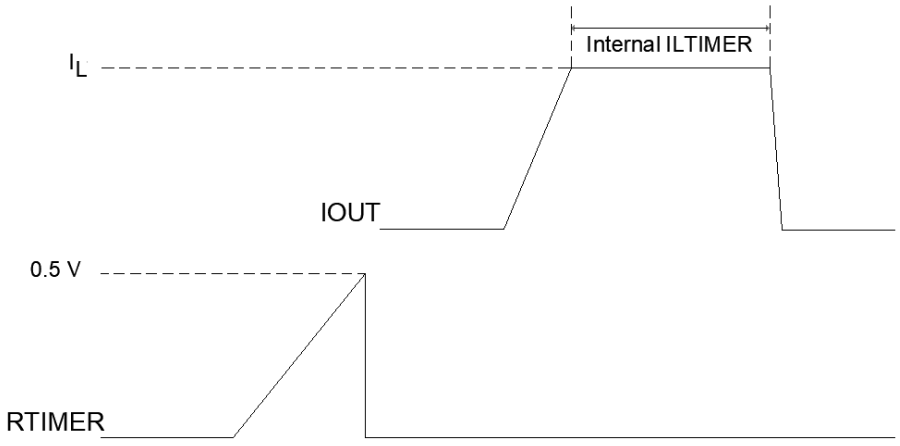

FIGURE 8. Internal ILTIMER waveforms.

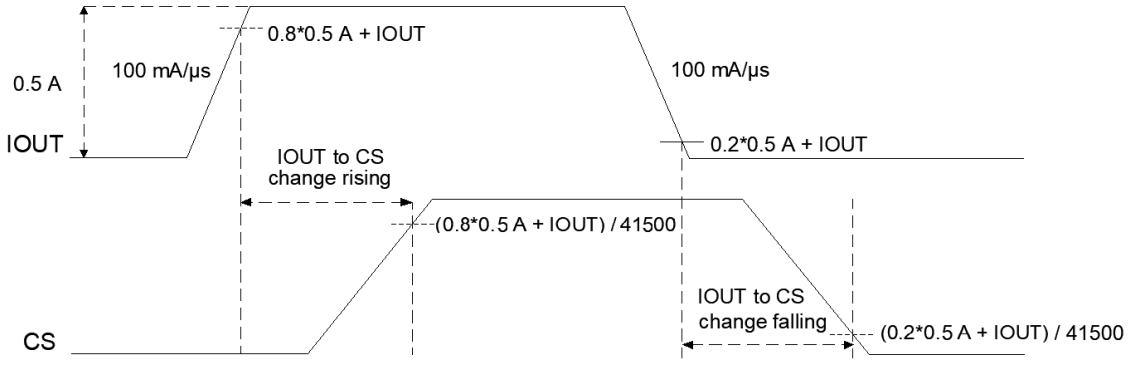

FIGURE 9. VOUT current to CS change delay time.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0°≤angle≤60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ± 10% for SEL.

f. For SEP test limits, see table IB

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Manufacturers performed devices electrostatic discharge sensitive rate with Human body model (HDM) and classified as ESDS class 1 minimum 2000 V and also performed ESDS rate with Charge device model (CDM) and classified as ESDS is 250 V.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/23608-01XE	01295	Small tape and reel, 250 units	TPS7H2201	TPS7H2201MDAPTSEP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ This device has been marked RHA TID level 50 krads(Si) with L level (see paragraph 1.5 herein).

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243