REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

Original date of drawing

YY-MM-DD
23-08-02

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TITLE

MICROCIRCUIT, LINEAR, ULTRA-LOW NOISE, HIGH PSRR, LOW DROPOUT LINEAR REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/23602
REV		PAGE 1 OF 22

AMSC N/A

5962-V048-23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance ultra-low noise, high power supply rejection ratio (PSRR), low dropout (LDO) linear regulation microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H1111-SEP	Radiation hardened ultra-low noise, high power supply rejection ratio (PSRR), low dropout (LDO) linear regulation

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	28	MO-153 - AET	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage:	
Input (IN)	-0.3 V to 7.5 V
Bias supply (BIAS)	-0.3 V to 16 V
Enable (EN), Power good indicator (PG), Feedback and Power good (FB_PG), Output sense (OUTS), Current limit mode (CLM)	-0.3 V to 7.5 V
Output voltage:	
Output (OUT)	-0.3 V to 7.5 V
Soft start and voltage set (SS_SET), Reference (REF), Stability (STAB)	-0.3 V to 7.5 V
Input current of PG	-0.001 A to 0.01 A
Output current of OUT	-2 A to 2.25 A
Junction temperature range (T_J)	-55°C to +150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient ($R\theta_{JA}$)	24.7°C/W
Thermal resistance, junction to case (top) ($R\theta_{JC(top)}$)	15.6°C/W
Thermal resistance, junction to board ($R\theta_{JB}$)	6.6°C/W
Characterization parameter, junction to top (Ψ_{JT})	0.2°C/W
Characterization parameter, junction to board (Ψ_{JB})	6.6°C/W
Thermal resistance, junction to case (bottom) ($R\theta_{JC(bot)}$)	1.0°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM), per JEDEC JS-001, all pins	±2000 V 2/
Charge device model (CDM), per JEDEC JS-002, all pins	±1000 V 3/

1.4 Recommended operating conditions. 4/

Input voltage:	
IN	0.85 V to 7 V
BIAS 5/	V_{IN} to 14 V 2.2 V to 14 V
PG, EN	0 V to 7 V
FB_PG	0 V to 6 V
CLM	0 V to V_{IN}
Output voltage:	
OUT 6/	$V_{IN} – V_{DO}$ maximum 0.4 V to 5.5 V
SS_SET 6/	$V_{IN} – V_{DO}$ maximum 0.4 V to 5.5 V

_____

1/ Operation outside the absolute maximum ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under recommended operating conditions. If used outside the recommended operating conditions but, within the absolute maximum ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ BIAS has two minimum values, V_{IN} and 2.2 V. BIAS must be set greater than or equal to the larger of these two values. The BIAS max value is always 14 V. For full performance set $V_{BIAS} \geq V_{OUT} + 1.6$ V. See the manufacturer's datasheet for further details.

6/ OUT and SS_SET have two maximum values, ($V_{IN} – V_{DO}$) and 5.5 V. OUT and SS_SET must be set to less than or equal to the smaller of these two values. The OUT and SS_SET min value is always 0.4 V.

1.4 Recommended operating conditions - continued. 4/

Input current of PG	0 A to 0.002 A
Output current of OUT	0 A to 1.5 A
Output bulk capacitance: 7/	
COUT	132 µF to 308 µF 200 µF nominal
ESR	7 mΩ to 40 mΩ
ESL	0.8 nH to 2.4 nH
Reference configuration (RREF)	11 kΩ to 13 kΩ 12 kΩ nominal
EN toggle time (t_{EN_LOW}) 8/	20 µs minimum
Junction temperature range (T_J)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s)	50 krads(Si) 9/

Heavy ion single event phenomenon (SEP):

No Single event latch-up (SEL) occurs at effective LET_{eff} (see 4.3)	≤ 43 MeV/(mg/cm^2)	10/
No Single event burnout (SEB) occurs at LET_{eff} (see 4.3)	≤ 43 MeV/(mg/cm^2)	10/
No Single event gate rupture (SEGR) occurs at LET_{eff} (see 4.3)	≤ 43 MeV/(mg/cm^2)	10/

7/ These are the default acceptable output capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL) values for the bulk capacitance. Other values may be acceptable, such as by modifying the control loop with external compensation using the STAB pin. Tantalum or Tantalum Polymer capacitors are normally used to meet these requirements. Additional ceramic decoupling capacitors are not required, but a single 0.1 µF ceramic capacitor with low ESL near the point of load is acceptable. Additional larger ceramic capacitors are not needed due to the high PSRR and low noise provided by the device LDO across a wide bandwidth. Therefore, the device is not designed to support larger ceramic capacitors. See the manufacturer's datasheet for additional information.

8/ t_{EN_LOW} is the time the EN pin must be driven low before again being driven high for the device to detect a reset. This is generally only applicable when attempting to exit turn-off current limit mode.

9/ Device type 01 supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krads(Si) as specified herein.

10/ For more information on SEP test results, customers are requested to contact the manufacturer (see SEP table IB).

2. APPLICABLE DOCUMENTS

AMERICAN SOCIETY OF MECHANICAL ENGINEERS (ASME)

ASME Y14.5 M – Dimensioning and Tolerancing. (DoD adopted)

(Copies of these documents are available from https:/www.asme.org.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) INTERNATIONAL

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

ELECTRONIC INDUSTRIES ALLIANCE

EIA-RS-198 – Ceramic Dielectric Capacitors Classes I, II, III, and IV

(Copies of these documents are available online at https://www.eia.org.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JEDEC JESD 57 – Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram . The block diagram shall be as shown in figure 3.

3.5.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

TABLE IA. Electrical performance characteristics. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supplies and currents							
Dropout voltage with $V_{BIAS} \geq V_{OUT} + 1.6$ V	V_{DO}	I_{OUT} = 0.1 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C	01		40	mV
			+25°C		17	typical	
		I_{OUT} = 0.5 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			150	
			+25°C		75	typical	
		I_{OUT} = 1 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			280	
			+25°C		110	typical	
		I_{OUT} = 1.5 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			430	
			+25°C		215	typical	
Dropout voltage with $V_{BIAS} = V_{IN}$	V_{DO}	I_{OUT} = 0.1 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C	01		1100	mV
			+25°C		785	typical	
		I_{OUT} = 0.5 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			1150	
			+25°C		908	typical	
		I_{OUT} = 1 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			1250	
			+25°C		1063	typical	
		I_{OUT} = 1.5 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	-55°C to +125°C			1400	
			+25°C		1168	typical	
Output current limit	I_{LIM}	2.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.5 V, V_{CLM} = V_{IN}	-55°C	01	1.8	2.1	A
					1.95	typical	
			+25°C		1.75	2	
					1.85	typical	
			+125°C		1.7	1.95	
					1.8	typical	
CLM input leakage current	$I_{CLM(LKG)}$	V_{CLM} = 7 V	-55°C to +125°C	01		150	nA
			+25°C		5	typical	
Quiescent current	I_{Q_IN}	V_{EN} = 7 V, I_{OUT} = 0 A	-55°C to +125°C	01		27	mA
			+25°C		19	typical	
Bias current with no output load	I_{Q_BIAS}	V_{EN} = 7 V, I_{OUT} = 0 A	-55°C to +125°C	01		25	mA
			+25°C		16	typical	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supplies and curre nts - contin ued.							
I_{IN} – I_{OUT} with full output load	I_{IN_GND}	V_{EN} = 7 V, I_{OUT} = 1.5 A	-55°C to +125°C	01		27	mA
			+25°C		20 typical		
Bias current with full output load	I_{BIAS}	V_{EN} = 7 V, I_{OUT} = 1.5 A	-55°C to +125°C	01		25	mA
			+25°C		17 typical		
Shutdown current	ISHDN	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V	-55°C to +125°C	01		350	µA
			+25°C		20 typical		
Shutdown bias current	ISHDN _BIAS	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V	-55°C to +125°C	01		1000	µA
			+25°C		550 typical		
Accuracy							
Output voltage accuracy	V_{ACC}	1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V, 4/ P_D ≤ 4 W 5/	-55°C to +125°C	01	-1.3	1.2	%
			-55°C		-1.3	0.5	
			+25°C		-0.7	0.9	
			+125°C		-0.7	1.2	
		M,D,P,L,R, 1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V, 4/ P_D ≤ 4 W 5/	+25°C		-0.7	1.1	
SS_SET pin current to set V_{OUT}	I_{SET}		-55°C to +125°C	01	98.8	101	µA
					99.9 typical		
			-55°C		98.8	100.3	
					99.4 typical		
			+25°C		99.0	100.9	
					100 typical		
			+125°C		99.2	101	
					100.2 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Accuracy – continued.							
Output offset voltage ($V_{OUT} - V_{SS\_SET}$)	VOS		-55°C to +125°C	01	-2.0	0.78	mV
			-55°C		-1.33	0.78	
					-0.1	typical	
			+25°C		-1.45	0.7	
					-0.25	typical	
			+125°C		-2	0.7	
					-0.5	typical	
		M,D,P,L,R	+25°C		-1.45	1.5	
V_{OUT} temperature coefficient	V_{OUT} tempco		-55°C to +125°C	01	0.004%	typical	V_{OUT} / °C
			-55°C to +40°C		0.011%	typical	
			-40°C to +0°C		0.007%	typical	
			0°C to +25°C		0.005%	typical	
			+25°C to +85°C		0.003%	typical	
			+85°C to +125°C		0.001%	typical	
Reference voltage	V_{REF}		-55°C to +125°C	01	1.190	1.221	V
					1.206	typical	
Line regulation	ΔV_{OUT} / ΔV_{IN}	0.85 V ≤ V_{IN} ≤ 7 V, I_{OUT} = 1 mA, V_{BIAS} = 5 V, V_{OUT} = 0.4 V, see manufacturer's datasheet	-55°C to +125°C	01		200	µV/V
			+25°C		3	typical	
Load regulation	ΔV_{OUT} / ΔI_{OUT}	1 mA ≤ I_{OUT} ≤ 1.5 A, V_{BIAS} = 5 V, V_{IN} = 2.5 V, V_{OUT} = 1.8 V see manufacturer's datasheet	-55°C to +125°C	01		1000	µV/A
			+25°C		500	typical	
Current sharing error percentage		$I_{OUT(TOTAL)}$ = 1.2 A, $R_{ballast}$ = 5 mΩ	+25°C	01	±1%	typical	
		$I_{OUT(TOTAL)}$ = 2.9 A, $R_{ballast}$ = 5 mΩ			±0.1%	typical	
OUTS leakage current	I_{OUTS} (LKG)		-55°C to +125°C	01		200	nA
			+25°C		20	typical	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
ENABLE							
Enable rising threshold (turn-on)	$V_{EN(rising)}$		-55°C to +125°C	01	0.58	0.62	V
			+25°C		0.60 typical		
Enable falling threshold (turn-off)	$V_{EN(falling)}$		-55°C to +125°C	01	0.48	0.52	V
			+25°C		0.50 typical		
EN propagation delay	$t_{EN(delay)}$	EN high to V_{OUT} = 10 mV	-55°C to +125°C	01		500	µs
			+25°C		90 typical		
Enable input leakage current	$I_{EN(LKG)}$	V_{EN} = 7 V	-55°C to +125°C	01		150	nA
			+25°C		3 typical		
Thermal shutdown enter	$T_{SD(enter)}$			01	160 typical		°C
Thermal shutdown exit	$T_{SD(exit)}$			01	130 typical		°C
POWER GOOD							
Power good rising threshold	$V_{FB\_PG(rising)}$		-55°C to +125°C	01	290	313	mV
			+25°C		306 typical		
Power good hysteresis	$V_{FB\_PG(HYS)}$		-55°C to +125°C	01	7	19	mV
			+25°C		14 typical		
FB_PG input leakage current	$I_{FB\_PG(LKG)}$	V_{FB_PG} = 6 V	-55°C to +125°C	01		150	nA
			+25°C		9 typical		
Power good output low	$V_{PG(OL)}$	$I_{PG(SINK)}$ = 2 mA	-55°C to +125°C	01		200	mV
			+25°C		113 typical		
Minimum V_{IN} or V_{BIAS} for valid PG (V_{PG} < 0.5 V)	$V_{IN(MIN\_PG)}$	$I_{PG(sink)}$ = 0.6 mA	-55°C to +125°C	01		0.8	V
			+25°C		0.6 typical		
Power good leakage	$I_{PG(LKG)}$	V_{PG} = 7 V, V_{FB_PG} > $V_{FB\_PG(rising threshold)}$	-55°C to +125°C	01		2	µA
			+25°C		0.1 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SOFT START							
SS_SET pin current during startup	I_{SS_SET} (start)		-55°C to +125°C	01	1.68	2.52	mA
			+25°C		2.1	typical	
Soft start time	t_{SS}	C_{SS} = 2.2 µF, V_{IN} = 2.5 V, V_{OUT} =1.8 V, I_{OUT} = 1 A, $R_{FB\_PG(top)}$ = 44.2 kΩ, $R_{FB\_PG(bot)}$ = 10 kΩ	+25°C	01	1.7	typical	ms
		C_{SS} = 4.7 µF, V_{IN} = 2.5 V, V_{OUT} =1.8 V, I_{OUT} = 1 A, $R_{FB\_PG(top)}$ = 44.2 kΩ, $R_{FB\_PG(bot)}$ = 10 kΩ			3.7	typical	
		C_{SS} = 10 µF, V_{IN} = 2.5 V, V_{OUT} =1.8 V, I_{OUT} = 1 A, $R_{FB\_PG(top)}$ = 44.2 kΩ, $R_{FB\_PG(bot)}$ = 10 kΩ			7.8	typical	
NOISE and PSRR							
Power supply rejection ratio	PSRR	f_{ripple} = 100 Hz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω	+25°C	01	109	typical	dB
		f_{ripple} = 1 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			109	typical	
		f_{ripple} = 10 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			90	typical	
		f_{ripple} = 100 kHz, V_{IN} = 2.5 V, V_{OUT} =1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			71	typical	
		f_{ripple} = 1 MHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			66	typical	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
NOISE and PSRR - continued							
Power supply rejection ratio	PSRR	f_{ripple} = 10 MHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω	+25°C	01	30 typical		dB
Power supply rejection ratio V_{BIAS} to V_{OUT}	PSRR BIAS	f_{ripple} = 100 Hz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω	+25°C	01	102 typical		dB
		f_{ripple} = 1 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			105 typical		
		f_{ripple} = 10 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			87 typical		
		f_{ripple} = 100 kHz, V_{IN} =2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			97 typical		
		f_{ripple} = 1 MHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			118 typical		
		f_{ripple} = 10 MHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω			68 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
NOISE and PSRR - conti nued.							
Output noise rms voltage (Bandwidth from 10 Hz to 100 kHz)	V_{IN}	C_{SS} = 2.2 µF V_{IN} = 2.5 V, V_{OUT} = 1.8 V, VBIAS = 5 V, I_{OUT} = 1 A	+25°C	01	1.73 typical		µVRMS
		C_{SS} = 4.7 µF V_{IN} = 2.5 V, V_{OUT} = 1.8 V, VBIAS = 5 V, I_{OUT} = 1 A			1.71 typical		
		C_{SS} = 10 µF V_{IN} = 2.5V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A			1.69 typical		
Output noise voltage density	e_N	f = 10 Hz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF	+25°C	01	97 typical		$nV/\sqrt{Hz}$
		f = 100 Hz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			11.2 typical		
		f = 1 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			5.4 typical		
		f = 10 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			5.6 typical		
		f = 100 kHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			4.9 typical		
		f = 1 MHz, V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			1.6 typical		
		f = 10 MHz, V_{IN} =2.5 V, V_{OUT} =1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF			1.7 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued. 1/ 2/ 3/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
STABILITY							
Phase margin	PM	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A, C_{OUT} = 2 x 100 µF	+25°C	01	98° typical		
Gain margin	GM	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A, C_{OUT} = 2 x 100 µF	+25°C	01	19 typical		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Device type 01 supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 50 krads(Si) as specified herein.

3/ Over 0.85 V ≤ V_{IN} ≤ 7 V, V_{BIAS} ≥ V_{OUT} + 1.6 V (V_{IN} ≤ V_{BIAS} ≤ 14 V and V_{BIAS} ≥ 2.2 V), V_{OUT} (target) ≤ V_{IN} – 1.6 V, I_{OUT} = 1 mA, C_{OUT} = 220 µF (a single 220 µF tantalum capacitor is utilized), R_{REF} = 12.0 kΩ, over operating temperature range (T_A = –55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted.
See Figure 4 for Line regulation and Figure 5 for load regulation.

4/ Additionally, V_{BIAS} ≥ V_{IN} and VBIAS ≥ VOUT + 1.6 V.

5/ P_D is the internal power dissipation. When P_D exceeds 4 W, the current is lowered to avoid excessive local heating (due to tester limitations).

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_C)	V_{IN}	V_{BIAS}	Linear energy transfer (LET_{eff})
01	No SEL	125°C	7 V	14 V	LET_{eff} ≤ 43 MeV/(mg/cm^2)
	No SEB	25°C	7 V	14 V	LET_{eff} ≤ 43 MeV/(mg/cm^2)
	No SEGR	25°C	7 V	14 V	LET_{eff} ≤ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEP test results, customers are requested to contact the manufacturer.

Case X

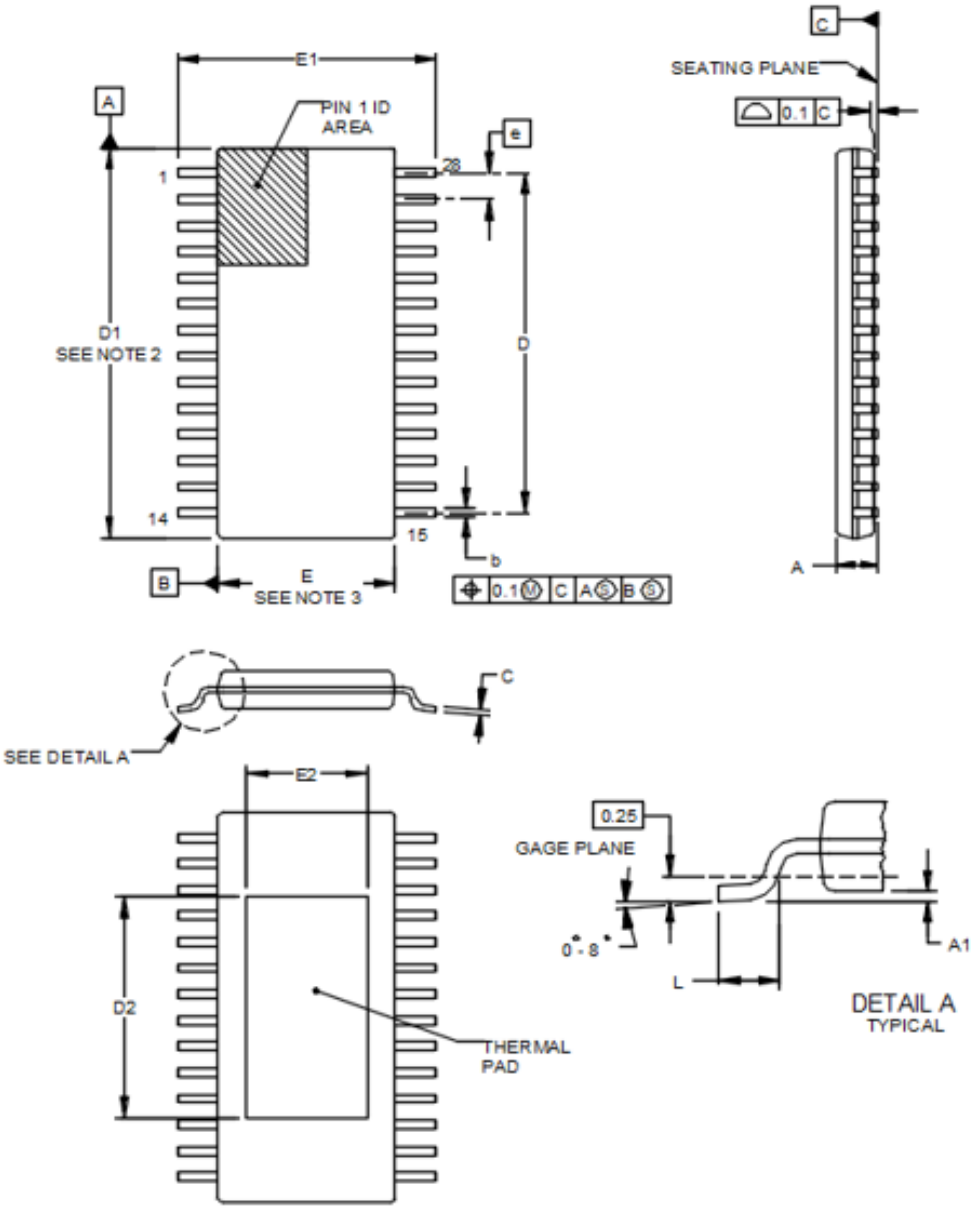


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/23602
		REV	PAGE 14

Symbol	Dimensions			
	Inches		Millimeter	
	Minimum	Maximum	Minimum	Maximum
A	---	.043	---	1.1
A1	.001	.004	0.02	0.10
b	.007	.012	0.19	0.30
c	.003	.008	0.09	0.20
D	.332 BSC		8.45 BSC	
D1	.378	.386	9.6	9.8
D2	.207	.222	5.25	5.65
E	.169	.177	4.3	4.5
E1	.244	.260	6.2	6.6
E2	.108	.124	2.75	3.15
e	.026 BSC		0.65 BSC	
L	.020	.027	0.5	0.7

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. Dimension D1 does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. Dimension E does not include interlead flash. Interlead flash shall not exceed 0.25 mm (.010 inch) per side.
4. Falls within reference to JEDEC MO-153 variation AET.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
2	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
3	BIAS	I	Bias supply. To support full output current, a separate bias supply is required if the headroom voltage is less than 1.6 V ($V_{headroom} = V_{IN} - V_{OUT} < 1.6$ V). Set the separate bias supply to a voltage at least 1.6 V higher than V_{OUT} for full output current support. A 12 V bias supply will satisfy these conditions (generally a 5 V supply will also suffice). There are no sequencing requirements between V_{BIAS} and V_{IN}. In order to limit noise on BIAS, an RC filter is recommended (typically 10 Ω and 4.7 µF) unless V_{BIAS} is an ultra-clean supply. If a separate bias supply is not used, connect BIAS to V_{IN} (it is also recommended to connect the V_{IN} rail to the BIAS pin through an RC filter).
4	EN	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to IN. Do not float this pin.
5	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
6	IN	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
7	IN	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
8	IN	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
9	CLM	I	Current limit mode. Connect CLM to V_{IN} for brick wall current limit mode (when current limit is reached, V_{OUT} is regulated to maintain a constant output current until the fault is removed). Connect CLM to GND for turn-off current limit mode (when current limit is reached, V_{OUT} stops regulating until EN is toggled). Do not change the value of this pin when the device is enabled, and do not float this pin.

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
10	GND	---	Ground.
11	GND	---	Ground.
12	PG	O	Power good indicator. This is an open drain pin. Use a pull-up resistor to pull this pin up to V_{OUT} or the desired logic level. It may be pulled down to ground if unused.
13	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
14	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
15	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
16	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
17	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
18	REF	I/O	Reference pin. REF outputs a nominal 1.2 V. Place a high accuracy 12.0 kΩ external resistor from REF to GND to set the internal 100 µA current source.
19	SS_SET	I/O	Soft start and voltage set pin. An external capacitor (nominally 4.7 µF ceramic) is used to slow down the output voltage ramp rate during startup along with filtering internal device noise. Capacitor values less than 4.7 µF will result in marginally higher output noise. There is internal fast start circuitry to enable reasonable soft start times. Additionally, a resistor from SS_SET to GND sets the output voltage. During nominal operation, 100 µA is output on this pin and a resistor from SS_SET to GND sets the output voltage.
20	STAB	I/O	Stability pin. This is an output from the internal operational transconductance (OTA) error amplifier to aid in measuring or optimizing the control loop. Use a series capacitor (C_{COMP}) and resistor (R_{COMP}) of 4.7 nF and 5 kΩ to compensate the device. For different compensation options, see manufacturer's datasheet. A C0G (NP0) type ceramic dielectric capacitor capable of withstanding the lower of V_{BIAS} or 7.5 V is recommended (for example, a 25 V rated capacitor). See NOTE.

FIGURE 2. Terminal connections - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
21	OUT	O	Output power pin. The regulated output voltage. A single 220 µF or two 100 µF tantalum or tantalum polymer capacitors are recommended. See manufacturer's datasheet for additional information.
22	OUT	O	Output power pin. The regulated output voltage. A single 220 µF or two 100 µF tantalum or tantalum polymer capacitors are recommended. See manufacturer's datasheet for additional information.
23	OUT	O	Output power pin. The regulated output voltage. A single 220 µF or two 100 µF tantalum or tantalum polymer capacitors are recommended. See manufacturer's datasheet for additional information.
24	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
25	OUTS	I	Output sense pin. This pin is used to sense the output voltage for regulation. Connect OUTS to the OUT pin at the desired point of regulation (remote sense).
26	FB_PG	I	Feedback and power good pin. The FB_PG pin enables setting of a configurable power good threshold. This is achieved by feeding the output voltage through a resistor divider to this pin (typical threshold of 300 mV). When the threshold is reached, PG is asserted. Additionally, when the threshold on this pin is reached, start-up is over and the internal fast start circuitry is disabled. If this pin is connected directly to OUT, fast start operation ceases and PG is asserted as soon as V_{OUT} reaches 300 mV (typical).
27	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
28	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
Thermal pad			It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.

NOTE: Reference EIA standard RS-198. COG, C = letter code meaning 0 temperature coefficient, 0 = temperature coefficient multiplier, and G = letter code. NP0 = Negative positive 0ppm/°C.

FIGURE 2. Terminal connections - continued.

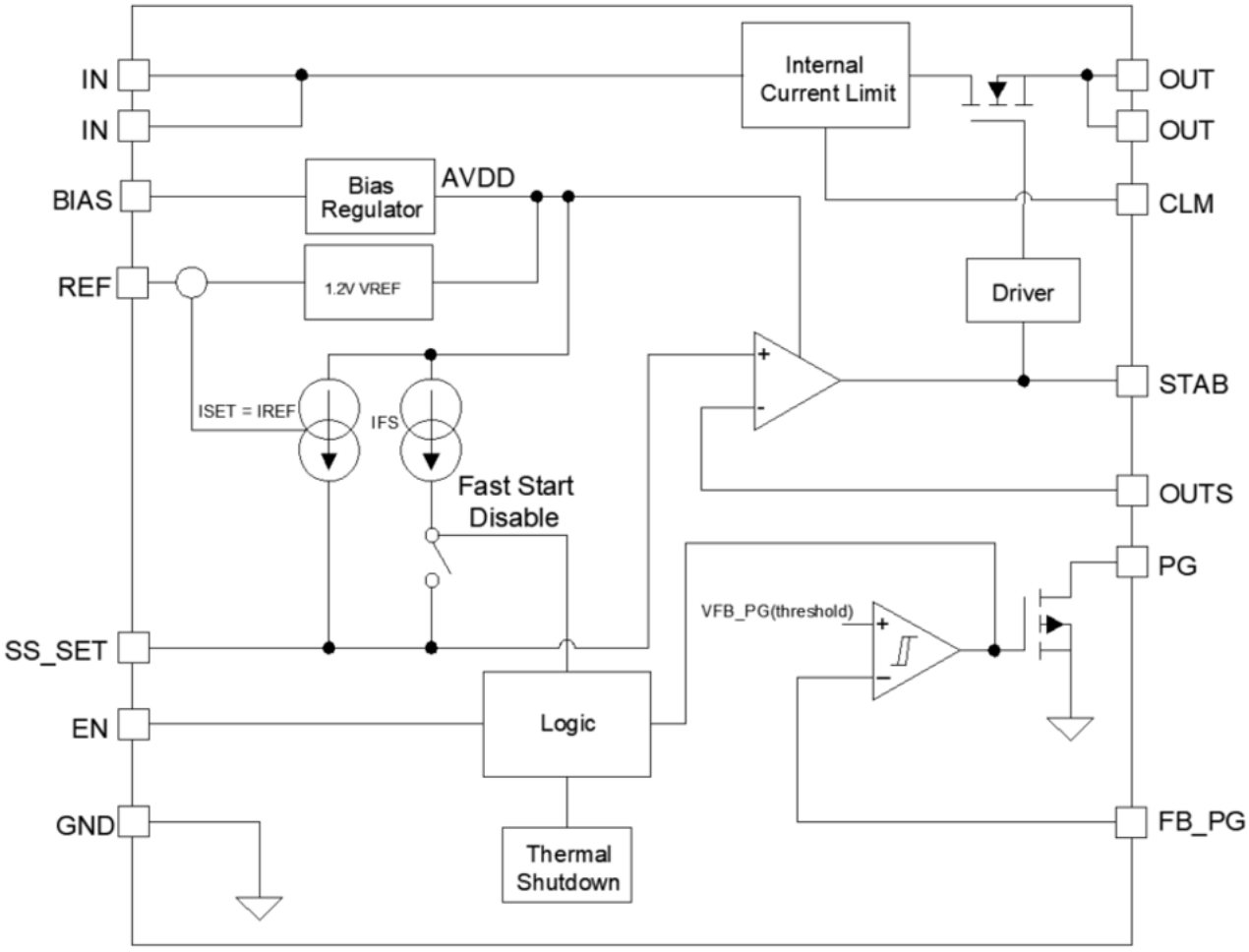
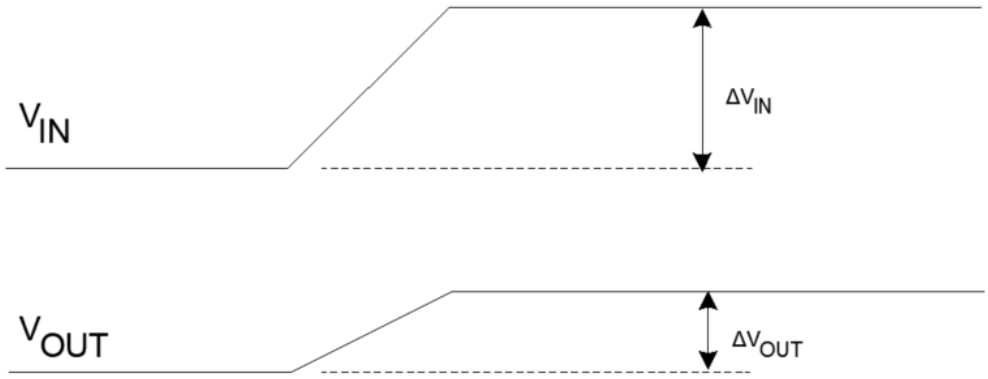
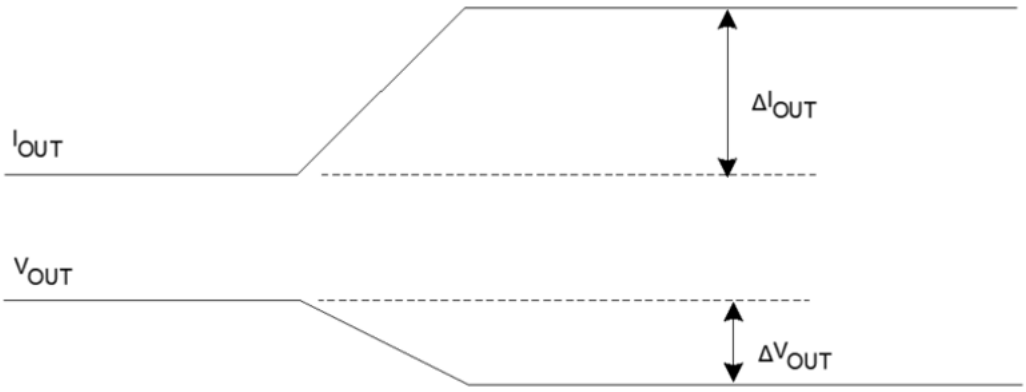


FIGURE 3. Block diagram.



NOTE: $\Delta V_{OUT}/\Delta V_{IN}$ = 3 µV/V. This means for a 1 V change in V_{IN} (ΔV_{IN} = 1 V), there will be a 3 µV change in ΔV_{OUT} (ΔV_{OUT} = 3 µV). Line regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow V_{IN} slew rate.

FIGURE 4. Line regulation.



NOTE: $\Delta V_{OUT}/\Delta I_{OUT}$ = 500 µV/V. This means for a 1 A change in I_{OUT} (ΔI_{OUT} = 1 A), there will be a 500 µV change in ΔV_{OUT} (ΔV_{OUT} = 500 µV). Load regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow I_{OUT} slew rate.

FIGURE 5. Load regulation.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for all device types and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C $\pm$10% for SEL.

f. For SEP test limits, see table IB herein.

g. For SEL test limits, see table IB herein.

h. For SEB test limits, see table IB herein.

i. For SEGR test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latch-up (SEL).

c. Occurrence of burnout (SEB).

e. Occurrence of gate rupture (SEGR).

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/23602-01XE	01295	Small tape and reel, 250 units	7H1111PWP	TPS7H1111MPWPTSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243