REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

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TITLE
MICROCIRCUIT, LINEAR, 2 MHz CURRENT MODE PWM CONTROLLERS, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO.
V62/22607

REV

PAGE 1 OF 20

AMSC N/A

5962-V045-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 2 MHz current mode pulse width modulator (PWM) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/22607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H5005-SEP	2 MHz current mode pulse width modulator
02	TPS7H5006-SEP	2 MHz current mode pulse width modulator
03	TPS7H5007-SEP	2 MHz current mode pulse width modulator
04	TPS7H5008-SEP	2 MHz current mode pulse width modulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	MO-153	Thin scale small outline package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input:
- VIN ..... -0.3 V to 16 V
- RT, VSENSE, SS, RSC, COMP, PS, SP, HICC, LEB ..... -0.3 V to 3.3 V
- SYNC ..... -0.3 V to 7.5 V
- EN, FAULT ..... -0.3 V to 7.5 V
- DCL, CS_ILIM ..... -0.3 V to 7.5 V

Output:
- OUTA, OUTB, SRA and SRB ..... -0.3 V to 7.5 V
- VLDO ..... -0.3 V to 7.5 V
- REFCAP ..... -0.3 V to 3.3 V

Junction temperature range (T_J) ..... -55°C to +150°C

Storage temperature range (T_{STG}) ..... -65°C to +150°C

Electrostatic discharge (ESD) rating:
- Human body model (HDM), per JEDEC JS-001, all pins ..... ±1000 V 2/
- Charge device model (CDM), per JEDEC JS-002, all pins ..... ±250 V 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (VIN) ..... 4 V to 14 V

Input voltage slew rate (SR_{VIN}) ..... 0.03 V/μs maximum

Junction temperature range (T_J) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	74.5	°C/W
Thermal resistance, junction-to-board	θ_{JB}	30.8	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	17.9	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.8	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	30.3	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.6 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) ..... 50 krads(Si) 5/

Heavy ion single event phenomenon (SEP):
No Single event latchup (SEL) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 6/
No Single event burn out (SEB) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 6/
No Single event gate rupture (SEGR) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 6/

2. APPLICABLE DOCUMENTS

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

5/ Device types 01-04 supplied to this drawing have been total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A to TID level of 50 krads(Si). Post irradiation electrical parametric limits falls within the specification limits during electrical measurement. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 50 krads(Si).

6/ For more information on SEP test results, customers are requested to contact the manufacturer (see SEP table IB).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Outputs timing waveforms. The outputs timing waveforms shall be as shown in figure 3.

3.5.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
SUPPLY VOLTAGES AND CURRENTS							
Operating input voltage	VIN		-55°C to +125°C	01,02, 03,04	4	14	V
Operating supply current	IDD	f_{SW} = 500 kHz, no load for OUTA, OUTB, SRA, and SRB	-55°C to +125°C	01,02,		8	mA
				03,04	6.25 typical		
		f_{SW} = 1 MHz, no load for OUTA, OUTB, SRA, and SRB				9.5	
					6.75 typical		
		f_{SW} = 2 MHz, no load for OUTA, OUTB, SRA, and SRB				13.5	
					8.5 typical		
		f_{SW} = 500 kHz, C_L = 100 pF, for OUTA, OUTB, SRA, and SRB				9.5	
					7.5 typical		
		f_{SW} = 1 MHz, C_L = 100 pF, for OUTA, OUTB, SRA, and SRB				12	
					9 typical		
		f_{SW} = 2 MHz, C_L = 100 pF, for OUTA, OUTB, SRA, and SRB				19.5	
					14 typical		
Standby current	$I_{DD(dis)}$	EN = 0 V	-55°C to +125°C	01,02, 03,04		3	mA
Internal linear regulator output voltage	VLDO	5 V ≤ VIN ≤ 14 V, f_{SW} ≤ 1 MHz	-55°C to +125°C	01,02,	4.75	5.2	V
				03,04	5 typical		
Internal linear regulator output voltage	VLDO	5 V ≤ VIN ≤ 14 V, f_{SW} = 2 MHz	-55°C to +125°C	01,02,	4.65	5.2	V
				03,04	5 typical		
ENABLE AND UNDERVO LTAGE LOCKOUT							
EN threshold rising	V_{ENR}		-55°C to +125°C	01,02,	0.57	0.65	V
				03,04	0.6 typical		
EN threshold falling	V_{ENF}		-55°C to +125°C	01,02,	0.47	0.55	V
				03,04	0.5 typical		
EN hysteresis voltage	V_{ENH}		-55°C to +125°C	01,02,	85	105	mV
				03,04	95 typical		
EN pin input leakage current	I_{EN}	VIN = 14 V, EN = 5 V	-55°C to +125°C	01,02,		50	nA
				03,04	5 typical		
VLDO UVLO rising	$VLDO_{UVLOR}$		-55°C to +125°C	01,02,	3.44	3.66	V
				03,04	3.55 typical		
VLDO UVLO falling	$VLDO_{UVLOF}$		-55°C to +125°C	01,02,	3.29	3.51	V
				03,04	3.4 typical		
VLDO UVLO hysteresis	$VLDO_{UVLOH}$		-55°C to +125°C	01,02,	115	160	V
				03,04	135 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
SOFT START							
Soft start current	I_{SS}	SS = 0.3 V	-55°C to +125°C	01,02,	1.98	3.32	µA
				03,04	2.7 typical		
ERROR AMPLIFIER							
Transconductance	EA_{gm}	–2 µA < I_{COMP} < 2 µA,	-55°C to +125°C	01,02,	1150	2500	µA/V
		$V_{(COMP)}$ = 1 V		03,04	1800 typical		
DC gain	EA_{DC}	V_{SENSE} = 0.6 V	-55°C to +125°C	01,02, 03,04	10000 typical		V/V
Error amplifier source current	EA_{ISRC}	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	-55°C to +125°C	01,02, 03,04	100	190	µA
Error amplifier sink current	EA_{ISNK}	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	-55°C to +125°C	01,02, 03,04	100	190	µA
Error amplifier output resistance	EA_{ro}		-55°C to +125°C	01,02, 03,04	7 typical		MΩ
Error amplifier input offset voltage	EA_{OS}		-55°C to +125°C	01,02, 03,04	-2	2	mV
Error amplifier input bias current	EA_{IB}		-55°C to +125°C	01,02, 03,04		35	nA
Bandwidth	EA_{BW}		-55°C to +125°C	01,02, 03,04	10 typical		MHz
OSCILLATOR							
SYNC in low level	$SYNC_{IL}$	VIN < 5 V	-55°C to +125°C	01,02,		0.8	V
		VIN ≥ 5 V		03,04		0.8	
SYNC in high level	$SYNC_{IH}$	VIN < 5 V	-55°C to +125°C	01,02,	3.5		V
		VIN ≥ 5 V		03,04	3.5		
SYNC in frequency range	F_{SYNC}		-55°C to +125°C	01,02, 03,04	200	4000	kHz
SYNC in duty cycle	D_{SYNC}	Duty cycle of external clock	-55°C to +125°C	01,02, 03,04	40	60	%
SYNC out low-to-high	$SYNC_{RT}$	C_L = 25 pF	-55°C to +125°C	01,02,		15	ns
rise time (10%/90%)				03,04	6 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
OSCILLATOR – continued.							
SYNC out high to low	$SYNC_{FT}$	C_L = 25 pF	-55°C to +125°C	01,02,		17	ns
fall time (10%/90%)				03,04	6 typical		
SYNC out low level	$SYNC_{OL}$	I_{OL} = 10 mA	-55°C to +125°C	01,02, 03,04		500	mV
SYNC out high level 3/	VLDO – $SYNC_{OH}$	I_{OH} = 10 mA	-55°C to +125°C	01,02, 03,04		0.5	V
Externally set frequency detection time	EXT_{DT}	RT = Open, f = 200 kHz	-55°C to +125°C	01,02, 03,04		20	µs
Externally set frequency	FSW_{EXT}	RT = 1.07 MΩ	-55°C to +125°C	01,02,	95	115	kHz
				03,04	105 typical		
		RT = 511 kΩ			190	230	
					210 typical		
		RT = 90.0 kΩ			900	1100	
					1000 typical		
		RT = 34.8 kΩ			1700	2300	
					2000 typical		
VOLTAGE REFERENCE							
Internal voltage reference	VREF	Measured at COMP	+25°C	01,02,	0.609	0.615	V
initial tolerance				03,04	0.613 typical		
Internal voltage reference		Measured at COMP	-55°C	01,02,	0.607	0.612	
				03,04	0.609 typical		
		Measured at COMP	+125°C	01,02,	0.611	0.617	
				03,04	0.614 typical		
REFCAP voltage	REFCAP	REFCAP = 470 nF	-55°C to +125°C	01,02,	1.213	1.237	V
				03,04	1.225 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
CURRENT SENSE, CURRENT LIMIT AND HICCUP							
COMP to CS_LIM ratio	CCSR		-55°C to +125°C	01,02,	2.00	2.12	
				03,04	2.06 typical		
Current limit (overcurrent) threshold	V_{CS_ILIM}		-55°C to +125°C	01,02,		1.09	V
				03,04	1.05 typical		
Hiccup delay current	I_{HICC_DEL}	CS_ILIM = 1.3 V, COMP = 3 V, VSENSE = REFCAP/2 V, C_{HICC} = 3 nF, LEB = 49.9 kΩ, f_{SW} = 100 kHz	-55°C to +125°C	01,02, 03,04	80 typical		µA
Hiccup restart current	I_{HICC_RST}		-55°C to +125°C	01,02, 03,04	1 typical		µA
Hiccup pull up threshold	V_{HICC_PU}		-55°C to +125°C	01,02, 03,04	1.0 typical		V
Hiccup shut down threshold	V_{HICC_SD}		-55°C to +125°C	01,02, 03,04	0.6 typical		V
Hiccup restart threshold	V_{HICC_RST}		-55°C to +125°C	01,02, 03,04	0.3 typical		V
SLOPE COMPENSATION							
Slope compensation		f_{SW} = 100 kHz, RSC = 1.18 MΩ	-55°C to +125°C	01,02, 03,04	0.033 typical		V/µs
		f_{SW} = 200 kHz, RSC = 562 kΩ			0.066 typical		
		f_{SW} = 1000 kHz, RSC = 100 kΩ			0.333 typical		
		f_{SW} = 2000 kHz, RSC = 49.9 kΩ			0.666 typical		
FAULT							
FLT threshold rising	V_{FLTR}		-55°C to +125°C	01,02,	0.57	0.65	V
				03,04	0.6 typical		
FLT threshold falling	V_{FLTF}		-55°C to +125°C	01,02,	0.47	0.55	V
				03,04	0.5 typical		
FLT hysteresis voltage	V_{FLTH}		-55°C to +125°C	01,02,	90	110	mV
				03,04	100 typical		
FLT minimum pulse width	T_{FLT}	V_{FLT} = 1 V	-55°C to +125°C	01,02, 03,04	0.4	1.4	µs

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
FAULT – continued.							
FLT delay duration	t_{DFLT}	f_{SW} = 100 kHz	-55°C to +125°C	01,02,	140	169	µs
				03,04	152 typical		
		f_{SW} = 200 kHz			66	86	
					78 typical		
		f_{SW} = 1 MHz			14	21	
					17 typical		
		f_{SW} = 2 MHz			7	14	
					11 typical		
THERMAL SHUTDOWN							
Thermal shutdown			-55°C to +125°C	01,02,	165	185	°C
				03,04	175 typical		
Thermal shutdown hysteresis			-55°C to +125°C	01,02,	10	20	°C
				03,04	15 typical		
PRIMARY AND SYNCHRONOUS RECTIFIER OUTPUTS							
Low level threshold voltage		I_{SINK} = 10 mA	-55°C to +125°C	01,02, 03,04	0.5 typical		V
High level threshold voltage		I_{SOURCE} = 10 mA	-55°C to +125°C	01,02, 03,04	4.5 typical		V
Rise and fall time		R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF,	-55°C to +125°C	01,02,		17	ns
		10% to 90%		03,04	10 typical		
Output source resistance	R_{SRC_P}	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	01,02, 03,04	15 typical		Ω
Output sink resistance	R_{SINK_P}	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	01,02, 03,04	15 typical		Ω

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
MINIMUM ON TIME AND DEAD TIME							
Minimum on time	t_{MIN}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	01		85	ns
Primary off to secondary on dead time	TD_{PS}	PS = floating, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	-55°C to +125°C	01	5	11	ns
					8 typical		
		PS = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating			43	55	
					50 typical		
		PS = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating			85	110	
					100 typical		
Secondary off to primary on dead time	TD_{SP}	SP = floating, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	-55°C to +125°C	01	5	11	ns
					8 typical		
		SP = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating			43	55	
					50 typical		
		SP = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating			85	110	
					100 typical		
LEADING EDGE BLANK TIME AND DUTY CYCLE							
Leading edge blank time	T_{LEB}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	01	12	19	ns
					15 typical		
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V			45	55	
					50 typical		
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V			85	110	
					100 typical		
Maximum duty cycle	D_{MAX}	DCL = AVSS	-55°C to +125°C	01	45	50	%
					48 typical		
		DCL = floating, clock duty cycle = 50%			70	80	
					75 typical		
		DCL = VLDO				100	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
MINIMUM ON TIME AND DEAD TIM E							
Minimum on time	t_{MIN}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	02		85	ns
Primary off to secondary on dead time	TD_{PS}	PS = floating, 5 V ≤ VIN ≤ 14 V, 90 % of OUTx falling to 10% of SRx rising, OUTx and SRx floating	-55°C to +125°C	02	5	11	ns
					8 typical		
		PS = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating			43	55	
					50 typical		
		PS = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90 % of OUTx falling to 10% of SRx rising, OUTx and SRx floating			85	110	
					100 typical		
Secondary off to primary on dead time	TD_{SP}	SP = floating, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	-55°C to +125°C	02	5	11	ns
					8 typical		
		SP = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating			43	55	
					50 typical		
		SP = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating			85	110	
					100 typical		
LEADING EDGE BLANKTIME AND DUTY CYCLE							
Leading edge blank time	T_{LEB}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	02	12	19	ns
					15 typical		
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V			45	55	
					50 typical		
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V			85	110	
					100 typical		
Maximum duty cycle	D_{MAX}	DCL = floating, clock duty cycle = 50%	-55°C to +125°C	02	70	80	%
					75 typical		
		DCL = VLDO				100	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions VIN = 4 V to 14 V, unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
MINIMUM ON TIME AND DEAD TIME							
Minimum on-time	t_{MIN}	5 V ≤ VIN ≤ 14 V	-55°C to +125°C	03		115	ns
Primary off to secondary on dead time	TD_{PS}	5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	-55°C to +125°C	03	40	60	ns
					50 typical		
Secondary off to primary on dead time	TD_{SP}	5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	-55°C to +125°C	03	40	60	ns
					50 typical		
LEADING EDGE BLANK TIME AND DUTY CYCLE							
Leading edge blank time	T_{LEB}	5 V ≤ VIN ≤ 14 V	-55°C to +125°C	03	40	60	ns
					50 typical		
Maximum duty cycle	D_{MAX}	DCL = floating, clock duty cycle = 50%	-55°C to +125°C	03	70	80	%
					75 typical		
		DCL = VLDO				100	
MINIMUM ON TIME AND DEAD TIME							
Minimum on-time	t_{MIN}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	04		85	ns
Leading edge blank time	T_{LEB}	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	-55°C to +125°C	04	12	19	ns
					15 typical		
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V			45	55	
					50 typical		
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V			85	110	
					100 typical		
Maximum duty cycle	D_{MAX}	DCL = AVSS	-55°C to +125°C	04	45	50	%
					48 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Device types 01-04 supplied to this drawing have been total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A to TID level of 50 krads(Si). Post irradiation electrical parametric limits falls within the specification limits during electrical measurement. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 50 krads(Si).

3/ Bench verified. Not tested in production.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP/SEE	Temperature (T_C)	V_{IN}	Effective linear energy transfer (LET)
01,02,03,04	No SEL	+125°C	14 V	$\leq$ 43 MeV/(mg/cm^2)
01,02,03,04	No SEB nor SEGR	+25°C	14 V	$\leq$ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEP test results, customers are requested to contact the manufacturer.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for all device types and as specified in 1.6 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° $\leq$ angle $\leq$ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C $\pm$10% for SEL.

f. For SEP test limits, see table IB herein.

Case X

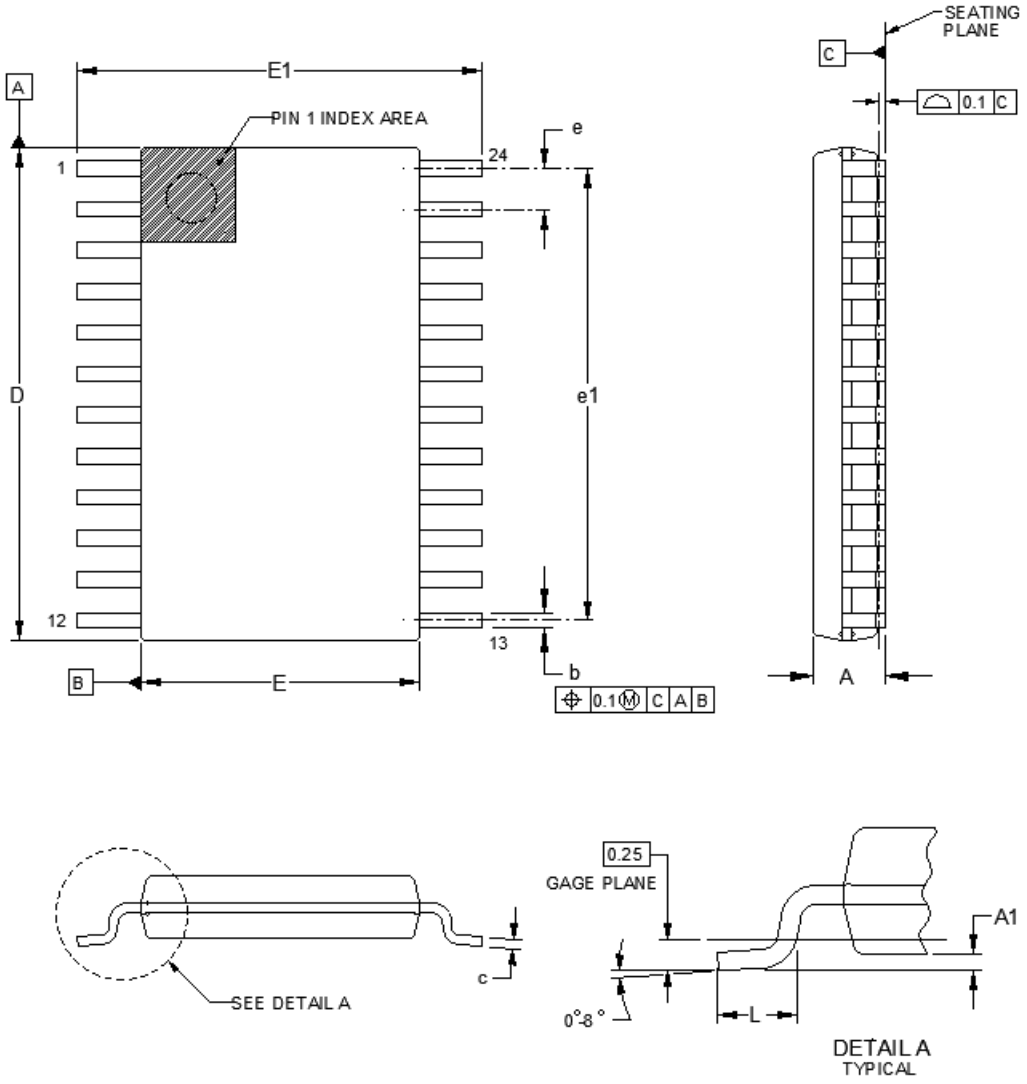


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/22607
		REV	PAGE 15

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.2
A1	.002	.006	0.05	0.15
b	.007	.012	0.19	0.30
c	.006 TYP		0.15 TYP	
D	.303	.311	7.7	7.9
E	.169	.177	4.3	4.5
E1	.244	.260	6.2	6.6
e	.025 BSC		0.65 BSC	
e1	.281 BSC		7.15 BSC	
L	.020	.029	0.50	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. Dimension E does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.0098 inch) per side.
4. Falls within reference to JEDEC MO-153.

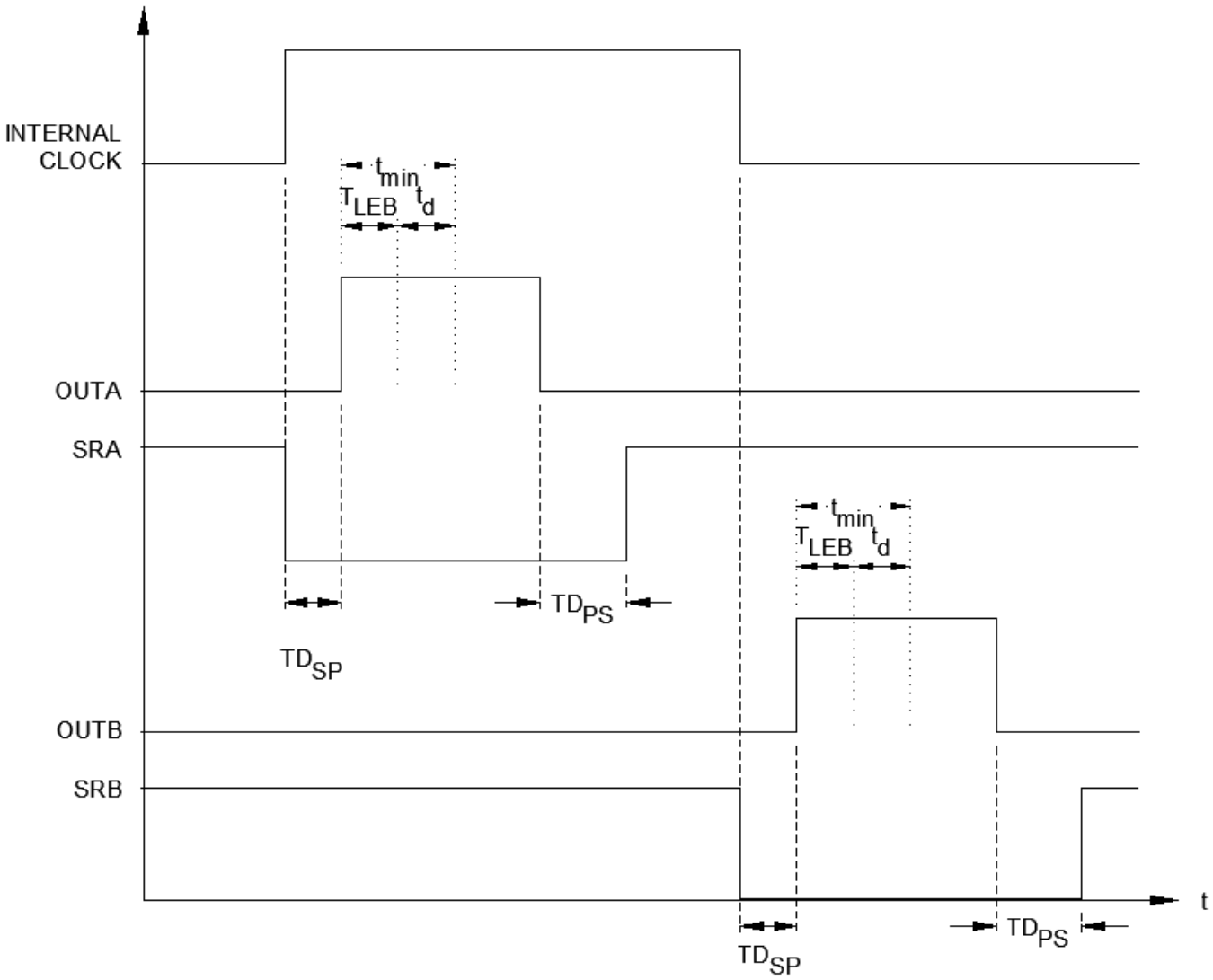
FIGURE 1. Case outline - Continued.

Case outline	X					
Terminal symbol	Device type 01	Device type 02	Device type 03	Device type 04	I/O	Description
	Terminal number					
RT	1	1	1	1	I/O	In internal oscillation mode, the RT pin must be populated with a resistor to AVSS. When the RT pin is floating, a 200 kHz to 4 MHz external clock is required at the SYNC pin. The frequency of the external clock must be twice the desired switching frequency.
PS	2	2	---	---	I/O	Primary off to synchronous rectifier on dead time set. Programmable through an external resistor to AVSS.
SP	3	3	---	---	I/O	Synchronous rectifier off to primary on dead time set. Programmable through an external resistor to AVSS.
LEB	4	4	---	4	I/O	Leading edge blank time set. Programmable through an external resistor to AVSS.
HICC	5	5	5	5	I/O	Cycle by cycle current limit time delay and hiccup time setting. Delay time and hiccup time determined by capacitor from HICC to AVSS. Connecting this pin to AVSS disables hiccup mode.
SYNC	6	6	6	6	I/O	When the RT pin is floating, SYNC is configured as an input for a 200 kHz to 4 MHz external clock. In this case, the external clock input gets inverted and the system clock will run at half the frequency of the external clock input. When the RT pin is populated with a resistor to AVSS, SYNC outputs a 200 kHz to 4 MHz clock signal at twice the device switching frequency in phase with the switching of the device.
DCL	7	7	7	7	I/O	Duty cycle limit configurability. For device type 01, connect to AVSS for 50% duty cycle limit, floating for 75%, and VLDO for 100%. For device type 02 and device type 03, the DCL pin can be left floating or connected to VLDO to set the maximum duty cycle to 75% or 100%, respectively. For device type 04, this pin must be connected to AVSS in order to obtain the 50% maximum duty cycle.
EN	8	8	8	8	I	Connecting the EN pin to the VLDO pin or external source greater than 0.6 V enables the device. In addition, input undervoltage lockout (UVLO) can be adjusted with two resistors.
VIN	9	9	9	9	I	Input supply to the device. Input voltage range is from 4 V to 14 V.
OUTA	10	10	10	10	O	Primary switching output A.

FIGURE 2. Terminal connections.

Case outline	X					
Terminal symbol	Device type 01	Device type 02	Device type 03	Device type 04	I/O	Description
	Terminal number					
OUTB	11	---	---	11	O	Primary switching output B. Active only when DCL = AVSS.
NC	12,13	11,12, 13,14	2,3,4, 11,12, 13,14	2,3, 12,13, 14,15	---	No connect.
SRB	14	---	---	---	O	Synchronous rectifier output B. Active only when DCL = AVSS.
SRA	15	15	15	---	O	Synchronous rectifier output A.
AVSS	16	16	16	16	---	Ground of the device.
VLDO	17	17	17	17	O	Output of internal regulator. Requires at least 1 µF external capacitor to AVSS.
CS_ILIM	18	18	18	18	I/O	Current sense for PWM control and cycle by cycle overcurrent protection. An input voltage over 1.05 V on CS_ILIM will trigger an overcurrent in the PWM controller.
FAULT	19	19	19	19	I	Fault protection pin. When the rising threshold of the FAULT pin is exceeded, the outputs will stop switching. After the external voltage drops below the falling threshold, the device will restart after a set delay. Connect this pin to AVSS to disable FAULT.
REFCAP	20	20	20	20	O	1.2 V internal reference. Requires a 470 nF external capacitor to AVSS.
RSC	21	21	21	21	I/O	A resistor from RSC to AVSS sets the desired slope compensation.
SS	22	22	22	22	I/O	Soft start. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
VSENSE	23	23	23	23	I	Inverting input of the error amplifier.
COMP	24	24	24	24	I/O	Error amplifier output. Connect frequency compensation to this pin.

FIGURE 2. Terminal connections - Continued.



NOTE: OUTB and SRB waveforms are only applicable for device type 01.

FIGURE 3. Outputs timing waveforms.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/22607-01XE	01295	Small tape and reel, 250 units	7H5005PW	TPS7H5005MPWTSEP
V62/22607-02XE	01295	Small tape and reel, 250 units	7H5006PW	TPS7H5006MPWTSEP
V62/22607-03XE	01295	Small tape and reel, 250 units	7H5007PW	TPS7H5007MPWTSEP
V62/22607-04XE	01295	Small tape and reel, 250 units	7H5008PW	TPS7H5008MPWTSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243