REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 21-12-16	**CHECKED BY** RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, -16.5 V, 1 A, NEGATIVE VOLTAGE LINEAR REGULATOR, MONOLITHIC SILICON
	APPROVED BY JAMES R. ESCHMEYER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/21616**
	REV	**PAGE** 1 **OF** 15

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AMSC N/A

5962-V081-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance -16.5 V, 1 amp, negative voltage linear regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7H1210-SEP	Radiation hardened -16.5 V, 1 amp, negative voltage linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	See figure 1	Plastic leadless quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage:	
IN to GND	-35 V to 0.3 V
FB to GND	-2 V to 0.3 V
FB to IN	-0.3 V to 35 V
EN to GND	-35 V to 10 V
NR_SS to IN	-0.3 V to 35 V
NR_SS to GND	-2 V to 0.3 V
Output voltage:	
OUT to GND	-33 V to 0.3 V
OUT to IN	-0.3 V to 35 V
Output current (peak output)	Internally limited
Operating virtual junction temperature range (T_J)	-55°C to +150°C
Storage temperature range (T_{stg})	-65°C to +150°C
Electrostatic discharge (ESD) rating:	
Human body model (HDM), per JEDEC JS-001, all pins	±1000 V 2/
Charge device model (CDM), per JEDEC specification JESD22-C101, all pins	±500 V 3/

1.4 Recommended operating conditions. 4/

Input voltage:	
IN	-16.5 V to -3 V
FN	V_{IN} to 10 V
Output voltage (OUT)	-15.5 V to V_{REF} 5
Output current (OUT)	0 A to 1 A 6/
Lower feedback resistor (R_{FB-BOT})	240 kΩ maximum 7/
Input capacitance (C_{IN})	10 µF minimum
Output capacitance (C_{OUT})	10 µF minimum 47 µF nominal
Noise reduction capacitor (C_{NR_SS})	100 nF nominal
Operating junction temperature range (T_J)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ The minimum dropout voltage must also be met.
6/ To ensure stability at no load conditions, a current from the feedback resistive network greater than or equal to 5 µA is required.
7/ This condition helps ensure stability at no load.

1.5 Radiation features.

Maximum total dose available (high dose rate = 50-300 rad(Si)/s) ..... 20 krads(Si) 8/
Maximum total dose available (low dose rate ≤ 10 mrads(Si)/s) ..... 20 krads(Si) 8/

Single event phenomenon (SEP):
No Single event latchup (SEL) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 9/
No Single event burn out (SEB) observes at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 9/
No Single event gate rupture (SEGR) observes at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 9/

1.6 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	$R\theta_{JA}$	32.7	°C/W
Thermal resistance, junction-to-case (top)	$R\theta_{JC(TOP)}$	24	°C/W
Thermal resistance, junction-to-board	$R\theta_{JB}$	11.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.3	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	11.7	°C/W
Thermal resistance, junction-to-case (bottom)	$R\theta_{JC(bot)}$	3.6	°C/W

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 – Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

8/ Device type 01 supplied to this drawing has been performed total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A and condition D to TID level of 30 krads(Si. Post irradiation electrical parametric limits falls within the specified limits during electrical measurement. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 20 krads(Si).

9/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver(Ag) ion beam was used at an angle of incidence of 0^o at flux of 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) or single event burnout (SEB) or single event gate rupture (SEGR) were observed at an effective LET of 43 MeV/(mg/cm^2) under certain test conditions. For more information on SEE/SEP test please contact device manufacturer.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192	–	Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD 57	–	Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supplies and currents							
Undervoltage lockout threshold	V_{UVLO}		-55°C to +125°C	01	-2 typical		V
Dropout voltage	$\|V_{DO}\|$	I_{OUT} = 0.5 A, V_{IN} = -4.6 V, $V_{OUT(set)}$ = -5 V, C_{IN} = 30 µF, $\|V_{DO}\| = \|V_{IN} - V_{OUT(measured)}\|$	-55°C to +125°C	01		325	mV
					224 typical		
		I_{OUT} = 1 A, V_{IN} = -4.6 V, $V_{OUT(set)}$ = -5 V, C_{IN} = 30 µF, $\|V_{DO}\| = \|V_{IN} - V_{OUT(measured)}\|$	+25°C			450	
					363 typical		
			-55°C to +125°C			500	
					363 typical		
Current limit	I_{CL}	V_{IN} = -6 V, $V_{OUT(SET)}$ = -5 V, $V_{OUT(forced)}$ = -4.5 V	-55°C to +125°C	01	2.9 typical		A
Quiescent current	I_Q	V_{EN} = 3 V, I_{OUT} = 0 A	-55°C to +125°C	01		350	µA
					210 typical		
Ground current 5/	I_{GND}	V_{EN} = 3 V, I_{OUT} = 0.5 A	-55°C to +125°C	01		10	mA
					5 typical		
Shutdown current	$\|I_{SHDN}\|$	V_{EN} = 0.4 V	-55°C to +125°C	01		3	µA
					1 typical		
		V_{EN} = -0.4 V				3	
					1 typical		
Feedback leakage 6/ current	$I_{FB(LKG)}$		-55°C to +125°C	01		75	nA
					14 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Accuracy							
Reference voltage	V_{REF}	$V_{FB} = V_{REF}$	-55°C to +125°C	01	-1.199	-1.164	V
					-1.182 typical		
Output voltage accuracy	V_{ACC}	$\|V_{IN}\| = 3$ V, 1 mA ≤ I_{OUT} ≤ 1 A	-55°C to +125°C	01	-2%	2%	
					±1% typical		
		$\|V_{IN}\| = 16.5$ V, 1 mA ≤ I_{OUT} ≤ 100 mA			-2%	2%	
					±1% typical		
		$\|V_{IN}\| = 16.5$ V, $\|V_{OUT}\| = 15.5$ V, $I_{OUT} = 1$ A			-2%	2%	
					±1% typical		
Line regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3 V ≤ $\|V_{IN}\|$ ≤ 16.5 V	-55°C to +125°C	01	-0.007% typical		V_{OUT}/V
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	1 mA ≤ I_{OUT} ≤ 1 A	-55°C to +125°C	01	-0.5% typical		V_{OUT}/A
Enable							
Enable turn-on (positive logic)	$V_{EN(+HI)}$		-55°C to +125°C	01	2	10	V
Enable turn-on (negative logic)	$V_{EN(-HI)}$	$V_{IN} = -16.5$ V	-55°C to +125°C	01	V_{IN}	-2	V
Enable turn-off (positive logic)	$V_{EN(+LO)}$		-55°C to +125°C	01	0	0.4	V
Enable turn-off (negative logic)	$V_{EN(-LO)}$		-55°C to +125°C	01	-0.4	0	V
Enable current	$\|I_{EN}\|$	$V_{IN} = V_{EN} = -3$ V	-55°C to +125°C	01		1	µA
					0.48 typical		
		$V_{IN} = V_{EN} = -16.5$ V				1	
					0.51 typical		
		$V_{IN} = -16.5$ V, $V_{EN} = 10$ V				1	
					0.5 typical		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Enable – continued.							
Thermal shutdown enter temperature	$T_{SD(enter)}$			01	178 typical		°C
Thermal shutdown exit temperature	$T_{SD(exit)}$			01	152 typical		°C
Noise and Temperature							
Power supply rejection ratio	PSRR	V_{IN} = -6 V, V_{OUT} = -5 V, 7/ C_{OUT} = 50.11 µF, C_{NR_SS} = 100 nF, f = 100 Hz	-55°C to +125°C	01	61		dB
		V_{IN} = -6 V, V_{OUT} = -5 V, 7/ C_{OUT} = 50.11 µF, C_{NR_SS} = 100 nF, f = 100 kHz			61		
		V_{IN} = -6 V, V_{OUT} = -5 V, 7/ C_{OUT} = 50.11 µF, C_{NR_SS} = 100 nF, f = 1 MHz			41		
Output noise rms voltage (Bandwidth from 10 Hz to 100 kHz)	V_N	V_{IN} = -3 V, $V_{OUT(nom)} = V_{REF}$, C_{IN} = 11.1 µF, C_{OUT} = 50.11 µF, C_{NR_SS} = 100 nF, I_{OUT} = 1 A	-55°C to +125°C	01	13.7 typical		µVRMS

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, over operating temperature range T_J = -55°C to +125°C, $|V_{IN}|$ = 3 V, I_{OUT} = 1 mA, C_{IN} = 20 µF, C_{OUT} = 20 µF, C_{NR_SS} = 0 nF, FB tied to OUT, EN tied to IN.

3/ At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(nom)} \leq V_{REF} \leq 0$ V; at regulation, $V_{IN} \leq V_{OUT(nom)} - |V_{DO}|$; $I_{OUT} > 0$ flows from OUT to IN.

4/ Device type 01 supplied to this drawing has been characterized at 30 krads(Si) of irradiation. However, this device's radiation end point limits for the noted parameters are guaranteed to TID level 20 krads(Si) as specified in MIL-STD-883, method 1019, condition D. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

5/ $I_{GND} = I_{IN} - I_{OUT}$.

6/ $I_{FB} > 0$ flows into the device.

7/ C_{IN} is removed as part of PSRR testing. During normal operation, follow the recommended operating condition of $C_{IN} \geq 10$ µF.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_C)	V_{IN}	Effective linear energy transfer (LET)
01	No SEL	+125°C	-16.5 V	≤ 43 MeV/(mg/cm^2)
	No SEB	+125°C	-16.5 V	≤ 43 MeV/(mg/cm^2)
	No SEGR	+125°C	-16.5 V	≤ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver(Ag) ion beam was used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) or single event burnout (SEB) or single event gate rupture (SEGR) were observed at an effective LET of 43 MeV/(mg/cm^2) under certain test conditions. SEE test shall be perform in accordance with JESD57. For more information on SEE/SEP test please contact device manufacturer.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D for device type 01 and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10%.

f. For SEL test limits, see table IB herein.

g. For SET test limits, see table IB herein.

h. For SEFI test limits, see table IB herein.

Case X

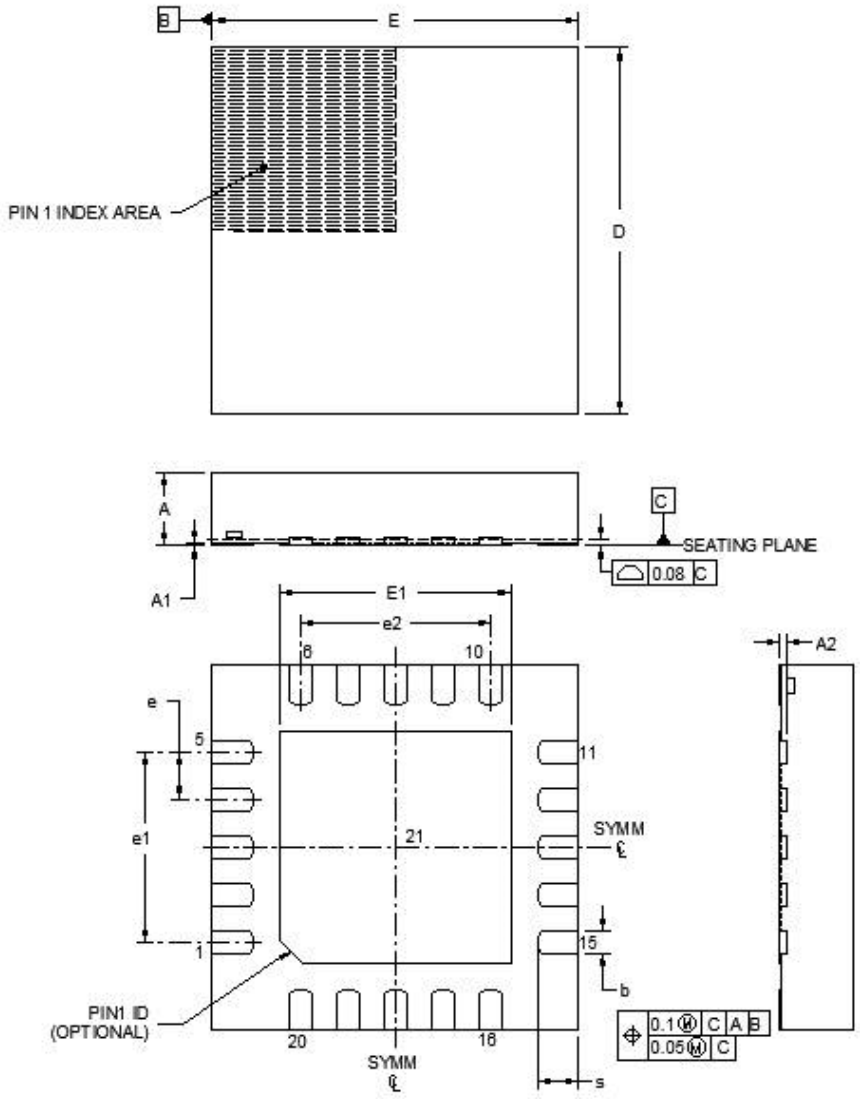

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/21616
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Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.040	---	1.00
A1	.000	.002	0.00	0.05
A2	.004 TYP		0.10 TYP	
b	.010	.014	0.26	0.36
D	.193	.201	4.90	5.10
E	.193	.201	4.90	5.10
E1	.124	.124	3.14	3.16
e	.025 BSC		0.65 BSC	
e1	.102 BSC		2.60 BSC	
e2	.102 BSC		2.60 BSC	
s	.010	.014	0.26	0.36

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

FIGURE 1. Case outline - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O SEE NOTE	Description
1	OUT	O	Output of the regulator. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to ensure stability. The manufacturer recommends connecting a 47 µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize AC performance.
2	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
3	FB	I	Feedback. This pin is the input to the control loop error amplifier. It is used to set the output voltage of the device and is normally equal to V_{REF}, -1.182 V (typical), during operation.
4	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
5	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
6	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
7	GND	---	Ground.
8	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
9	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.

See note at end of table.

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O SEE NOTE	Description
10	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
11	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
12	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
13	EN	I	Enable. This dual polarity pin turns the regulator on when $\|V_{EN}\| \geq 2$ V. The EN pin can be connected to IN if not used. If V_{EN} is negative polarity then $\|V_{EN}\| \leq \|V_{IN}\|$.
14	NR_SS	---	Noise reduction and soft start. A capacitor connected from this pin to GND, controls the soft start function and allows RMS noise to be reduced to very low levels. The manufacturer recommends connecting a 100 nF capacitor from NR_SS to GND (as close to the device as possible) to filter the noise generated by the internal band gap and maximize AC performance.
15	IN	I	Input supply. It is recommended to connect a 10 μF capacitor from IN to GND (as close to the device as possible).
16	IN	I	Input supply. It is recommended to connect a 10 μF capacitor from IN to GND (as close to the device as possible).
17	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
18	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.

See Note at end of table.

FIGURE 2. Terminal connections - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O SEE NOTE	Description
19	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
20	OUT	O	Output of the regulator. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to ensure stability. The manufacturer recommends connecting a 47 µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
Thermal pad	---	---	Connect the thermal pad to a large area ground plane. The thermal pad is not internally grounded and it must be externally tied to GND for proper operations.

NOTE: I = Input, O = Output, I/O = Input/Output.

FIGURE 2. Terminal connections - continued.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

c. Number of transients (SET).

d. Number of functional interrupts (SEFI).

e. See Table IB for SEP test conditions.

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21616-01XE	01295	Tube, 20 units	7H1210	TPS7H1210MRGWSEP 2/
		Reel, 250 units	7H1210	TPS7H1210MRGWTSEP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ This device has been RHA TID tested to 20 krads(Si) (see paragraph 1.5 herein).

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243