

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add 02 device type. Update boilerplate paragraphs to current VID description requirements. - DRH	22-11-29	Muhammad A. Akbar



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

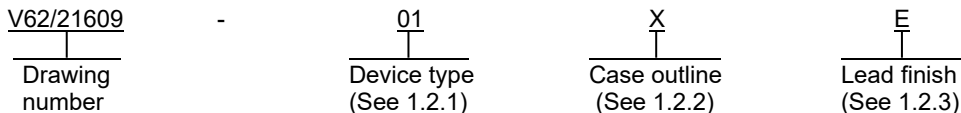
REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A Original date of drawing 22-01-26	PREPARED BY Donald R. Hohe		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime																	
	CHECKED BY Donald R. Hohe		TITLE MICROCIRCUIT, LINEAR BiCMOS, 7-V, 18-A SYNCHRONOUS BUCK CONVERTER, RADIATION-TOLERANT, MONOLITHIC SILICON																	
	APPROVED BY Muhammad A. Akbar		DWG NO. V62/21609																	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Radiation-tolerant 7-V, 18-A Synchronous Buck Converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS7H4003 –SEP	Radiation-tolerant 7-V, 18-A Synchronous Buck Converter
02	TPS7H4001 –SHP	Radiation-Hardness-Assured 3-V to 7-V Input 18-A Synchronous Buck Converter

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	44	Plastic small outline package with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

- 1/ Device type 02 (TPS7H4001 –SHP) production screening has two additional steps:
- A. Temperature cycle flow of 20 cycles from -55°C to 125°C.
 - B. Burn in of 240 hours at 125°C.

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1.3 Absolute maximum ratings. 2/

Input voltages:	
VIN, PVIN, EN	-0.3 V to 7.5 V
RSC, VSENSE, COMP	-0.3 V to 3.3 V
PWRGD	-0.3 V to 7.5 V
SS/TR, RT	-0.3 V to 3.3 V
SYNC1, SYNC2	-0.3 V to 7.5 V
Output voltages:	
REFCAP	-0.3 V to 3.3 V
PH	-1 V to 7.5 V
PH 10-ns transient	-3 V to 7.5 V
Voltage differential: GND to exposed thermal pad	-0.2 V to 0.2 V
Source current:	
PH	Current limit A
RT	±100 µA
Sink current:	
PH, PVIN	Current limit A
COMP	±200 µA
PWRGD	-0.1 mA to 5 mA
Operating junction temperature	-55°C to 150°C
Storage temperature, T _{stg}	-65°C to 150°C
ESD ratings:	
Human body model (HBM) , all pins	±2000 V <u>3/</u> <u>4/</u>
Charged device model (CDM), all pins	±1000 V <u>5/</u> <u>6/</u>

1.4 Recommended operating conditions.

Maximum switching current, I _{OUT}	18 A
Junction operating temperature, T _J	-55°C to 125°C
Thermal characteristics:	
Junction to ambient thermal resistance, R _{θJA}	23.7 °C/W
Junction to case (top) thermal resistance, R _{θJctop}	12.4 °C/W
Junction to board thermal resistance, R _{θJB}	6.8 °C/W
Junction to top characterization parameter, Ψ _{JT}	0.2 °C/W
Junction to board characterization parameter, Ψ _{JB}	6.7 °C/W
Junction to case (bottom) thermal resistance, R _{θJcbot}	1.2 °C/W

- 2/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 3/ HBM ESD tested per ANSI/ESDA/JEDEC JS-001.
- 4/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- 5/ CDM ESD tested per ANSI/ESDA/JEDEC JS-002.
- 6/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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1.5 Radiation features.

For device type 01:

- Maximum total ionizing does (TID) available (dose rate=50-300 rad/s (Si)) 50 krad (Si) 7/
- Maximum total ionizing does (TID) available (LDR dose rate= 10mrads/s(Si0)) 50 krad (Si) 7/
- Heavy ion single event phenomenon (SEP) test:
 - No SEL occurs at effective LET (see 4.3) ≤ 43 MeV/(mg/cm²) 8/
 - No SEB observe at effective LET (see 4.3) ≤ 43 MeV/(mg/cm²) 8/
 - No SEGR observe at effective LET (see 4.3) ≤ 43 MeV/(mg/cm²) 8/

For device type 02:

- Maximum total ionizing does (TID) available (dose rate=50-300 rad/s (Si)) 100 krad (Si) 7/
- Heavy ion single event phenomenon (SEP) test:
 - No SEL occurs at effective LET (see 4.3) ≤ 75 MeV/(mg/cm²) 8/
 - No SEB observe at effective LET (see 4.3) ≤ 75 MeV/(mg/cm²) 8/
 - No SEGR observe at effective LET (see 4.3) ≤ 75 MeV/(mg/cm²) 8/

2.0 APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

ASTM INTERNATIONAL (ASTM)

- ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at <https://www.astm.org/>.)

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC JEP155 – Recommended ESD target levels for HBM/MM qualification.
- JEDEC JEP157 – Recommended ESD-CDM target levels.
- JEDEC JS-001 – Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Human Body Model (HBM)
- JEDEC JS-002 – Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Charged Device Model (CDM)
- JEDEC JESD57 – Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Radiation.

(Copies of these documents are available online at <https://www.jedec.org/>.)

7/ Device types supplied to this drawing has been performed total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A and condition D to TID level of 50 krad(Si) for device type 01. Manufacturer also performed RLAT test at high dose rate condition A to TID level of 100 krad(Si) for device type 02. Post irradiation electrical parametric limits falls within the spec limits during electrical measurement. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D as specified herein section 1.5. For more information on TID test for device types 01 and 02, please contact device manufacturer.

8/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver(Ag) ion beam was used at an angle of incidence of 0° at flux of 10⁵ ions/cm² s, fluence level of 10⁷ ions/cm². After the runs, no single event latch-up (SEL) or Single event Burnout (SEB) or Single event gate rupture (SEGR) were observed at an effective LET of 43 MeV/(mg/cm²) for device type 01 and 75 MeV/(mg/cm²) for device type 02 under certain test conditions. For more information on SEE/SEP test please contact device manufacturer.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal functions. The terminal functions shall be as shown in figure 3.

3.5.4 Simplified schematic. The simplified schematic shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 RT versus frequency. RT versus frequency shall be as shown in figure 6.

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TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit	
			Min	Typ	Max		
SUPPLY VOLTAGE (VIN AND PVIN PINS)							
PVIN operating input voltage			3.0		7.0	V	
PVIN internal UVLO threshold		PVIN rising	2.425	2.50	2.575	V	
PVIN internal UVLO hysteresis		Load = 0 A	425	450	475	mV	
VIN operating input voltage			3.0		7.0	V	
VIN internal UVLO threshold		VIN rising	2.71	2.75	2.80	V	
VIN internal UVLO hysteresis			134	150	178	mV	
VIN shutdown supply current		V _{EN} = 0 V		2.32	2.85	mA	
VIN operating – non switching supply current		V _{SENSE} = V _{BG}		4	6	mA	
ENABLE AND UVLO (EN PIN)							
Enable threshold		Rising	1.110	1.14	1.172	V	
		Falling	1.080	1.11	1.148		
Input current		V _{EN} = 1.1 V	4.8	6.1	7.6	μA	
Hysteresis current		V _{EN} = 1.3 V	2.4	3.0	3.9	μA	
VOLTAGE REFERENCE							
Internal voltage reference initial tolerance		0 A ≤ IO _{UT} ≤ 18 A, 25°C	0.598	0.605	0.613	V	
Internal voltage reference		0 A ≤ IO _{UT} ≤ 18 A	-55°C	0.594	0.602	0.609	V
			-40°C	0.596	0.602	0.608	
			85°C	0.600	0.606	0.613	
			125°C	0.599	0.607	0.614	
REFCAP voltage		REFCAP = 470 nF	1.189	1.209	1.228	V	
MOSFET							
High-side switch resistance 3/		PVIN = VIN = 3 V, lead length = 3 mm	-55°C		16	18	mΩ
			25°C		19	21	
			125°C		23	27	
		PVIN = VIN = 5 V, lead length = 3 mm	-55°C		14	16	
			25°C		17	19	
			125°C		20	23	
		PVIN = VIN = 7 V, lead length = 3 mm 5/	-55°C		13	15	
			25°C		15	18	
			125°C		19	22	
Low-side switch resistance 3/		PVIN = VIN = 3 V, lead length = 3 mm	-55°C		7	11	mΩ
			25°C		9	12	
			125°C		13	17	
		PVIN = VIN = 5 V, lead length = 3 mm	-55°C		6	10	
			25°C		9	11	
			125°C		12	15	

See footnote at end of table.

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TABLE IA. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions <u>2/</u>	Limits			Unit	
			Min	Typ	Max		
MOSFET - continued							
Low-side switch resistance <u>3/</u>		PVIN = VIN = 7 V, lead length = 3 mm <u>5/</u>	-55°C		5	9	mΩ
			25°C		8	10	
			125°C		11	14	
ERROR AMPLIFIER							
Error amplifier input offset voltage		VSENSE = 0.6 V		-2		2.55	mV
VSENSE pin input current		VSENSE = 0.6 V		-15		15	nA
Error amplifier transconductance	gm	-2 μA < ICOMP < 2 μA, V(COMP) = 1V		1150	1800	2400	μS
Error amplifier DC gain <u>4/</u>		VSENSE = 0.6 V			10000		V/V
Error amplifier source		V(COMP) = 1 V,		100	140	190	μA
Error amplifier sink		100-mV input overdrive		100	140	190	μA
Error amplifier output resistance					7		MΩ
COMP to Iswitch gm <u>5/</u>		COMP = 0.5 V	-55°C	28	38	49	S
			25°C	29	40	50	
			125°C	30	41	52	
OVERCURRENT PROTECTION							
High-side switch current limit threshold <u>5/</u>		VIN = 7 V			27	34	A
Low-side switch sourcing overcurrent threshold <u>5/</u>		VIN = 7 V			25	32	A
Low-side switch sinking overcurrent threshold <u>5/</u>		VIN = 7 V	3.5	6			A
SLOPE COMPENSATION							
Slope compensation <u>6/</u>		fsw = 100 kHz, RSC = 1.1 MΩ		-1.2			A/μs
		fsw = 500 kHz, RSC = 196 kΩ		-6.0			
		fsw = 1000 kHz, RSC = 80.6 kΩ		-16.0			
THERMAL SHUTDOWN							
Thermal shutdown					190		°C
Thermal shutdown hysteresis					18		°C
INTERNAL SWITCHING FREQUENCY							
Internally set frequency		RT = Open	VIN = 3 V	444	473	515	kHz
			VIN = 5 V	449	502	560	
Externally set frequency		RT = 1.07 MΩ (1%)	VIN = 3 V	80	98	125	kHz
			VIN = 5 V	80	100	125	
	RT = 165 kΩ (1%)	VIN = 3 V	455	495	535		
		VIN = 5 V	475	523	615		
	RT = 73.2 kΩ (1%)	VIN = 3 V	689	850	1011		
		VIN = 5 V	760	986	1212		

See footnote at end of table.

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TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
EXTERNAL SYNCHRONIZATION						
SYNC1/SYNC2 out low-to-high rise time (10%/90%)		Cl _{oad} = 25 pF		70	180	ns
SYNC1/SYNC2 out high-to-low fall time (90%/10%)		Cl _{oad} = 25 pF		10	21	ns
SYNC2 TO SYNC1 rising edge phase shift			77	85	94	°
SYNC1 falling edge delay 5/			165	180	185	°
SYNC1/SYNC2 out high level threshold		I _{OH} = 50 μA	VIN-0.3			V
SYNC1/SYNC2 out low level threshold		I _{OH} = 50 μA			600	mV
SYNC1/SYNC2 in low level threshold		PVIN = VIN = 3 V			800	mV
		PVIN = VIN = 5 V			800	
		PVIN = VIN = 7 V 5/			800	
SYNC1/SYNC2 in high level threshold		PVIN = VIN = 3 V	2.25			V
		PVIN = VIN = 5 V	3.5			
		PVIN = VIN = 7 V 5/	4.9			
SYNC1 in frequency range		PVIN = VIN = 5 V	100		1000	kHz
SYNC1 in duty cycle range		Duty cycle of external clock	40		60	%
PH (PH PIN)						
Minimum on time		Measured at 10% to 90% of VIN, I _{PH} = 2 A, VIN = 3 V		190	235	ns
		Measured at 10% to 90% of VIN, I _{PH} = 2 A, VIN = 5 V		190	225	
SOFT START AND TRACKING (SS/TR PIN)						
SS charge current			1.5	2.5	3	μA
SS/TR to VSENSE matching 5/		V _(SS/TR) = 0.3 V		30	90	mV
POWER GOOD (PWRGD PIN)						
VSENSE threshold		VSENSE falling (fault)	90	91		%VREF
		VSENSE rising (good)		94	97	
		VSENSE rising (fault)		109	111	
		VSENSE falling (good)	103	106		
Output high leakage		VSENSE = VREF, V _(PWRGD) = 5 V		30	181	nA
Output low		I _(PWRGD) = 2 mA			0.3	V
Minimum VIN for valid output		V _(PWRGD) < 0.5 V at 100 μA		0.6	1	V
Minimum SS/TR voltage for PWRGD					1.1	V

See footnote at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, junction operating temperature (T_j) = -55°C to $+125^{\circ}\text{C}$, $V_{IN} = P_{VIN} = 3\text{ V}$ to 7 V .
- 3/ Measured at pins.
- 4/ Ensured by design only. Not tested in production.
- 5/ Bench verified. Not tested in production.
- 6/ Example values are shown in the table. Actual values are application specific. Please refer to manufacturer datasheet for information on selecting the slope compensation (SC) and RSC resistor value.

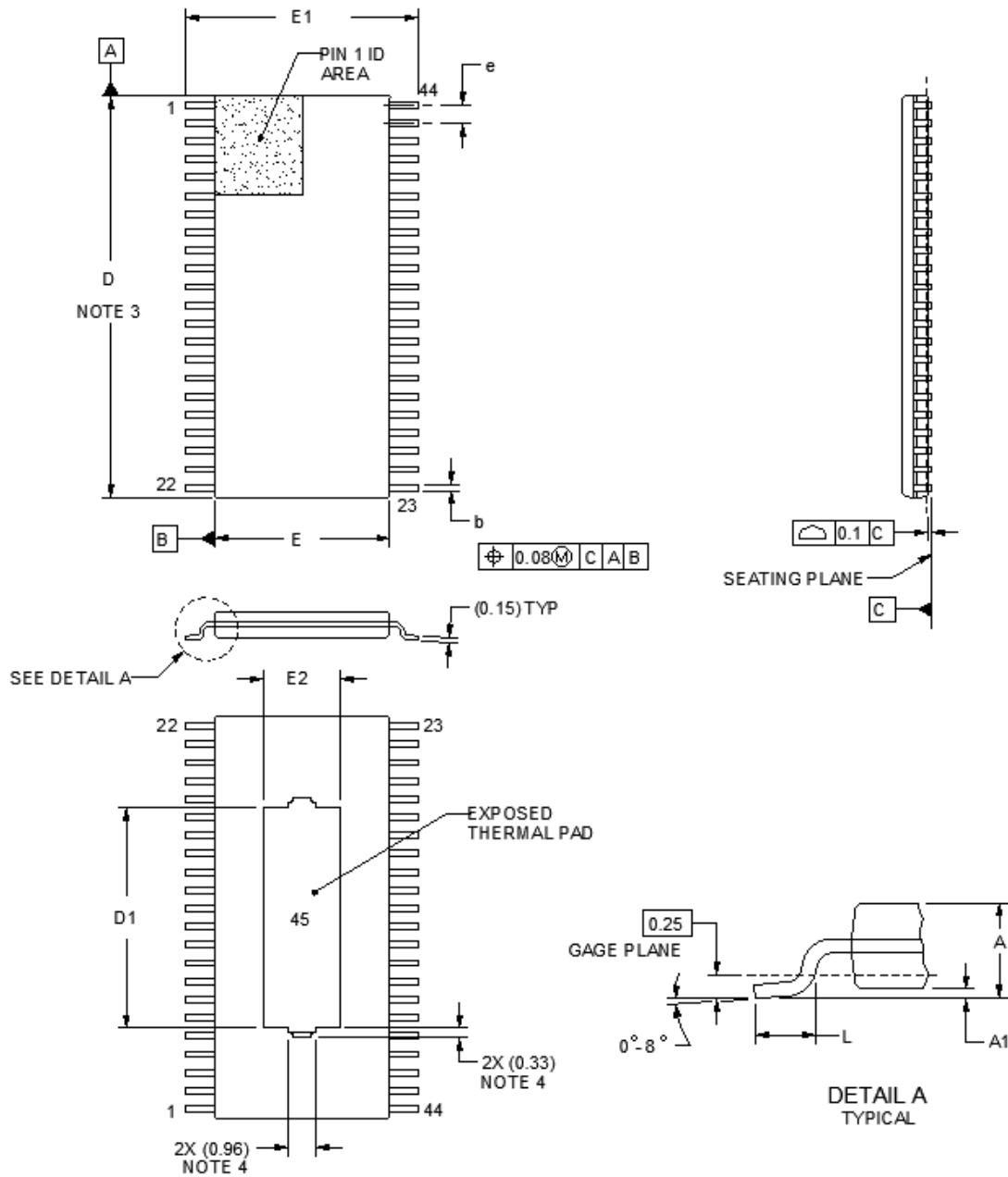
Table IB. SEP test limit. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_c)	V_{IN}	Results
01	SEL	$+125^{\circ}\text{C}$	7 V	No single event latch-up (SEL) was observed up to effective linear energy transfer (LET) of 43 MeV/(mg/cm ²)
	SEB/SEGR	$+25^{\circ}\text{C}$	7 V	No SEB/SEGR observed up to effective LET of 43 MeV/(mg/cm ²)
02	SEL	$+125^{\circ}\text{C}$	7 V	No single event latch-up (SEL) was observed up to effective linear energy transfer (LET) of 75 MeV/(mg/cm ²)
	SEB/SEGR	$+25^{\circ}\text{C}$	7 V	No SEB/SEGR observed up to effective LET of 75 MeV/(mg/cm ²)

- 1/ For single event phenomena (SEP) test conditions, see 4.3 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
- 3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. The Silver(Ag) ion beam was used at an angle of incidence of 0° at flux of 10^5 ions/cm²s, fluence level of 10^7 ions/cm². After the runs, no single event latch-up (SEL) or Single event Burnout (SEB) or Single event gate rupture (SEGR) were observed at an effective LET of 43 MeV/(mg/cm²) for device type 01 and 75 MeV/(mg/cm²) for device type 02 under certain test conditions. SEE test shall be perform in accordance with JESD57. For more information on SEE/SEP test please contact device manufacturer.

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Case outline X



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice. Features may differ or may not be present.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.

FIGURE 1. Case outline X (DIP Package).

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Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	-	1.2	e	0.635 BSC	
A1	0.05	0.15	E	6.0	6.2
b	0.17	0.27	E1	7.9 TYP	8.3 TYP
D	13.9	14.1	E2	2.42	2.94
D1	7.44	7.96	L	0.50	0.75

FIGURE 1. Case outline X (DIP Package) – continued.

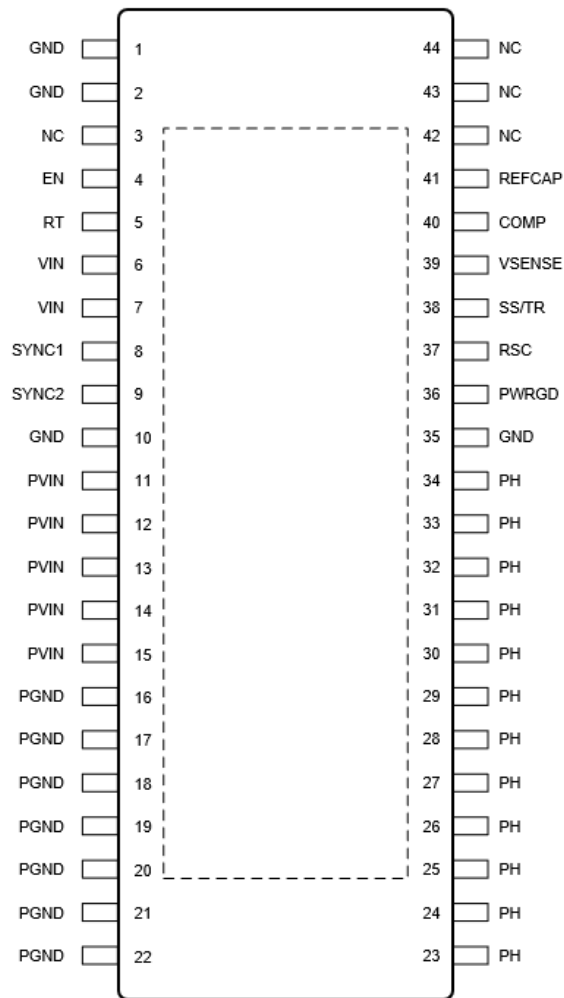


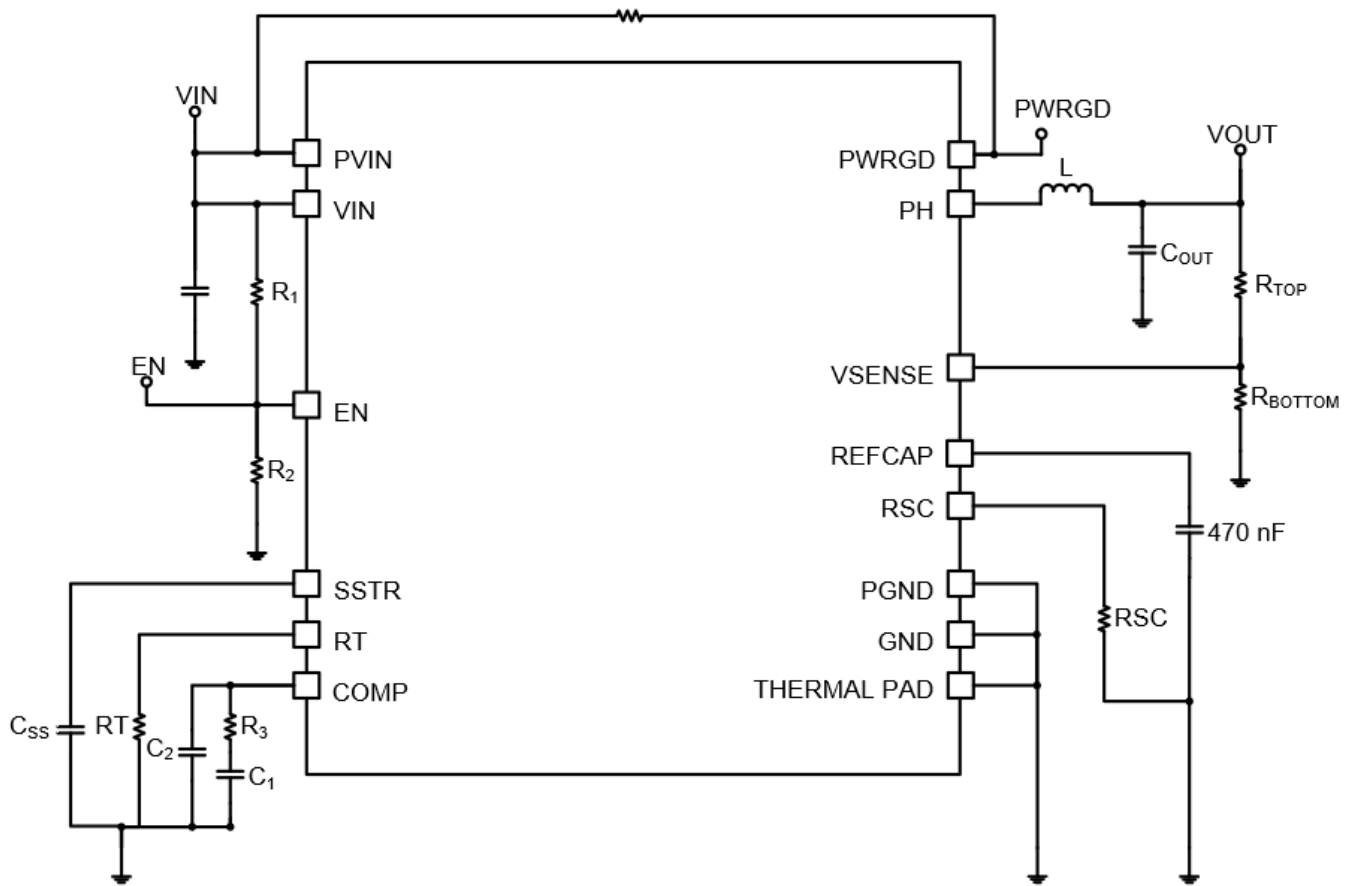
FIGURE 2. Terminal connections.

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PIN		I/O	Description
No.	Name		
1, 2, 10, 35	GND		Return for control circuitry.
3, 42-44	NC	I	No connect
4	EN	I	EN pin is internally pulled up allowing for the pin to be floated to enable the device.
5	RT	I/O	A resistor connected between RT and GND sets the switching frequency of the converter. The switching frequency range is 100 kHz to 1 MHz. When an external clock is used, RT must be selected such that the set switching frequency coincides with the frequency of the applied clock. Leaving this pin floating sets the internal switching frequency to 500 kHz and SYNC1 and SYNC2 become output clocks at 500 kHz, with SYNC1 aligned with the converter switching and SYNC2 90° out of phase.
6, 7	VIN	I	Input power for the control circuitry of the switching regulator.
8	SYNC1	I/O	SYNC1 is an input when an external clock is provided. The frequency of the external clock should match the switching frequency that is set by the resistor between RT and GND. With an external clock applied, the converter switching action is 180° out of phase with the external clock. When RT is floating, SYNC1 serves as an output of a 500-kHz clock signal that is in phase with the converter switching action. SYNC1 can be used in combination with SYNC2 in order to connect up to four devices in parallel.
9	SYNC2	I/O	SYNC2 is used for connecting multiple devices in parallel. For the primary device, with RT floating, SYNC2 outputs 500-kHz signal that is 90° out of phase with the SYNC1 output clock. For the secondary devices, in which RT is populated, SYNC2 is used to configure the phase of the input clock signal on SYNC1. When SYNC2 is connected to VIN, the internal clock of the secondary device is in phase with clock provided at SYNC1. When SYNC2 is connected to GND, the input clock signal at SYNC1 is internally inverted.
11-15	PVIN	I	Input power for the output stage of the switching regulator.
16-22	PGND		Return for low-side power MOSFET.
23-34	PH	O	Switch phase node.
36	PWRGD	O	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during soft-start.
37	RSC	I/O	A resistor to GND sets the desired slope compensation.
38	SS/TR	I/O	Soft-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
39	VSENSE	I	Inverting input of the gm error amplifier.
40	COMP	I/O	Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.
41	REFCAP	O	Required 470-nF external capacitor for internal reference.
	PowerPAD™		Used for heat sinking by soldering to GND copper on printed circuit board.

FIGURE 3. Terminal functions.

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NOTES:

1. The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. It is recommended to use a 1% tolerance or better and a 10 kΩ resistor for R_{TOP}. Calculate R_{BOTTOM} using equation: $R_{BOTTOM} = V_{REF} / (V_{OUT} - V_{REF}) \times R_{TOP}$, where V_{REF} = 0.605 V.

FIGURE 4. Simplified Schematic.

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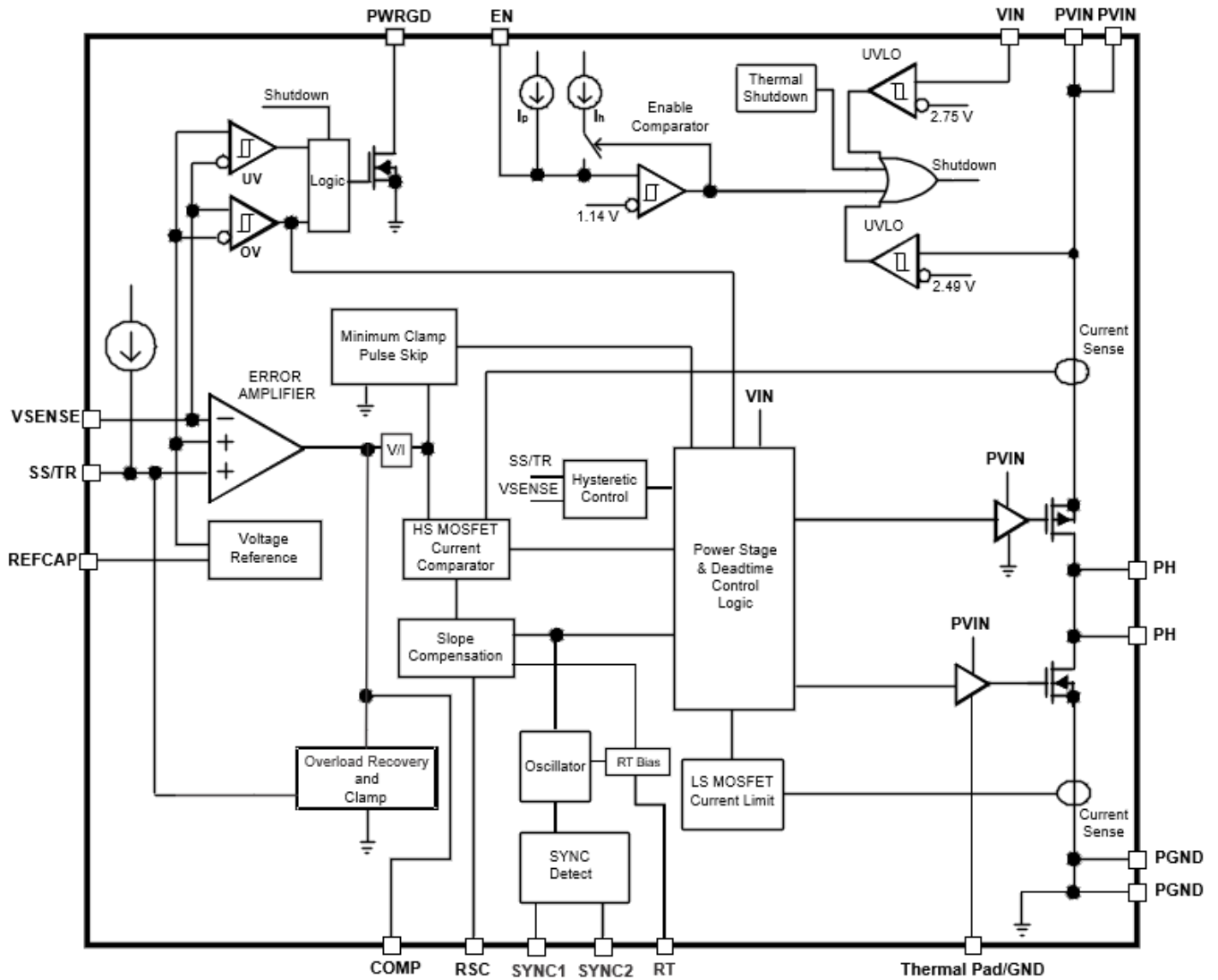
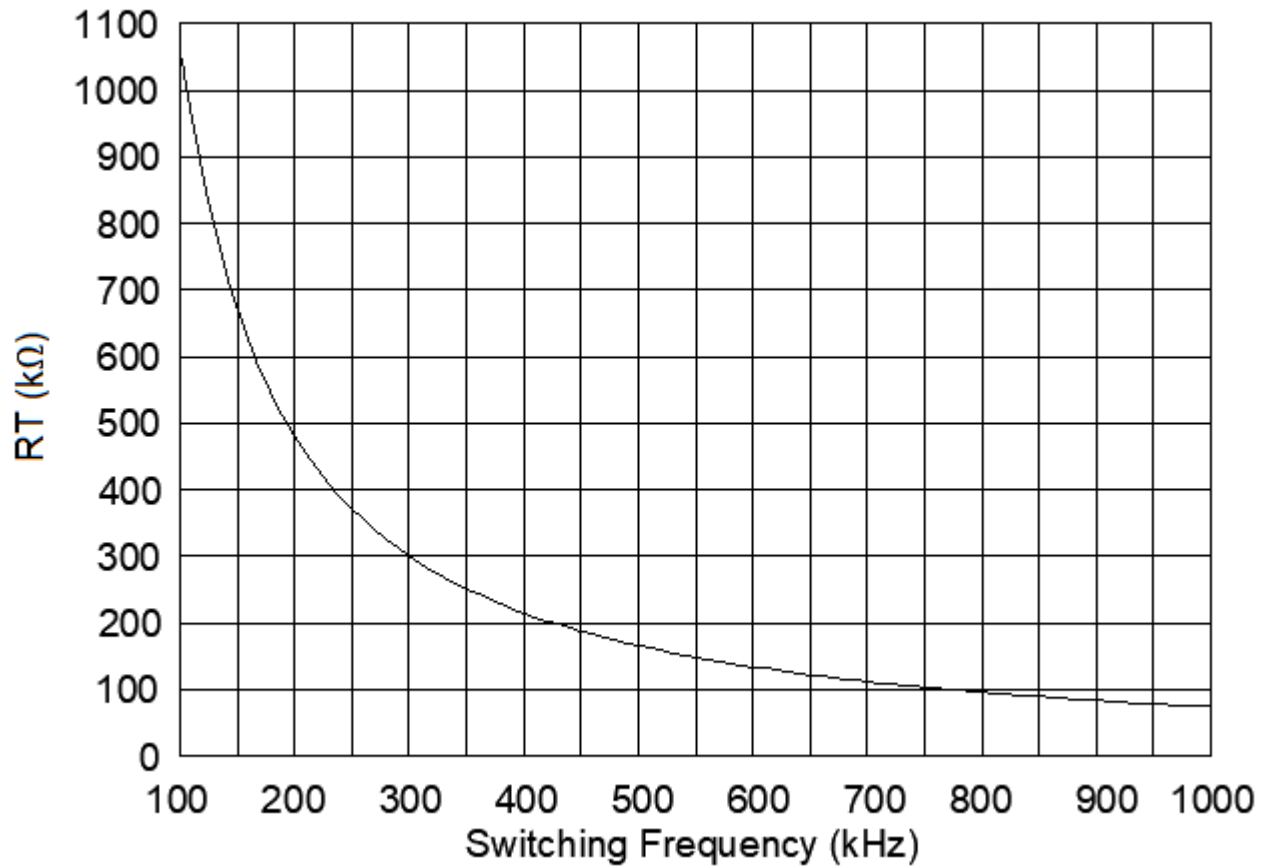


FIGURE 5. Functional Block Diagram.

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NOTES:

1. A resistor is connected between the RT pin and GND to configure the switching frequency, f_{sw} , of the device. The switching frequency is adjustable from 100 kHz to 1 MHz depending on the RT resistor value, which is calculated using the following equation: $RT = 223260 \times f_{sw}^{-1.159}$, where RT in kΩ and f_{sw} in kHz.

FIGURE 6. RT versus Frequency.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D for device type 01 and 02, and as specified in 1.5 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or ≥ 10⁷ ions/cm².
- c. The flux shall be between 10² and 10⁵ ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be +125°C ± 10% for SEL.
- f. For SEP test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS rating 2000V per Human body model (HDM) per ANSI/ESDA/JEDEC JS-0001 and Charge device model (CDM) to ESDS to 1000V (all pins) per ANSI/ESDA/JEDEC JS-002.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions of SEP.
- b. Number of single event latch-ups (SEL).
- c. Observance of SEB/SEGR.

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6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/21609-01XE	01295	TPS7H4003MDDWSEP
		TPS7H4003MDDWTSEP
V62/21609-02XE	01295	TPS7H4001MDDWTSHP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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