REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to the P_{DIS} and theta JC limits as specified under paragraph 1.3. Make change to the 6 GHz to 10 GHz frequency range section test limits as specified under Table I. Delete the COPLANARITY limits from A2 dimension limits as specified under Figure 1. Update Figure 3 graph. - ro	23-12-06	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing YY-MM-DD
19-08-07

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TITLE

MICROCIRCUIT, LINEAR, GaAs, pHEMT, MMIC, 0.01 GHz to 10 GHz LOW NOISE AMPLIFIER, MONOLITHIC GALLIUM ARSENIDE

SIZE	CAGE CODE	DWG NO.
A	16236	V62/19617
REV A		PAGE 1 OF 14

AMSC N/A

5962-V018-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 0.01 GHz to 10 GHz, low noise amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	HMC8411TCPZ-EP	GaAs, pHEMT, MMIC, 0.01 GHz to 10 GHz, low noise amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	See figure 1	Lead frame chip scale package(LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Drain bias voltage (V_{DD}) ..... 7 V
Radio frequency input (RF_{IN}) power ..... 20 dBm
Channel temperature ..... 175°C/W
Continuous power dissipation (P_{DIS}) : 3/
T_C = +85°C ..... 0.78 W
T_C = +125°C ..... 0.43 W
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Peak reflow temperature moisture sensitivity level 1 (MSL1) ..... 260°C
Thermal resistance, junction to case (θ_{JC}) ..... 115.35°C/W
Electrostatic discharge (ESD) rating:
Human body model (HDM) ..... 500 V, Class 1B passed

1.4 Recommended operating conditions. 4/

Drain bias voltage (V_{DD}) ..... 5 V
Supply current (I_{DQ}) ..... 55 mA
Operating temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the pin configuration and function descriptions section.
3/ For maximum power dissipation versus case temperature, see figure 3.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Maximum power dissipation versus case temperature graph. The Maximum power dissipation versus case temperature graph shall be as shown in figure 3.

3.5.4 Interface schematics. The interface schematics shall be as shown in figures 4, 5, 6, and 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{DD} = 5 V, I_{DQ} = 55 mA, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
0.01 GHz to 1 GHz frequency range							
Frequency range	f_R		+25°C	01	0.01	1	GHz
Gain	G		+25°C	01	15.5 typical		dB
					12.5		
Gain variation over temperature	G_{temp}		-55°C to 125°C	01	0.005 typical		dB / °C
Noise figure	NF		+25°C	01	1.8 typical		dB
Return loss input	RLI		+25°C	01	22 typical		dB
Return loss output	RLO		+25°C	01	17 typical		dB
Output power for 1 dB compression	P1dB		+25°C	01	20 typical		dBm
					17		
Saturated output power	P_{SAT}		+25°C	01	20.5 typical		dBm
Output third order intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 6 dBm	+25°C	01	33.5 typical		dBm
Output second order intercept	OIP2	Measurement taken at P_{OUT} per tone = 6 dBm	+25°C	01	43 typical		dBm
Power added efficiency	PAE	Measured at P_{SAT}	+25°C	01	30 typical		%
Supply current	I_{DQ}		+25°C	01	55 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, I_{DQ} = 55 mA, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
1 GHz to 6 GHz frequency range							
Frequency range	f_R		+25°C	01	1	6	GHz
Gain	G		+25°C	01	15 typical		dB
					12		
Gain variation over temperature	G_{temp}		-55°C to 125°C	01	0.010 typical		dB / °C
Noise figure	NF		+25°C	01	1.7 typical		dB
Return loss input	RLI		+25°C	01	25 typical		dB
Return loss output	RLO		+25°C	01	18 typical		dB
Output power for 1 dB compression	P1dB		+25°C	01	20 typical		dBm
					17		
Saturated output power	P_{SAT}		+25°C	01	21 typical		dBm
Output third order intercept	OIP3	Measurement taken at P_{OUT} per tone = 6 dBm	+25°C	01	34 typical		dBm
Output second order intercept	OIP2	Measurement taken at P_{OUT} per tone = 6 dBm	+25°C	01	39 typical		dBm
Power added efficiency	PAE	Measured at P_{SAT}	+25°C	01	34 typical		%
Supply current	I_{DQ}		+25°C	01	55 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, I_{DQ} = 55 mA, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
6 GHz to 10 GHz frequency range							
Frequency range	f_R		+25°C	01	6	10	GHz
Gain	G		+25°C	01	14 typical		dB
					11		
Gain variation over temperature	G_{temp}		-55°C to 125°C	01	0.013 typical		dB / °C
Noise figure	NF		+25°C	01	2 typical		dB
Return loss input	RLI		+25°C	01	15 typical		dB
Return loss output	RLO		+25°C	01	17 typical		dB
Output power for 1 dB compression	P1dB		+25°C	01	16 typical		dBm
					13		
Saturated output power	p_{SAT}		+25°C	01	19.5 typical		dBm
Output third order intercept	OIP3	Measurement taken at P_{OUT} per tone = 6 dBm	+25°C	01	33 typical		dBm
Output second order intercept	OIP2	Measurement taken at P_{OUT} per tone = 6 dBm	+25°C	01	40 typical		dBm
Power added efficiency	PAE	Measured at P_{SAT}	+25°C	01	23 typical		%
Supply current	I_{DQ}		+25°C	01	55 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

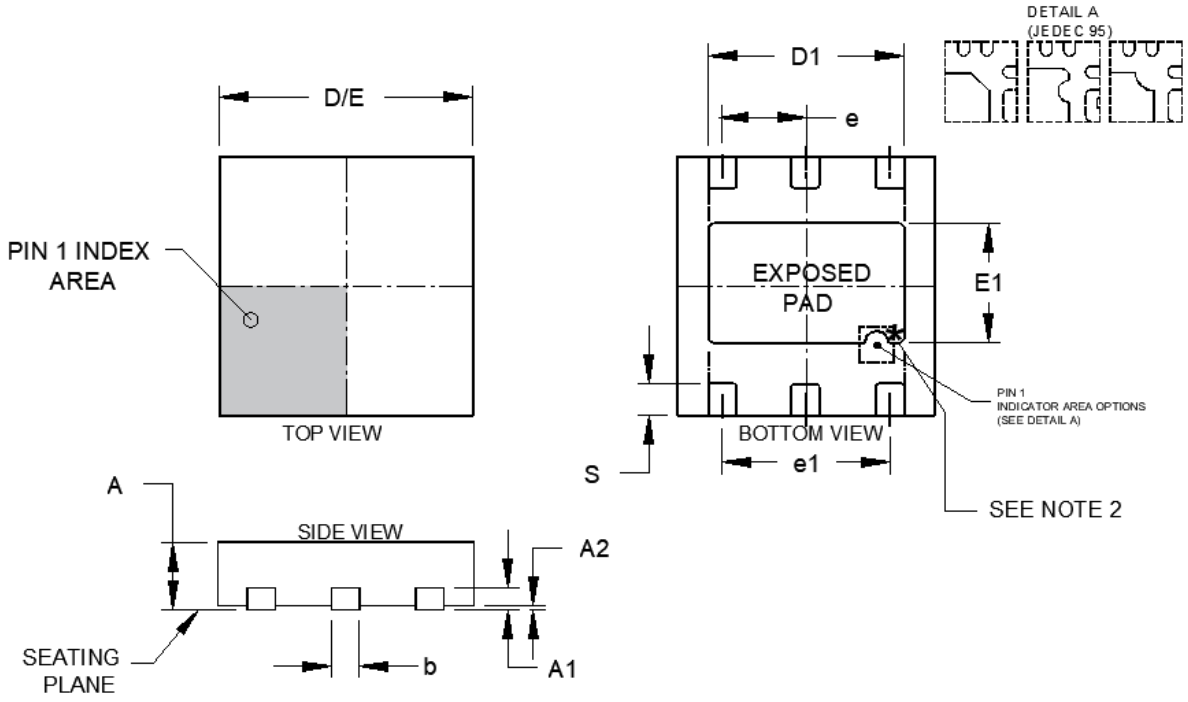

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/19617
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Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.031	.033	.035	0.80	0.85	0.90
A1	.008 REF			0.203 REF		
A2		.001	.002		0.02	0.05
b	.010	.012	.014	0.25	0.30	0.35
D/E	.077	.079	.081	1.95	2.00	2.05
D1	.059	.063	.067	1.50	1.60	1.70
E1	.035	.039	.043	0.90	1.00	1.10
e	.025 BSC			0.65 BSC		
e1	.051 REF			1.30 REF		
s	.008	.010	.012	0.20	0.25	0.30

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	R_{BIAS}	Current mirror bias resistor pin. Use this pin to set the current to the internal resistor by the external resistor. See figure 4 for the interface schematic.
2	RF_{IN}	RF input. This pin is ac-coupled and matched to 50 Ω. See figure 5 for the interface schematic.
3	NIC	Not internally connected. This pin is not connected internally. This pin must be connected to the RF and dc ground.
4	NIC	Not internally connected. This pin is not connected internally. This pin must be connected to the RF and dc ground.
5	RF_{OUT}/V_{DD}	Radio frequency output (RF_{OUT}). This pin is ac-coupled and matched to 50 Ω. See figure 6 for the interface schematic. Drain bias for the amplifier (V_{DD}). This pin is ac-coupled and matched to 50 Ω. See figure 6 for the interface schematic.
6	GND	Ground. This pin must be connected to the RF and dc ground. See figure 7 for the interface schematic.
	EPAD	Exposed pad. The exposed pad must be connected to RF and dc ground.

FIGURE 2. Terminal connections.

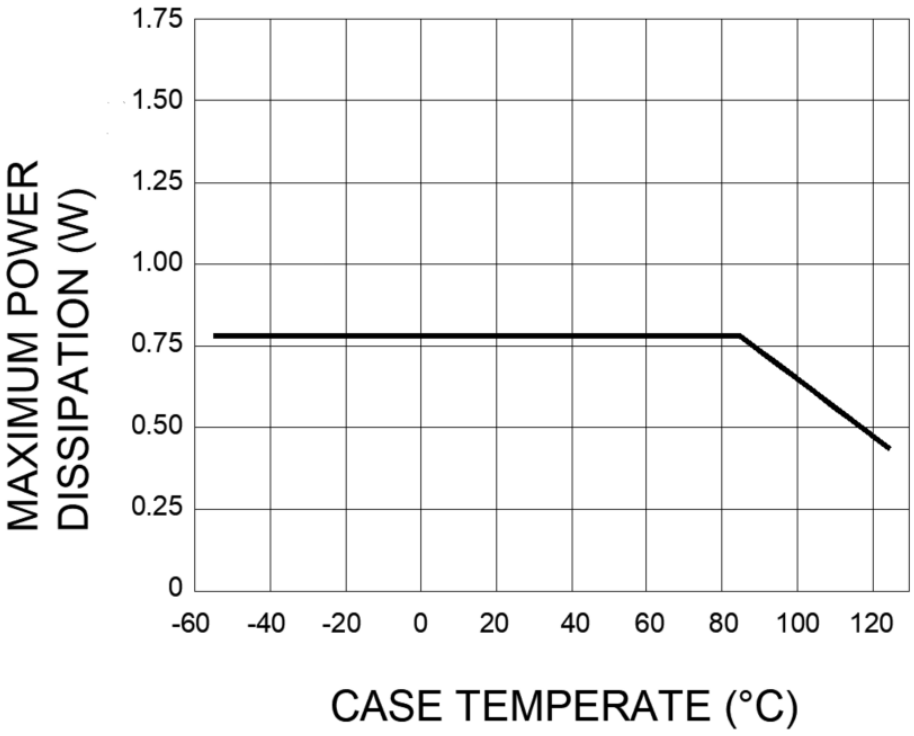

FIGURE 3. Maximum power dissipation versus case temperature.

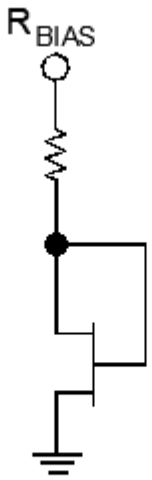

FIGURE 4. RBIAS interface schematic.

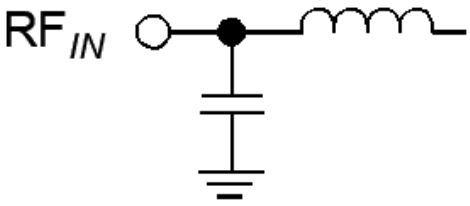

FIGURE 5. RFIN interface schematic.

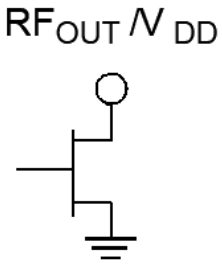

FIGURE 6. RFOUT/VDD interface schematic.

FIGURE 7. GND interface schematic.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/19617-01XE	24355	Cut tape (partial reel), 50 units	11T	HMC8411TCPZ-EP-PT
		Reel, 500 units	11T	HMC8411TCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123