REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add footnote 10/ to the Output propagation delay test as specified under Table I. Delete the A3 dimension and place the words 0.08 COPLANARITY on figure 1. Add L1 dimension to figure 1. Update document paragraphs to current requirements. - ro	24-10-17	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18				

PMIC N/A

Original date of drawing
YY-MM-DD
19-05-16

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TITLE

MICROCIRCUIT, DIGITAL-LINEAR, 10 BIT, 105 MSPS, 3 V DUAL ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/19610
REV A		PAGE 1 OF 18

AMSC N/A

5962-V083-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 10 bit, 105 million samples per second (MSPS) 3 V, dual analog to digital converter (ADC) microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	AD9218-EP	10 bit, 105 MSPS, 3 V, dual analog to digital converter

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026-BBC	Low profile quad flat package (LQFP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog supply voltage (V_D), Digital supply voltage (V_{DD})	4 V
Analog inputs	-0.5 V to V_D + 0.5 V
Digital inputs	-0.5 V to V_{DD} + 0.5 V
REF_{IN} inputs	-0.5 V to V_D + 0.5 V
Digital output current	20 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+150°C
Case temperature (T_C)	+150°C
Thermal resistance, junction to ambient (θ_{JC})	12°C/W 2/
Thermal resistance, junction to ambient (θ_{JA})	73°C/W 2/

1.4 Recommended operating conditions. 3/

Analog supply (V_D), Digital supply (V_{DD})	3 V
Operating temperature range (T_A)	-55°C to +105°C
Operating junction temperature (T_J)	+115°C
Operating case temperature (T_C)	+105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3, 4, and 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC SPECIFICATIONS.							
Resolution			+25°C	01	10 typical		Bits
Accuracy							
No missing codes 2/			-55°C to +105°C	01	Guaranteed, not tested		
Offset error 3/	OE		+25°C	01	+2 typical		LSB
					-18	+18	
Gain error 3/	GE		+25°C	01	+3.5 typical		%FS
					-2	+8	
Differential nonlinearity	DNL		+25°C	01	±0.8 typical		LSB
					-1	+1.7	
			-55°C to +105°C		±0.9 typical		
Integral nonlinearity	INL		+25°C	01	±2 typical		LSB
					-2.7	+2.7	
			-55°C to +105°C		±2.3 typical		
Temperature drift.							
Offset error			-55°C to +105°C	01	4 typical		ppm/°C
Gain error 3/			-55°C to +105°C	01	100 typical		ppm/°C
Reference			-55°C to +105°C	01	40 typical		ppm/°C
Reference.							
Internal reference voltage	REF_{OUT}		+25°C	01	1.24 typical		V
					1.18	1.28	
Input resistance	REF_{INA}, REF_{INB}		+25°C	01	11 typical		kΩ
					9	13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC SPECIFICATIONS – continued.							
Analog inputs.							
Differential input voltage range 4/	AINX, $\overline{AINX}$		-55°C to +105°C	01	1 typical		V
Common mode voltage 4/	V_{CM}		-55°C to +105°C	01	V_D/3 typical		V
Input resistance	R_{IN}		-55°C to +105°C	01	10 typical		kΩ
					7	16	
Input capacitance	C_{IN}		+25°C	01	3 typical		pF
Power supply.							
Analog supply voltage	V_D		-55°C to +105°C	01	3 typical		V
					2.7	3.6	
Digital supply voltage	V_{DD}		-55°C to +105°C	01	3 typical		V
					2.5	3.6	
Supply currents		I_{VD}(V_D = 3.0 V) 5/	-55°C to +105°C	01	183 typical		mA
						188	
		I_{VDD}(V_{DD} = 3.0 V) 5/	+25°C		17 typical		
Power dissipation dc 6/	P_D		-55°C to +105°C	01	550 typical		mW
						565	
Power down current 7/	I_{VD}		-55°C to +105°C	01	22 typical		mA
Power supply rejection ratio	PSRR		+25°C	01	±1 typical		mV/V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DIGITAL SPECIFICATIONS.							
Digital inputs.							
Encode input common mode			-55°C to +105°C	01	V_D/2 typical		V
Encode 1 voltage			-55°C to +105°C	01	2		V
Encode 0 voltage			-55°C to +105°C	01		0.8	V
Encode input resistance			-55°C to +105°C	01	2.0 typical		kΩ
					1.75	2.4	
Logic 1 voltage		S1, S2, DFS	-55°C to +105°C	01	2		V
Logic 0 voltage		S1, S2, DFS	-55°C to +105°C	01		0.8	V
Logic 1 current		S1	-55°C to +105°C	01	±0 typical		μA
					-50	50	
Logic 0 inputs		S1	-55°C to +105°C	01	-230 typical		μA
					-400	-50	
Logic 1 current		S2	-55°C to +105°C	01	230 typical		μA
					50	400	
Logic 0 inputs		S2	-55°C to +105°C	01	±0 typical		μA
					-50	50	
Logic 1 current		DFS	-55°C to +105°C	01	100 typical		μA
					30	200	
Logic 0 inputs		DFS	-55°C to +105°C	01	-230 typical		μA
					-400	-50	
Input capacitance	C_{IN}	S1, S2, Encode inputs	+25°C	01	2 typical		pF
		DFS			4.5 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DIGITAL SPECIFICATIONS – continued.							
Digital outputs.							
Logic 1 voltage			-55°C to +105°C	01	2.45		V
Logic 0 voltage			-55°C to +105°C	01		0.05	V
Output coding				01	Two's Complement or offset binary		
AC SPECIFICATIONS.							
Dynamic performance. 8/							
Signal to noise ratio (without harmonics)	SNR	f_{IN} = 10 MHz	+25°C	01	55 typical		dB
					53		
		f_{IN} = Nyquist 9/			54 typical		
					52		
Signal to noise and distortion (with harmonics)	SINAD	f_{IN} = 10 MHz	+25°C	01	53 typical		dB
					52		
		f_{IN} = Nyquist 9/			53 typical		
					51		
Effective number of bits	SNR	f_{IN} = 10 MHz	+25°C	01	8.6 typical		Bits
					8.4		
		f_{IN} = Nyquist 9/			8.6 typical		
					8.3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATIONS – continued.							
Dynamic performance – continued. 8/							
Second harmonic distortion	2HD	f_{IN} = 10 MHz	+25°C	01	-68 typical		dBc
					-60		
		f_{IN} = Nyquist 9/			-66 typical		
					-57		
Third harmonic distortion	3HD	f_{IN} = 10 MHz	+25°C	01	-63 typical		dBc
					-57		
		f_{IN} = Nyquist 9/			-69 typical		
					-57		
Spurious free dynamic range	SFDR	f_{IN} = 10 MHz	+25°C	01	-62 typical		dBc
					-57		
		f_{IN} = Nyquist 9/			-63 typical		
					-57		
Two tone intermodulation distortion	IMD	f_{IN1} = 30 MHz, f_{IN2} = 31 MHz at -7 dBFS	+25°C	01	-67 typical		dBc
Analog bandwidth, full power			+25°C	01	300 typical		MHz
Crosstalk			+25°C	01	-75 typical		dBc

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 3.0 V, V_D = 3.0 V, external reference unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SWITCHING SPECIFICATIONS. See figures 3, 4, and 5.							
Encode input parameters.							
Maximum encode rate			-55°C to +105°C	01	105		MSPS
Minimum encode rate			-55°C to +105°C	01		20	MSPS
Encode pulse width high	t_{EH}		-55°C to +105°C	01	3.8		ns
Encode pulse width low	t_{EL}		-55°C to +105°C	01	3.8		ns
Aperture delay	t_A		-55°C to +105°C	01	2 typical		ns
Aperture uncertainty	Jitter		-55°C to +105°C	01	3 typical		ps rms
Digital output parameters.							
Output valid time 10/	t_V		-55°C to +105°C	01	2.5		ns
Output propagation 10/ delay	t_{PD}		-55°C to +105°C	01	4.5 typical		ns
						6	
Output rise time	t_R		+25°C	01	1.0 typical		ns
Output fall time	t_F		+25°C	01	1.2 typical		ns
Out of range recovery time			+25°C	01	5 typical		ns
Transient response time			+25°C	01	5 typical		ns
Recovery time from power down			+25°C	01	10 typical		Cycles
Pipeline delay			-55°C to +105°C	01	5 typical		Cycles

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ No missing codes at room temperature guaranteed.

3/ Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.25 V external reference) in 1 V p-p range.

4/ ($A_{INx} - \overline{A_{INx}}$) = ±0.5 V in 1 V range (full-scale). The analog inputs self bias to $V_D/3$. This common-mode voltage can be overdriven externally by a low impedance source by ±300 mV (differential drive, gain = 1).

5/ AC power dissipation measured with rated encode and a 10 MHz analog input at 0.5 dBFS, C_{LOAD} = 5 pF.

6/ DC power dissipation measured with rated encode and a dc analog input (outputs static, IV_{DD} = 0).

7/ In power-down state, IV_{DD} = ±10 µA typical.

8/ AC specifications based on an analog input voltage of –0.5 dBFS at 10.0 MHz, unless otherwise noted. AC specifications are tested in 1 V p-p range and driven differentially.

9/ Tested close to Nyquist: 51 MHz.

10/ t_V and t_{PD} are measured from the 1.5 level of the ENC_X input to the 50% / 50% levels of the digital outputs swing. The digital output load during test must not exceed an ac load of 5 pF or a dc current of ±40 µA. Rise and fall times are measured from 10% to 90%.

Case X

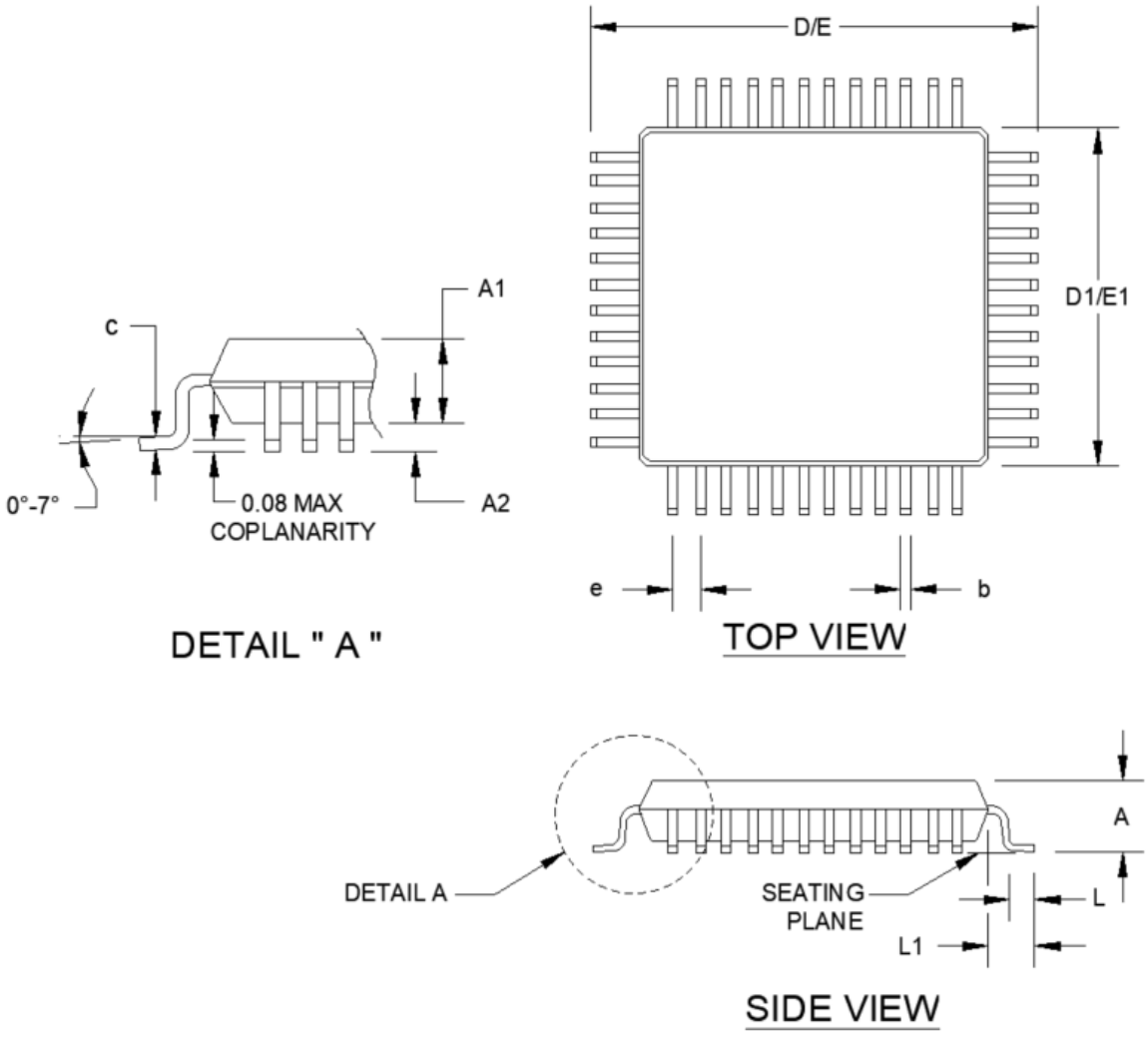

FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.0629	---	---	1.60
A1	.0531	.0551	.0570	1.35	1.40	1.45
A2	.0019	.0039	.0059	0.05	0.10	0.15
b	.0066	.0086	.0106	0.17	0.22	0.27
c	.0035	.0059	.0078	0.09	0.15	0.20
D/E	.3464	.35434	.3622	8.80	9.00	9.20
D1/E1	.2677	.2755	.2834	6.80	7.00	7.20
e	.019 BSC			0.50 BSC		
L	.0177	.0236	.0295	0.45	0.60	0.75
L1	.039 REF			1.00 REF		

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-026-BBC.

FIGURE 1. Case outline - Continued.

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	17	(MSB) $D9_B$	33	V_{DD}
2	AINA	18	$D8_B$	34	GND
3	$\overline{AINA}$	19	$D7_B$	35	$D0_A$
4	DFS/GAIN	20	$D6_B$	36	$D1_A$
5	$REF_{IN}A$	21	$D5_B$	37	$D2_A$
6	REF_{OUT}	22	$D4_B$	38	$D3_A$
7	$REF_{IN}B$	23	$D3_B$	39	$D4_A$
8	S1	24	$D2_B$	40	$D5_A$
9	S2	25	$D1_B$	41	$D6_A$
10	$\overline{AINB}$	26	$D0_B$	42	$D7_A$
11	AINB	27	GND	43	$D8_A$
12	GND	28	V_{DD}	44	$D9_A$ (MSB)
13	V_D	29	GND	45	GND
14	ENC_B	30	V_D	46	V_{DD}
15	V_{DD}	31	V_D	47	ENCA
16	GND	32	GND	48	V_D

FIGURE 2. Terminal connections.

Terminal numbers	Terminal symbol	Description
1, 12, 16, 27, 29, 32, 34, 45	GND	Ground.
2	AINA	Analog input for channel A.
3	$\overline{\text{AINA}}$	Analog input for channel A (complementary).
4	DFS/GAIN	Data format select and analog input gain mode. Low = offset binary output available, 1 V p-p supported; High = twos complement output available, 1 V p-p supported.
5	REF_{INA}	Reference voltage input for channel A.
6	REF_{OUT}	Internal reference voltage.
7	REF_{INB}	Reference voltage input for channel B.
8	S1	User select 1.
9	S2	User select 2.
10	$\overline{\text{AINB}}$	Analog input for channel B (complementary).
11	AIN_{B}	Analog input for channel B.
13, 30, 31, 48	V_D	Analog supply.
14	ENC_{B}	Encode B. Clock input for channel B.
15, 28, 33, 46	V_{DD}	Digital supply.
17 to 26	D9_{B} to D0_{B}	Digital output for channel B (D9_{B} = MSB).
35 to 44	D0_{A} to D9_{A}	Digital output for channel A (D9_{A} = MSB).
47	ENC_{A}	Encode A. Clock input for channel A.

FIGURE 2. Terminal connections - continued.

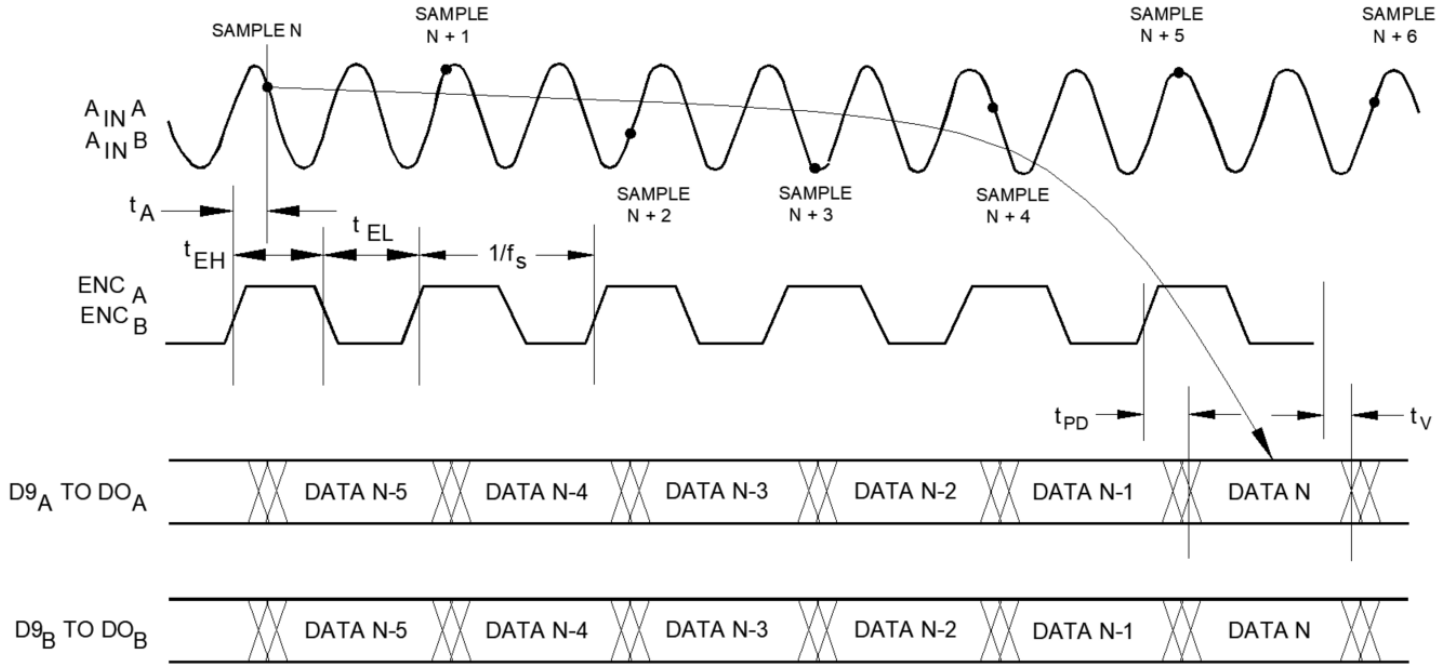

FIGURE 3. Normal operation, same clock (S1 = 1, S2 = 0) channel timing.

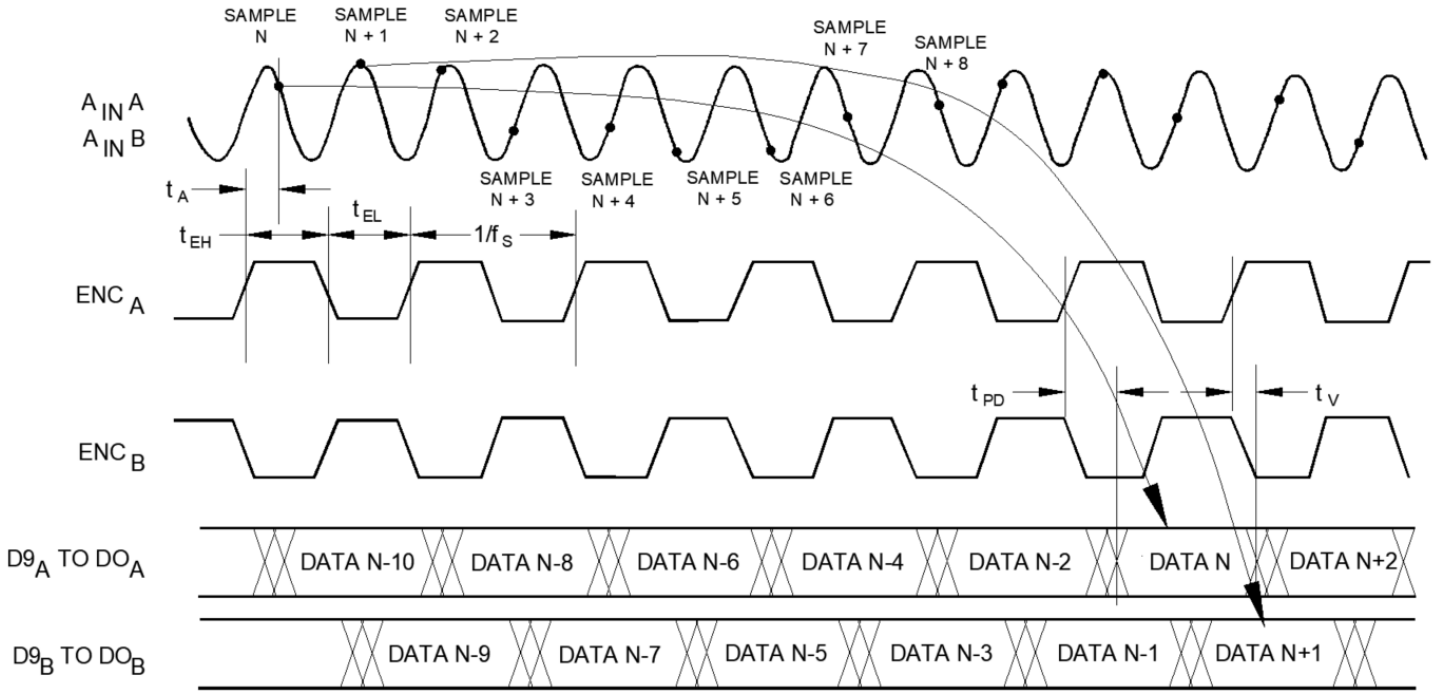

FIGURE 4. Normal operation with two clock sources (S1 = 1, S2 = 0) channel timing.

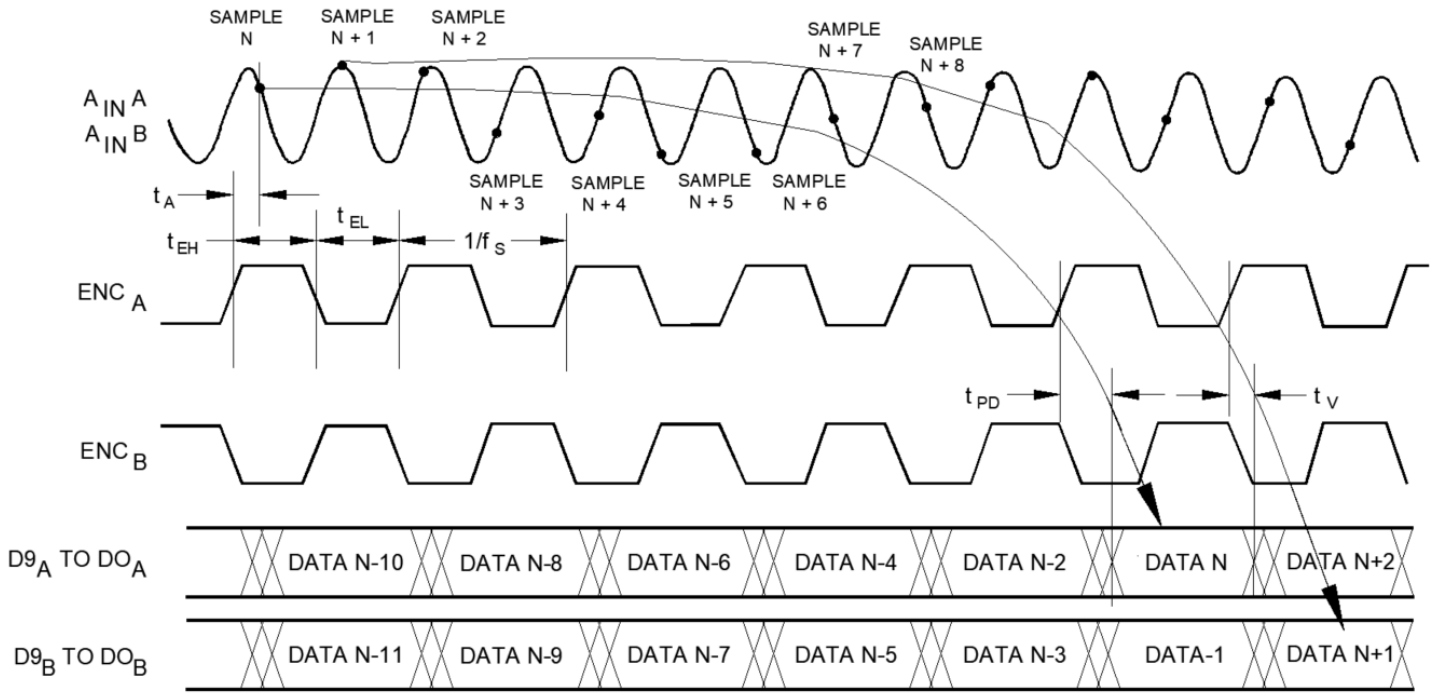

FIGURE 5. Data align with two clock sources (S1 = 1, S2 = 1) channel timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/19610-01XE	24355	Tray, 250 units	AD9218SSTZ-105-EP
		Reel, 2000 units	AD9218SSTZ-105EPRL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123