REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-09-17	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** JAMES R. ESCHMEYER	TITLE MICROCIRCUIT, LINEAR, DUAL DIFFERENTIAL DRIVERS AND RECEIVERS WITH ±12 kV ESD PROTECTION, MONOLITHIC SILICON
	SIZE A **CODE IDENT. NO.** 16236	**DWG NO.** V62/19606
	REV	**PAGE** 1 **OF** 20

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AMSC N/A

5962-V068-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual differential drivers and receives with ±12 kV electrostatic (ESD) protection microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19606	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65C1168E	Radiation hardened, dual differential and receivers with ±12 kV ESD protection

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7 V 2/
Input voltage:	
Driver, DE, RE	-0.5 V to +7 V
A or B, receiver	-14 V to +14 V
Differential input voltage (receiver)	-14 V to +14 V 3/
Output voltage (V_O):	
Driver	-0.5 V to +7 V
Receiver	-0.5 V to V_{CC} + 0.5 V
Input clamp current (I_{IK}) (driver, $V_I \leq 0$)	-20 mA
Output clamp current (I_{OK}):	
Driver $V_I \leq 0$	-20 mA
Receiver	±20 mA
Output current (I_O):	
Driver	±150 mA
Receiver	±25 mA
Supply current (I_{CC})	200 mA
Ground current	-200 mA
Junction temperature range (T_J)	150°C
Package thermal impedance	108°C/W 4/ 5/
Storage temperature range (T_{STG})	-65°C to +150°C
Operating free air temperature range (TA)	-55°C to +125°C
Electrostatic discharge (ESD) rating:	
Human body model (HDM) per JEDEC JS-001	±12,000 V 6/
Charge device model (CDM) per JEDEC JESD22-C1001	±1,000 V 7/
IEC 61000-4-2, air gap discharge	±8,000 V
IEC 61000-4-2,contact discharge	±8,000 V

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values except differential input voltage are with respect to the network GND.

3/ Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

4/ Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.

5/ The package thermal impedance is calculated in accordance with JESD 51-7.

6/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

7/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

1.4 Recommended operating conditions. 8/

Supply voltage range (V_{CC}) ..... 4.5 V to 5.5 V, 5 V nominal
Common mode input voltage (V_{IC}), receiver ..... ±7 V 9/
Differential input voltage (V_{ID}), receiver ..... ±7 V
Input voltage (V_I) except A, B ..... 0 V to 5.5 V
Output voltage (V_O) receiver ..... 0 V to V_{CC}
High level input voltage (V_{IH}) except A, B ..... 2 V minimum
Low level input voltage (V_{IL}) except A, B ..... 0.8 V maximum
High level output current (I_{OH}):
  Receiver ..... -6 mA maximum
  Driver ..... -20 mA maximum
Low level output current (I_{OL}):
  Receiver ..... 6 mA maximum
  Driver ..... 20 mA maximum
Operating free air temperature range (TA) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	102.5	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	32.3	°C/W
Thermal resistance, junction-to-board	θ_{JB}	48.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	1.8	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	48.2	°C/W

1.6 Radiation information.

Maximum total high dose rate available ..... 20 krads(Si) 10/
Single event phenomenon (SEP):
  No Single event latchup (SEL) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 11/

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
9/ Refer to TIA/EIA-422-B for exact conditions.
10/ Device type 01 supplied to this drawing has been characterized at 20 krad(Si) of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).
11/ See TABLE IB.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

International Electrotechnical Commission

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test

Copies of these documents are available online at https://www.iec.ch.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels
EIA-422 – Electrical Characteristics of Balanced Voltage Digital Interface Circuits.

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4 through 9.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section.							
Input clamp voltage	V_{IK}	I_I = -18 mA	-55°C to +125°C	01		-1.5	V
High level output voltage	V_{OH}	V_{IH} = 2 V, V_{IL} = 0.8 V,	+25°C	01	3.5 typical		V
		I_{OH} = -20 mA	-55°C to +125°C		2.4		
Low level output voltage	V_{OL}	V_{IH} = 2 V, V_{IL} = 0.8 V,	+25°C	01	0.2 typical		V
		I_{OL} = 20 mA	-55°C to +125°C			0.4	
Differential output voltage 1	$\|V_{OD1}\|$	I_O = 0 mA	-55°C to +125°C	01	2	6	V
Differential output voltage 2	$\|V_{OD2}\|$	R_L = 100 Ω, see figure 4 4/	+25°C	01	3.7 typical		V
			-55°C to +125°C		2		
Change in magnitude of differential output voltage	$\Delta\|V_{OD}\|$	R_L = 100 Ω, see figure 4 4/	-55°C to +125°C	01	-0.4	+0.4	V
Common mode output voltage	V_{OC}	R_L = 100 Ω, see figure 4 4/	-55°C to +125°C	01	-3	+3	V
Change in magnitude of common mode output voltage	$\Delta\|V_{OC}\|$	R_L = 100 Ω, see figure 4 4/	-55°C to +125°C	01	-0.4	+0.4	V
Output current with power off	$I_{O(OFF)}$	V_{CC} = 0 V, V_O = 6 V	-55°C to +125°C	01		100	µA
		V_{CC} = 0 V, V_O = -0.25 V				100	
	$I_{O(OFF)}$ 5/	V_{CC} = 0 V, V_O = 6 V	+25°C			3	mA
		V_{CC} = 0 V, V_O = -0.25 V				3	
High impedance state output current	I_{OZ}	V_O = 2.5 V	-55°C to +125°C	01		20	µA
		V_O = 5 V				-20	
	I_{OZ} 5/	V_O = 2.5 V	+25°C			2	mA
		V_O = 5 V				-2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section – continued.							
High level input current	I_{IH}	$V_I = V_{CC}$ or V_{IH}	-55°C to +125°C	01		1	µA
Low level input current	I_{IL}	V_I = GND or V_{IL}	-55°C to +125°C	01		-36	µA
Short circuit output current	I_{OS}	$V_O = V_{CC}$ or GND 6/	-55°C to +125°C	01	-30	-160	mA
Supply current (total package)	I_{CC}	$V_I = V_{CC}$ or GND, no load enabled	+25°C	01	4 typical		mA
			-55°C to +125°C			6	
		V_I = 2.4 V or 0.5 V, 7/ no load enabled	+25°C		5 typical		
			-55°C to +125°C			9	
	I_{CC} 5/	$V_I = V_{CC}$ or GND, no load enabled	+25°C			17	
		V_I = 2.4 V or 0.5 V, 7/ no load enabled				16	
Input capacitance	C_I		+25°C	01	6 typical		pF
Receiver section.							
Positive going input threshold voltage, differential input	V_{IT+}		-55°C to +125°C	01		0.2	V
Negative going input threshold voltage, differential input	V_{IT-}		-55°C to +125°C	01	-0.2 8/		V
Input hysteresis (V_{IT+} - V_{IT-})	V_{hys}		+25°C	01	60 typical		mV
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -6 mA	+25°C	01	4.2 typical		V
			-55°C to +125°C		3.8		
Low level output voltage	V_{OL}	V_{ID} = -200 mV, I_{OL} = 6 mA	+25°C	01	0.1 typical		V
			-55°C to +125°C			0.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver section - continued							
Line input current	I_I	V_I = 10 V, other input at 0 V	-55°C to +125°C	01		1.5	mA
		V_I = -10 V, other input at 0 V				-2.5	
Input resistance	r_I	VI_C = -7 V to 7 V, other input at 0 V	+25°C	01	17 typical		kΩ
			-55°C to +125°C		4		
Supply current (total package)	I_{CC}	V_I = V_{CC} or GND, no load enabled	+25°C	01	4 typical		mA
			-55°C to +125°C			6	
		V_{IH} = 2.4 or 0.5 V 4/ no load enabled	+25°C		5 typical		
			-55°C to +125°C			9	
	I_{CC} 5/	V_I = V_{CC} or GND, no load	+25°C			17	
		V_{IH} = 2.4 or 0.5 V, no load 7/				16	
Driver section switching characteristics.							
Propagation delay time, high to low level output	t_{PHL}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 5	+25°C	01	8 typical		ns
			-55°C to +125°C			16	
Propagation delay time, low to high level output	t_{PLH}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 5	+25°C	01	8 typical		ns
			-55°C to +125°C			16	
Pulse skew	$t_{sk(p)}$	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 5	+25°C	01	1.5 typical		ns
			-55°C to +125°C			4	
Rise time	t_r	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 6	+25°C	01	5 typical		ns
			-55°C to +125°C			8	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section switching characteristics - continued.							
Fall time	t_f	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 6	+25°C	01	5 typical		ns
			-55°C to +125°C			8	
Output enable time to high level	t_{PZH}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see figure 7	+25°C	01	10 typical		ns
			-55°C to +125°C			19	
Output enable time to low level	t_{PZL}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see figure 7	+25°C	01	10 typical		ns
			-55°C to +125°C			19	
Output disable time to high level	t_{PHZ}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see figure 7	+25°C	01	7 typical		ns
			-55°C to +125°C			16	
Output disable time to low level	t_{PLZ}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see figure 7	+25°C	01	7 typical		ns
			-55°C to +125°C			16	
Maximum switching frequency	f_{SW}	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see figure 6	-55°C to +125°C	01	20		MHz
Receiver section switching characteristics. 7/							
Propagation delay time, low to high level output	t_{PLH}	See figure 8	+25°C	01	15 typical		ns
			-55°C to +125°C		9	27	
Propagation delay time, high to low level output	t_{PHL}	See figure 8	+25°C	01	15 typical		ns
			-55°C to +125°C		9	27	
Transition time, low to high level output	t_{TLH}	V_{IC} = 0 V, see figure 8	+25°C	01	4 typical		ns
			-55°C to +125°C			9	
Transition time, high to low level output	t_{THL}	V_{IC} = 0 V, see figure 8	+25°C	01	4 typical		ns
			-55°C to +125°C			9	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical values are at V_{CC} = 5 V and T_A = +25°C.

3/ Device type 01 supplied to this drawing has been characterized at 20 krad(Si) of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

4/ Refer to TIA/EIA-422-B for exact conditions.

5/ Post radiation hardened limit.

6/ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7/ This parameter is measured per input, while the other inputs are at V_{CC} or GND.

8/ The algebraic convention, where the less positive (more negative) limit is designed as minimum, is used in manufacturer's datasheet for common mode input voltage and threshold voltage levels only.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP/SEE	Temperature (T_C)	Effective linear energy transfer (LET)
01	No SEL	+125°C	≤ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

Case X

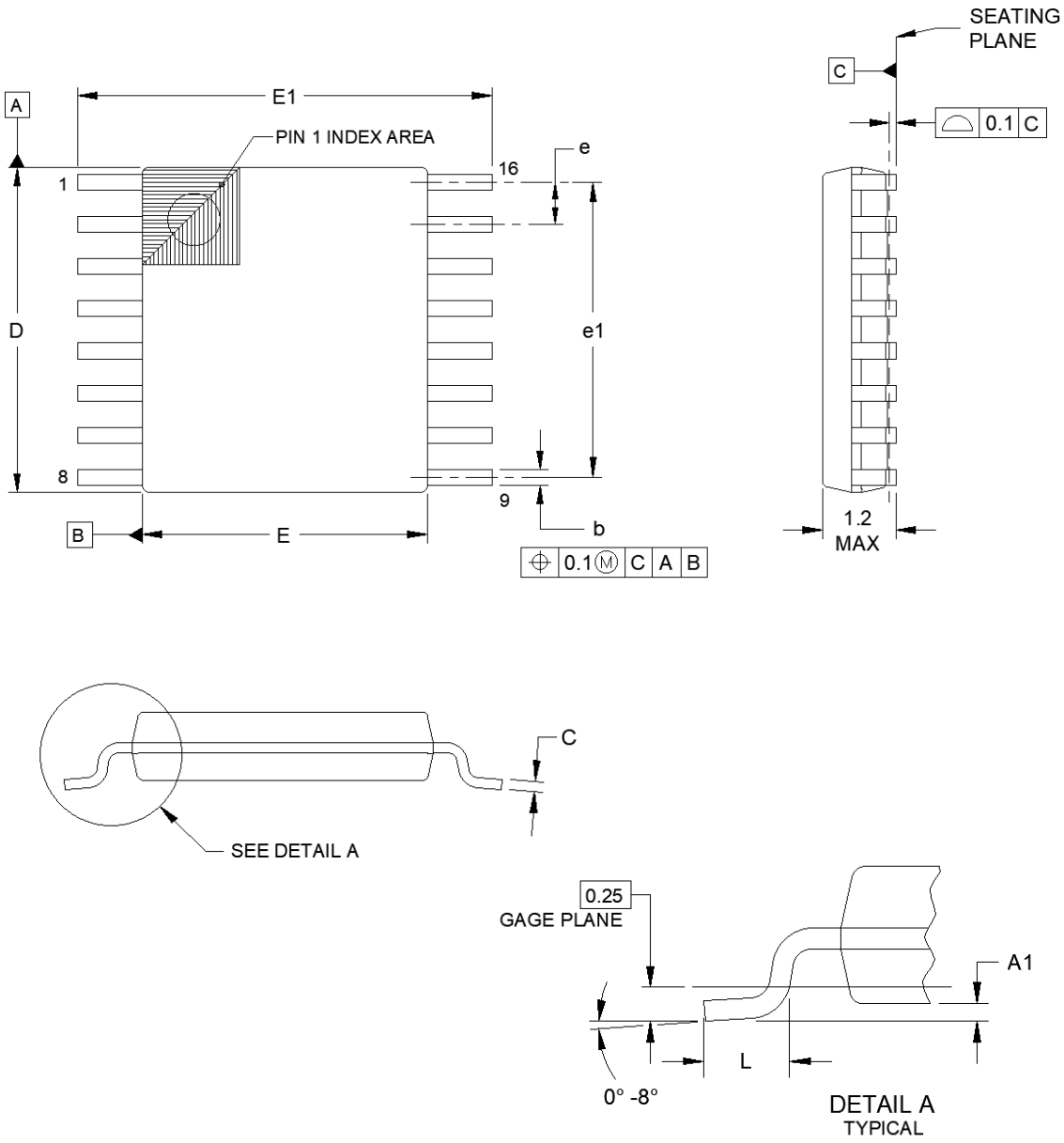

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/19606
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Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.2
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.005 TYP		0.15 TYP	
D	.192	.200	4.9	5.1
E	.169	.177	4.3	4.5
E1	.244	.259	6.2	6.6
e	.025 BSC		0.65 BSC	
e1	.179 BSC		4.55 BSC	
L	.019	.029	0.50	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.009 inch) per side.
4. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	1B	I	RS422 differential input (inverting) to receiver 1.
2	1A	I	RS422 differential input (noninverting) to receiver 1.
3	1R	O	Logic data output of RS422 receiver 1.
4	1DE	I	Driver 1 enable (active high).
5	2R	O	Logic data output of RS422 receiver 2.
6	2A	I	RS422 differential input (noninverting) to receiver 1.
7	2B	I	RS422 differential input (inverting) to receiver 2.
8	GND	---	Device ground.
9	2D	I	Logic data input to RS422 driver 2.
10	2Y	O	RS-422 differential (noninverting) driver output 2.
11	2Z	O	RS-422 differential (noninverting) driver output 2.
12	2DE	I	Driver 2 enable (active high).
13	1Z	O	RS-422 differential (noninverting) driver output 1.
14	1Y	O	RS-422 differential (noninverting) driver output 1.
15	ID	I	Logic data input to RS422 driver 1.
16	V_{CC}	---	Power supply.

FIGURE 2. Terminal connections.

Each driver

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

Each receiver

DIFFERENTIAL INPUTS A - B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leq -0.2$ V	L
Open	H

H = High voltage level
L = Low voltage level
? = Indeterminate

FIGURE 3. Truth table.

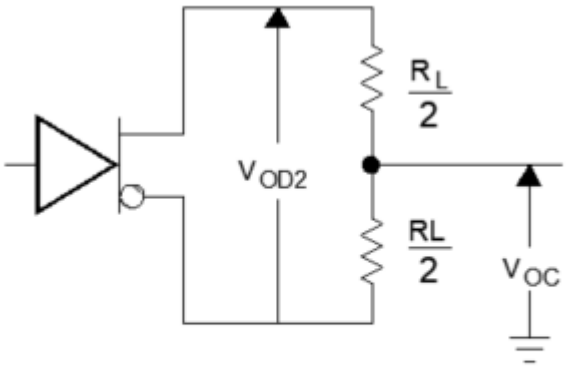
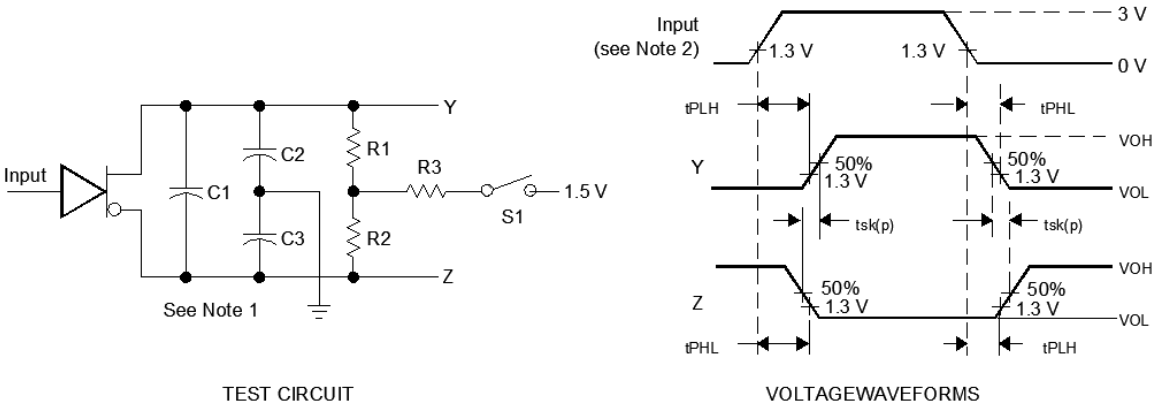
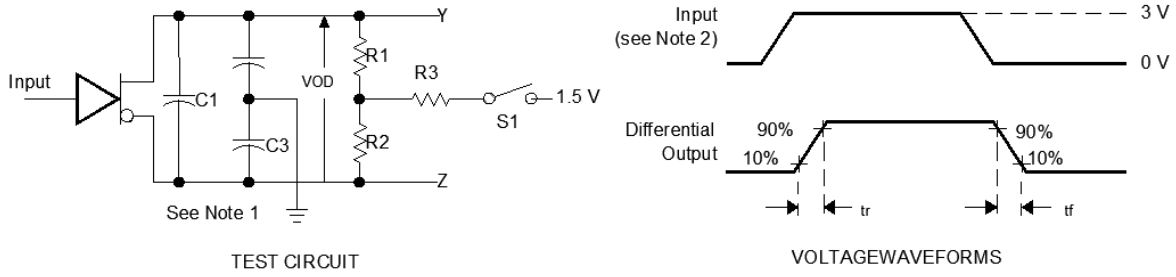


FIGURE 4. Driver test circuit, VOD and VOC.



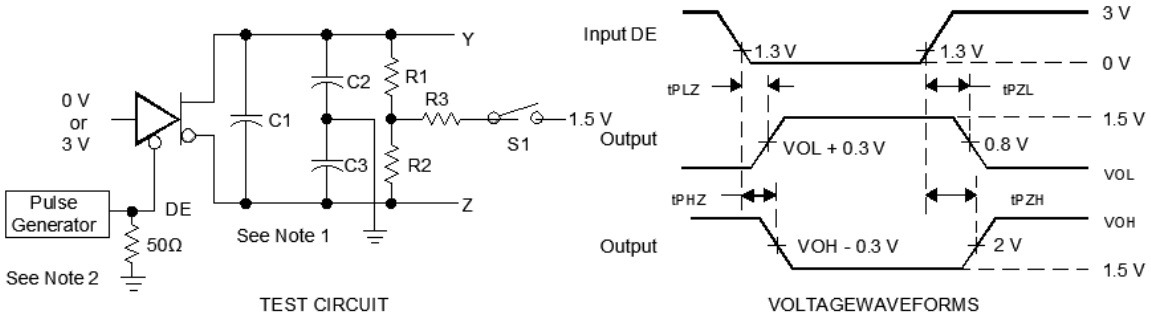
NOTES:
1. C1, C2, and C3 include probe and jig capacitance.
2. The input pulse is supplied be a generator having the following characteristics:
   PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

FIGURE 5. Driver test circuit and voltage waveforms.



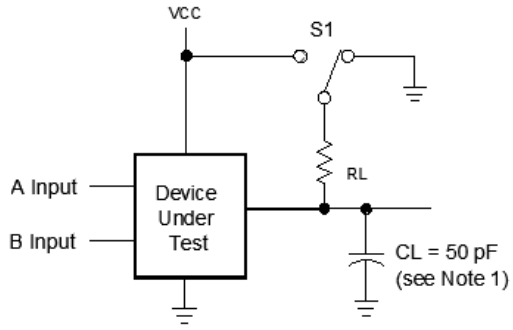
NOTES:
1. C1, C2, and C3 include probe and jig capacitance.
2. The input pulse is supplied be a generator having the following characteristics:
   PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

FIGURE 6. Driver test circuit and voltage waveforms.

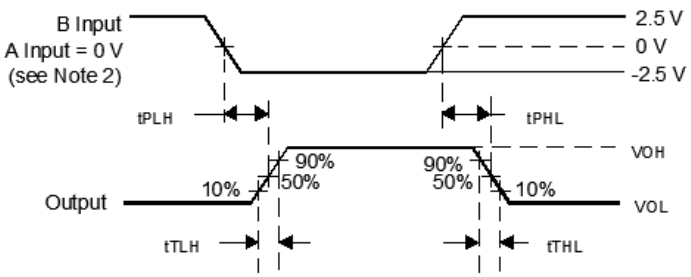


NOTES:
1. C1, C2, and C3 include probe and jig capacitance.
2. The input pulse is supplied be a generator having the following characteristics:
   PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

FIGURE 7. Driver test circuit and voltage waveforms.



TEST CIRCUIT



VOLTAGEWAVEFORMS

NOTES:
1. C1, C2, and C3 include probe and jig capacitance.
2. The input pulse is supplied be a generator having the following characteristics:
   PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

FIGURE 8. Receiver test circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified herein.

4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +125°C ±10%.

f. For SEL test limits, see table IB herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/19606-01XE	01295	Reel, 250 units	YMSG4	SN65C1168EMPWTSEP 2/
		Tube, 90 units	YMSG4	SN65C1168EMPWSEP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ This device has been characterized to 20 krads(Si), see paragraph 1.6 herein.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243