REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make change to SENSE input current and Timing capacitor charge current test limits as specified under Table I. - ro	21-07-27	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**			A	A	A	A	A	A	A	A	A	A									
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-04-10	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, SUPPLY VOLTAGE SUPERVISOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/19602**
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V082-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance supply voltage supervisor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TL7700-SEP	Supply voltage supervisor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-153-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... 41 V maximum 2/
Sense input voltage (V_S) ..... -0.3 V to 41 V
Output voltage (off state) (V_{OH}) ..... 41 V maximum
Output current (on state) (I_{OL}) ..... 5 mA
Operating virtual junction temperature range (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM) per JEDEC JS-001 ..... 500 V 3/
Charge device model (CDM) per JEDEC JESD22-C101 ..... 1000 V 4/

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 1.8 V to 40 V
Low level output current (I_{OL}) ..... 3 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	172.9	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	56.6	°C/W
Thermal resistance, junction-to-board	θ_{JB}	101.2	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	5.2	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	99.6	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to the network ground terminal.
3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Switching characteristics measurement circuit. The switching characteristics measurement circuit shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{CC} = 3 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical characteristics.							
SENSE input voltage	V_S		-55°C to +125°C	01	490	520	mV
SENSE input current	I_S	V_S = 0.4 V	25°C	01	2.5 typical		µA
			-55°C to +125°C		1	3.5	
Supply current	I_{CC}	V_{CC} = 40 V, V_S = 0.6 V, no load	25°C	01	0.6 typical		mA
						1	
Low level output voltage	V_{OL}	I_{OL} = 1.5 mA	25°C	01		0.4	V
		I_{OL} = 3 mA				0.8	
High level output current	I_{OH}	V_{OH} = 40 V, V_S = 0.6 V	-55°C to +125°C	01		1	µA
Timing capacitor charge current	I_{CT}	V_S = 0.6 V	25°C	01	15 typical		µA
					8	19	
Switching characteristics.		See figure 3					
SENSE pulse duration	t_{pl}	C_T = 0.01 µF	25°C	01	2		µs
Output pulse duration	t_{po}	C_T = 0.01 µF	25°C	01	1 typical		ms
					0.5	1.5	
Output rise time	t_r	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF	25°C	01		15	µs
Output fall time	t_f	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF	25°C	01		0.5	µs
Propagation delay time, SENSE to output	tpd	C_T = 0.01 µF	25°C	01		10	µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

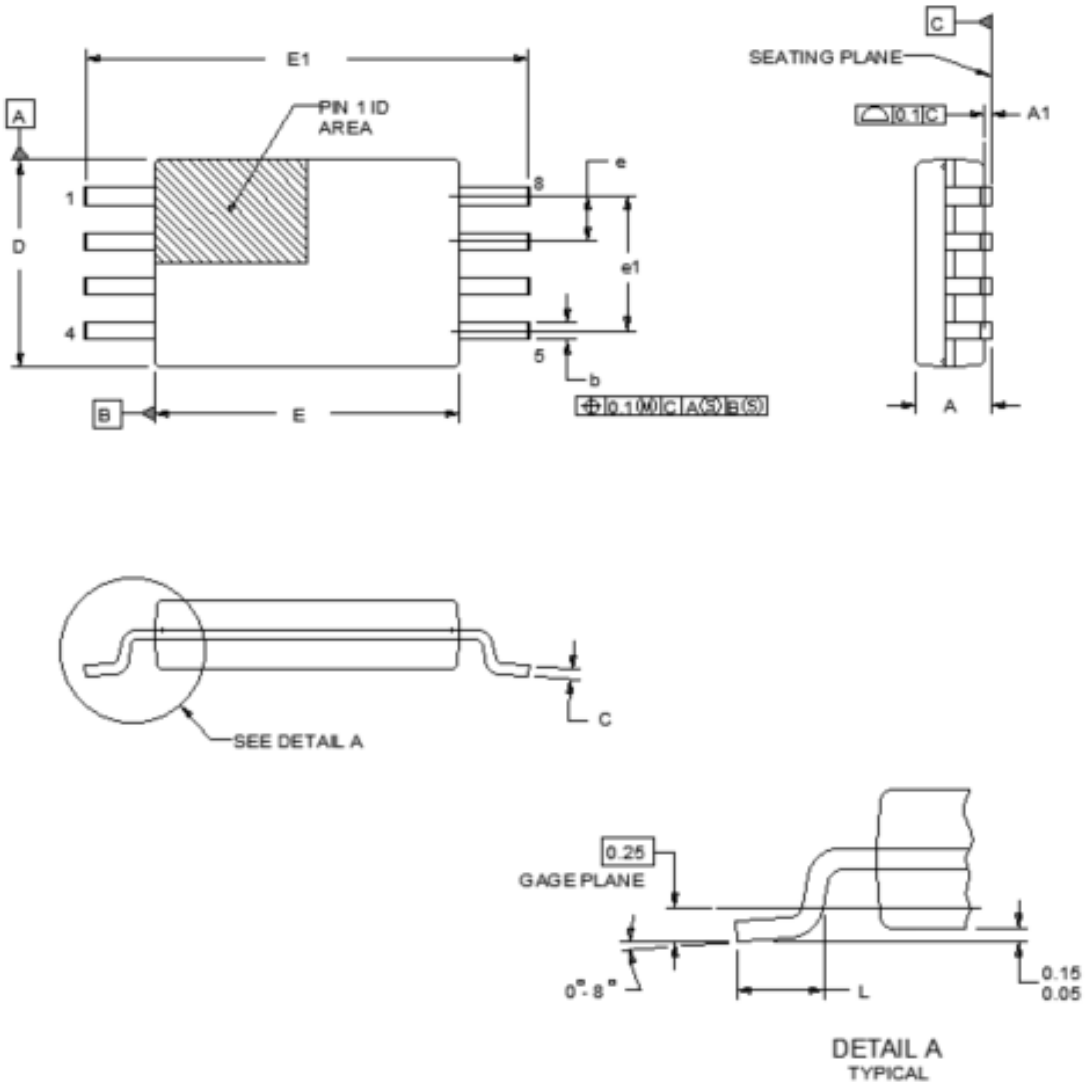

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/19602
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Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.2
A1	.004 BSC		0.1 BSC	
b	.007	.011	0.19	0.30
c	.005 TYP		0.15 TYP	
D	.114	.122	2.9	3.1
e	.025 BSC		0.65 BSC	
e1	.076 BSC		1.95 BSC	
E	.169	.177	4.3	4.5
E1	.244	.259	6.2	6.6
L	.019	.029	0.50	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The D dimension does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. The E dimension does not include interlead flash. Interlead flash shall not exceed 0.009 inch (0.25 mm) per side.
4. Falls within reference to JEDEC MO-153-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	CT	Timing capacitor connection. This terminal sets the RESET output pulse duration (t_{PO}). It is connected internally to a 15 μA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 μs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active, and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, field effect transistor (FET), or 3 state buffer (in the low level or high impedance state).
2	SENSE	Voltage sense. This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
3	NC	No internal connection.
4	GND	Ground. Keep this terminal as low impedance as possible to reduce circuit noise.
5	VCC	Power supply. This terminal is used in an operating-voltage range of 1.8 V to 40 V.
6	NC	No internal connection.
7	NC	No internal connection.
8	$\overline{\text{RESET}}$	Reset output. This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.

FIGURE 2. Terminal connections.

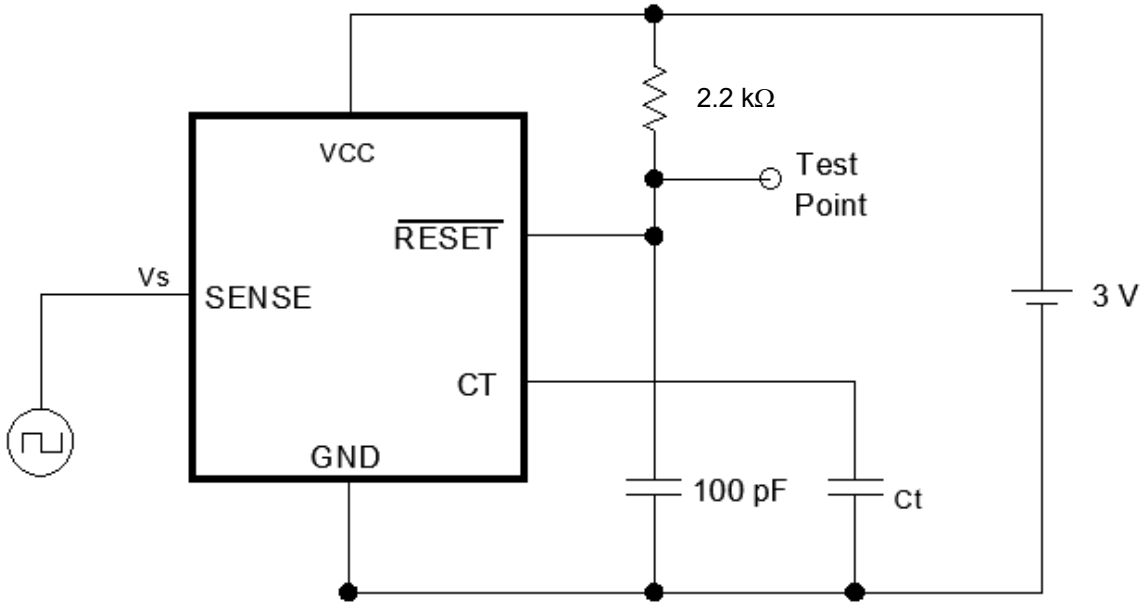

FIGURE 3. Switching characteristics measurement circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/19602-01XE	01295	150 units	7700SP	TL7700CMPWPSEP
		250 units	7700SP	TL7700CMPWTPSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243