REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	24-09-11	J. ESCHMEYER

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Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

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TITLE
MICROCIRCUIT, LINEAR, HIGH VOLTAGE ISOLATED GATE DRIVER WITH INTERNAL MILLER CLAMP, 2.3 AMP OUTPUT, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/19601
REV	A	PAGE 1 OF 14

AMSC N/A

5962-V080-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high voltage, isolated gate driver with internal Miller clamp 2.3 amp output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19601	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	ADuM4121-1-EP	Isolated gate driver with internal Miller clamp 2.3 amp output

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	See figure 1	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltages:
- V_{DD1} to GND_1 ..... -0.3 V to +7 V
- V_{DD2} to GND_2 ..... -0.3 V to +40 V

Input voltages:
- $+V_I$, $-V_I$ ..... -0.3 V to +7 V 2/
- V_{CLAMP} ..... -0.3 V to V_{DD2} + 0.3 V 3/

Output voltage:
- V_{OUT} ..... -0.3 V to V_{DD2} + 0.3 V 3/

Common mode transients |CM| ..... -200 kV/μs to +200 kV/μs 4/

Storage temperature range (T_{STG}) ..... -55°C to +150°C

Junction temperature range (T_J) ..... -55°C to +125°C

Thermal resistance, junction to ambient (θ_{JA}) ..... 104.2°C/W 5/

1.4 Recommended operating conditions. 6/

Supply voltages:
- V_{DD1} to GND_1 ..... 2.5 V to 6.5 V
- V_{DD2} to GND_2 ..... 7.5 V to 35 V

Junction temperature range (T_J) ..... -55°C to +125°C

1.5 Package characteristics.

Resistance (input side to high side output) (R_{IO}) ..... 10^{12} Ω typical 7/

Capacitance (input side to high side output) (C_{IO}) ..... 2.0 pF typical 7/

Input capacitance (C_I) ..... 4.0 pF typical

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Rating assumes V_{DD1} is above 2.5 V, $+V_I$ and $-V_I$ are rated up to 6.5 V when V_{DD1} is unpowered.

3/ Referenced to GND_2, maximum of 40 V.

4/ |CM| refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.

5/ Test condition 1: thermal impedance simulated values are based on a 4 layer printed circuit board (PCB).

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

7/ The device is considered a two-terminal device: pin 1 through pin 4 are shorted together, and pin 5 through pin 8 are shorted together.

1.6 Maximum continuous working voltage. 8/

Parameter	Rating	Unit	Constraint
AC voltage			
Bipolar waveform			
Basic insulation	849	V peak	50 year minimum insulation lifetime.
Reinforced insulation	789	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1.
Unipolar waveform			
Basic insulation	1698	V peak	50 year minimum insulation lifetime.
Reinforced insulation	849	V peak	50 year minimum insulation lifetime.
DC voltage			
Basic insulation	1118	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1.
Reinforced insulation	558	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1.

8/ Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier. See the manufacturer's data sheet for more details.

2. APPLICABLE DOCUMENTS

International Electrotechnical Commission

IEC 60950-1 – Information Technology Equipment - Safety

(Copies of these documents are available online at https://www.iec.ch.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
DC specifications							
High side power supply							
V_{DD2} Input voltage	V_{DD2}		-55°C to +125°C	01	7.5	35	V
V_{DD2} Quiescent input current	$I_{DD2(Q)}$		+25°C	01	2.3 typical		mA
			-55°C to +125°C			2.7	
V_{DD1} Input voltage	V_{DD1}		-55°C to +125°C	01	2.5	6.5	V
Input current	I_{DD1}	$+V_I$ = high, $-V_I$ = low	+25°C	01	3.6 typical		mA
			-55°C to +125°C			5	
Logic inputs ($+V_I$, $-V_I$)							
Input current	$+I_I$, $-I_I$		+25°C	01	0.01 typical		µA
			-55°C to +125°C		-1	+1	
Input voltage, logic high	V_{IH}	2.5 V ≤ V_{DD1} ≤ 5 V	-55°C to +125°C	01	0.7 x V_{DD1}		V
		V_{DD1} > 5 V			3.5		
Input voltage, logic low	V_{IL}	2.5 V ≤ V_{DD1} ≤ 5 V	-55°C to +125°C	01		0.3 x V_{DD1}	V
		V_{DD1} > 5 V				1.5	
Undervoltage lockout	(UVLO)						
V_{DD1}, Positive going threshold	$+V_{VDD1UV}$		+25°C	01	2.45 typical		V
			-55°C to +125°C			2.5	
V_{DD1}, Negative going threshold	$-V_{VDD1UV}$		+25°C	01	2.35 typical		V
			-55°C to +125°C		2.3		
V_{DD1}, Hysteresis	$V_{VDD1UVH}$		+25°C	01	0.1 typical		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Undervoltage lockout (UVLO) - continued.							
V_{DD2}, Positive going threshold	$+V_{VDD2UV}$		+25°C	01	7.3 typical		V
			-55°C to +125°C			7.5	
V_{DD2}, Negative going threshold	$-V_{VDD2UV}$		+25°C	01	7.1 typical		V
			-55°C to +125°C		6.9		
V_{DD2} Hysteresis	$V_{VDD2UVH}$		+25°C	01	0.2 typical		V
Internal NMOS gate resistance	R_{DSON_N}	Tested at 250 mA, V_{DD2} = 15 V	+25°C	01	0.6 typical		Ω
			-55°C to +125°C			1.6	
		Tested at 1 A, V_{DD2} = 15 V	+25°C		0.6 typical		
			-55°C to +125°C			1.6	
Internal PMOS gate resistance	R_{DSON_P}	Tested at 250 mA, V_{DD2} = 15 V	+25°C	01	0.8 typical		Ω
			-55°C to +125°C			1.8	
		Tested at 1 A, V_{DD2} = 15 V	+25°C		0.8 typical		
			-55°C to +125°C			1.8	
Internal Miller clamp resistance	R_{DSON_MILLER}	Tested at 200 mA, V_{DD2} = 15 V	+25°C	01	0.8 typical		Ω
			-55°C to +125°C			2	
Miller clamp voltage threshold	V_{CLP_TH}	Referenced to GND_2, V_{DD2} = 15 V	+25°C	01	2 typical		V
			-55°C to +125°C		1.75	2.25	
Peak current	I_{PK}	4 Ω gate resistance, V_{DD2} = 12 V	+25°C	01	2.3 typical		A

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Switching specifications							
Pulse width	PW	C_L = 2 nF, V_{DD2} = 15 V, 3/ R_{GON} = R_{GOFF} = 5 Ω	-55°C to +125°C	01	50		ns
Propagation delay, rising edge	t_{DLH}	C_L = 2 nF, V_{DD2} = 15 V, 4/ R_{GON} = R_{GOFF} = 5 Ω	+25°C	01	32 typical		ns
			-55°C to +125°C		22	42	
Propagation delay, falling edge	t_{DHL}	C_L = 2 nF, V_{DD2} = 15 V, 4/ R_{GON} = R_{GOFF} = 5 Ω	+25°C	01	38 typical		ns
			-55°C to +125°C		30	53	
Skew	t_{PSK}	C_L = 2 nF, V_{DD2} = 15 V, 5/ R_{GON} = R_{GOFF} = 5 Ω	-55°C to +125°C	01		22	ns
Skew, fall edge	t_{PSKHL}	C_L = 2 nF, V_{DD2} = 15 V, 5/ 6/ R_{GON} = R_{GOFF} = 5 Ω	-55°C to +125°C	01		12	ns
Skew, rising edge	t_{PSKLH}	C_L = 2 nF, V_{DD2} = 15 V, 5/ 7/ R_{GON} = R_{GOFF} = 5 Ω	-55°C to +125°C	01		15	ns
Pulse width distortion	t_{PWD}	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω	+25°C	01	7 typical		ns
			-55°C to +125°C			13	
Output rise/fall time (10% to 90%)	t_R / t_F	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω	+25°C	01	18 typical		ns
			-55°C to +125°C		11	26	
Common mode transient immunity (CMTI)							
Static CMTI 8/		V_{CM} = 1500 V	-55°C to +125°C	01	150		kV/μs
Dynamic CMTI 9/		V_{CM} = 1500 V	-55°C to +125°C	01	150		kV/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, low-side voltages referenced to GND_1. High side voltages referenced to GND_2; 2.5 V ≤ V_{DD1} ≤ 6.5 V; 7.5 V ≤ V_{DD2} ≤ 35 V, T_J = −55°C to +125°C. All minimum/maximum specifications apply over the entire recommended operating range. Unless otherwise specified, all typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 15 V.

3/ R_{GON} and R_{GOFF} are the external gate resistors in the text.

4/ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{OUT} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See the manufacturer's data sheet for waveforms of the propagation delay parameters.

5/ t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the manufacturer's data sheet for waveforms of the propagation delay parameters.

6/ t_{PSKHL} is the magnitude of the worst case difference in t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the manufacturer's data sheet for waveforms of the propagation delay parameters.

7/ t_{PSKLH} is the magnitude of the worst case difference in t_{DLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See the manufacturer's data sheet for waveforms of the propagation delay parameters.

8/ Static common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2, with inputs held either high or low, such that the output voltage remains either above 0.8 x V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.

9/ Dynamic common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2 with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

Case X

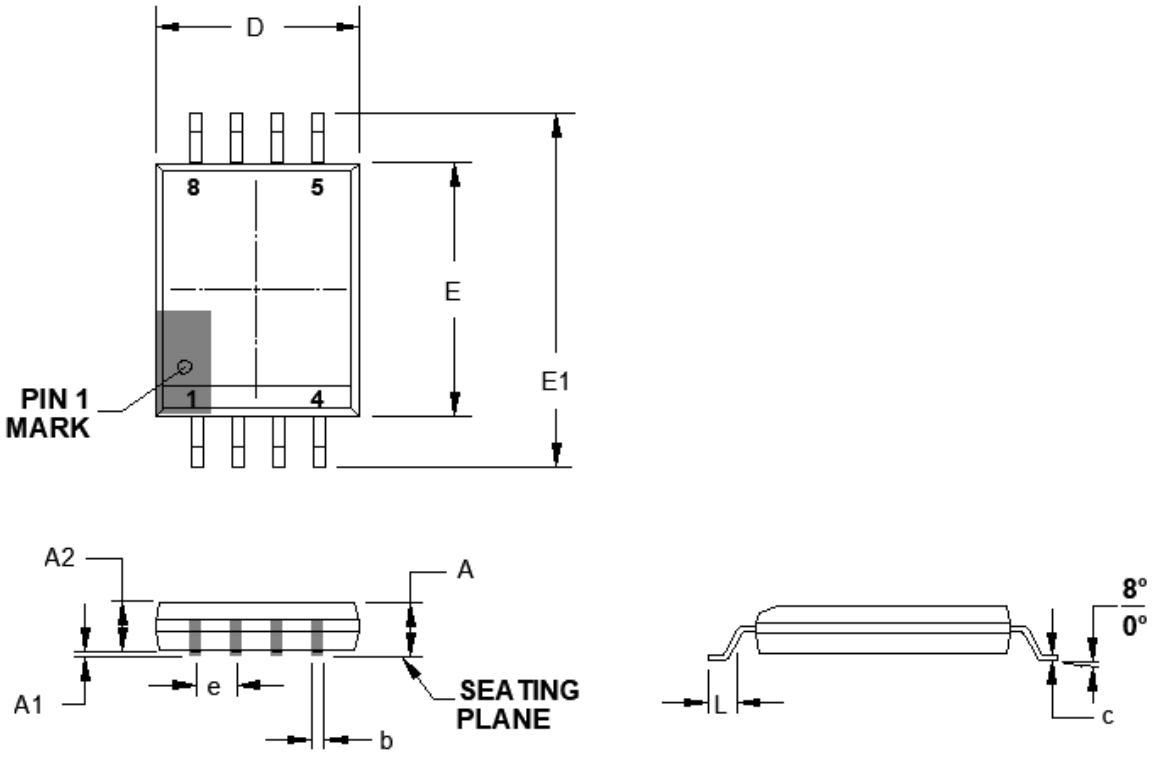

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/19601
		REV A	PAGE 10

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.0925	.0984	.1043	2.35	2.50	2.65
A1	.0039	.0078	.0118	0.10	0.20	0.30
A2	.0885	.0925	.0964	2.25	2.35	2.45
b	.0122	.0161	.0200	0.31	0.41	0.51
c	.0078	.0106	.0129	0.20	0.27	0.33
D	.2224	.2303	.2381	5.65	5.85	6.05
e	.0499 BSC			1.27 BSC		
E	.2913	.2952	.2992	7.40	7.50	7.60
E1	.3980	.4059	.4137	10.11	10.31	10.51
L	.0157	.0228	.0295	0.40	0.58	0.75

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Supply voltage for isolator side 1
2	$+V_I$	Noninverting gate drive logic input.
3	$-V_I$	Inverting gate drive logic input.
4	GND_1	Ground 1. This pin is the ground reference for isolator side 1.
5	GND_2	Ground 2. This pin is the ground reference for isolator side 2.
6	CLAMP	Miller clamp and gate voltage sense. Connect this pin directly to the gate being driven.
7	V_{OUT}	Gate drive output. Connect this pin to the gate being driven through an external series resistor.
8	V_{DD2}	Supply voltage for isolator side 2.

FIGURE 2. Terminal connections.

-VI	+VI	VDD1 state	VDD2 state	VOUT output
Don't care	Low	Powered	Powered	Low
Low	High	Powered	Powered	High
High	Don't care	Powered	Powered	Low
Don't care	Don't care	Unpowered	Powered	Low
Don't care	Don't care	Powered	Unpowered	Low SEE NOTE

NOTE: The output is low, but not actively driven because the device is not powered.

FIGURE 3. Truth table.

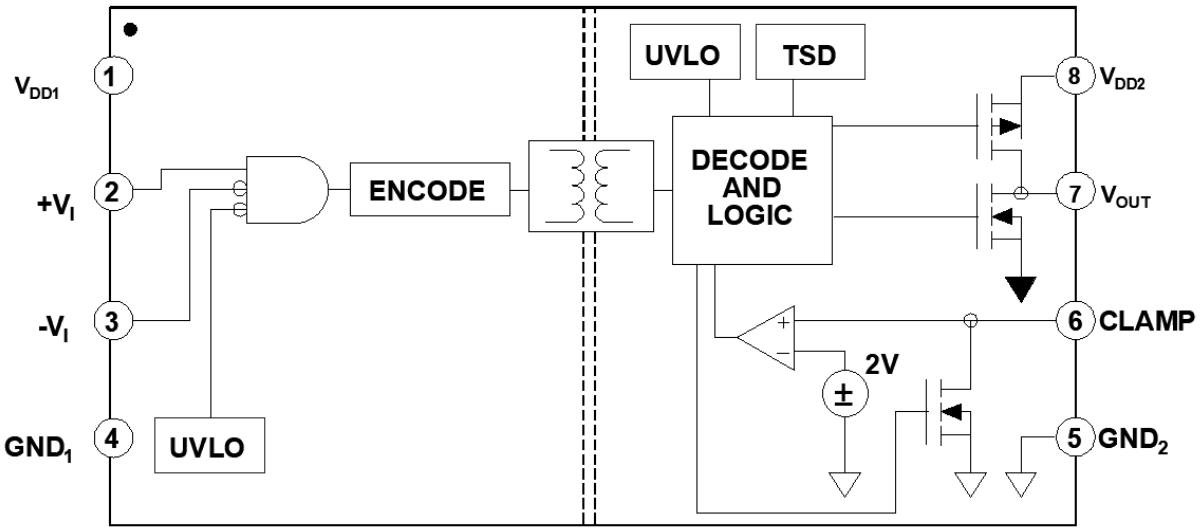

FIGURE 4. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/19601-01XE	24355	Tube, 80 units	4121	ADUM4121-1TRIZ-EP
		Reel, 1500 units	4121	ADUM4121-1TRIZ-EPR

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123