REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete paragraph 1.4 and add θ_{JA} limit to paragraph 1.3. Under Figure 1, delete numerical limits and replace with assigned letters and add dimensions table. Merge Figures 5, 6 and renumber figures. Update document paragraphs to current requirements. - ro	24-02-02	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing
YY-MM-DD
18-09-11

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, LINEAR-DIGITAL, 1.5 Ω ON RESISTANCE, ±15 V / 12 V / ± 5 V, CMOS, DUAL SPDT SWITCH, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. **V62/18618**

REV A

PAGE 1 OF 14

AMSC N/A

5962-V005-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1.5 Ω On resistance, ±15 V / 12 V / ±5 V, dual single pole, double throw (SPDT) switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/18618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG1436–EP	1.5 Ω On resistance, ±15 V/12 V/ ±5 V CMOS, dual SPDT switch

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	Thin shrink small outliner package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Positive power supply (V_{DD}) to Negative power supply (V_{SS})	35 V
V_{DD} to Gound (GND)	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog inputs 2/	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital inputs 2/	GND – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak current, Source (S) or Drain (D)	600 mA (pulsed at 1 ms, 10 % duty cycle maximum)
Continuous power dissipation 3/	See figure 5
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Reflow soldering peak temperature, lead (Pb) free	260(+0/-5)°C
Thermal resistance, junction to ambient (θ_{JA})	112°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Over voltages at Logic control input (IN), S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.

3/ Calculated based on 5 V dual supply model (see Table I).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.5 Truth table for switches. The truth table for switches shall be as shown in figure 4.

3.5.5 Maximum power dissipation versus ambient temperature graph. The maximum power dissipation versus ambient temperature graph shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 15 V dual supply 2/	Limits						Unit
			25°C			−55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						V_{DD} to V_{SS}			V
On Resistance	R_{ON}	V_S = ±10 V, I_S = −10 mA V_{DD} = +13.5 V, V_{SS} = −13.5 V		1.5	1.8			2.6	Ω
On-Resistance match between channels	ΔR_{ON}	V_S = ±10 V, I_S = −10 mA		0.1	0.18			0.21	Ω
On-Resistance flatness	$R_{FLAT(ON)}$	V_S = ±10 V, I_S = −10 mA		0.28	0.36			0.45	Ω
Continuous current per 3/ channel		V_{DD} = +13.5 V, V_{SS} = −13.5 V			260			100	mA
Leakage currents		(V_{DD} = +16.5 V, V_{SS} = −16.5 V)							
Source off leakage	$I_{S\ (Off)}$	V_S = ±10 V		±0.04	±0.55		±12.5		nA
Drain off leakage	$I_{D\ (Off)}$	V_S = ±10 V		±0.04	±0.55		±12.5		nA
Channel on leakage	I_D, $I_{S\ (On)}$	V_S = V_D = ±10 V		±0.1	±2		±35		nA
Digital inputs									
Input high voltage	V_{INH}					2.0			V
Input low voltage	V_{INL}							0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.005				±0.1	µA
Digital input capacitance	C_{IN}			3.5					pF
Dynamic characteristics									
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V		125	170			245	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF V_{S1} = V_{S2} = +10 V		20		10			ns
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF		-20					pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
Channel-to-channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
Total harmonic distortion + noise		R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz		0.011					%
−3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF		110					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-0.18					dB
Source off capacitance	$C_{S\ (Off)}$	f = 1 MHz, V_S = 0 V		23					pF
Drain off capacitance	$C_{D\ (Off)}$	f = 1 MHz, V_S = 0 V		50					pF
Drain on and Source on capacitance	C_D, $C_{S\ (On)}$	f = 1 MHz, V_S = 0 V		120					pF
POWER REQUIREMENTS		(V_{DD} = +16.5 V, V_{SS} = −16.5 V)							
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}		0.001				1	µA
		Digital input = 5 V		170				285	
Negative supply current	I_{SS}	Digital inputs = 0 V, 5 V, or V_{DD}		0.001				1.0	µA
Positive / negative supply voltage	V_{DD}/V_{SS}	GND = 0 V				±4.5		±16.5	V

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continuous. 1/

Test	Symbol	Test conditions 12 V single supply 4/	Limits						Unit
			25°C			−55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range							0 to V_{DD}		V
On Resistance	R_{ON}	V_S = 0 V to 10 V, I_S = −10 mA V_{DD} = +10.8 V, V_{SS} = −0 V		2.8	3.5			4.8	Ω
On-Resistance match between channels	ΔR_{ON}	V_S = 0 V to 10 V, I_S = −10 mA		0.13	0.21			0.25	Ω
On-Resistance flatness	$R_{FLAT(ON)}$	V_S = 0 V to 10 V, I_S = −10 mA		0.6	1.1			1.3	Ω
Continuous current per channel 3/		V_{DD} = 10.8 V, V_{SS} = 0 V			240			100	mA
Leakage currents		(V_{DD} = 13.2 V, V_{SS} = 0 V)							
Source off leakage	$I_{S\ (Off)}$	V_S = 1 V/10 V, V_D = 10 V/1 V		±0.04	±0.55		±12.5		nA
Drain off leakage	$I_{D\ (Off)}$	V_S = 1 V/10 V, V_D = 10 V/1 V		±0.04	±0.55		±12.5		nA
Channel on leakage	I_D, $I_{S\ (On)}$	V_S = V_D = 1 V or 10 V		±0.1	±1		±35		nA
Digital inputs									
Input high voltage	V_{INH}					2.0			V
Input low voltage	V_{INL}							0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.001				±0.1	µA
Digital input capacitance	C_{IN}			3.5					pF
Dynamics characteristics									
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V		200	270			350	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 8 V		70		10			ns
Charge injection		V_S = 6 V, R_S = 0 Ω, C_L = 1 nF		30					pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
Channel-to-channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
−3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF		78					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-0.3					dB
Source off capacitance	$C_{S\ (Off)}$	f = 1 MHz, V_S = 6 V		40					pF
Drain off capacitance	$C_{D\ (Off)}$	f = 1 MHz, V_S = 6 V		80					pF
Drain and Source on capacitance	C_D, $C_{S\ (On)}$	f = 1 MHz, V_S = 6 V		140					pF
Power requirements		(V_{DD} = 13.2 V)							
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}		0.001				1	µA
		Digital input = 5 V		170				285	
Negative supply current	I_{SS}	GND = 0 V, V_{SS} = 0 V				5		16.5	V

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continuous. 1/

Test	Symbol	Test conditions 5 V dual supply 5/	Limits						Unit
			25°C			−55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						0 to V_{DD}			V
On Resistance	R_{ON}	V_S = ±4.5 V, I_S = −10 mA V_{DD} = +4.5 V, V_{SS} = −4.5 V		3.3	4			5.4	Ω
On-Resistance match between channels	ΔR_{ON}	V_S = ±4.5 V, I_S = −10 mA		0.13	0.22			0.25	Ω
On-Resistance flatness	$R_{FLAT(ON)}$	V_S = ±4.5 V, I_S = −10 mA		0.9	1.1			1.31	Ω
Continuous current per channel 3/		V_{DD} = +4,5 V, V_{SS} = -4.5 V			240			100	mA
Leakage currents		(V_{DD} = +5.5 V, V_{SS} = -5.5 V)							
Source off leakage	$I_{S\ (Off)}$	V_S = ±4.5 V, V_D = ∓4.5 V		±0.03	±0.2		±12.5		nA
Drain off leakage	$I_{D\ (Off)}$	V_S = ±4.5 V, V_D = ∓4.5 V		±0.03	±0.2		±12.5		nA
Channel on leakage	$I_{D,\ IS\ (On)}$	V_S = V_D = ±4.5 V		±0.05	±0.25		±35		nA
Digital inputs									
Input high voltage	V_{INH}					2.0			V
Input low voltage	V_{INL}							0.8	V
Input current	I_{INL} or I_{INH}	V_{IN} = V_{GND} or V_{DD}		0.001				±0.1	µA
Digital input capacitance	C_{IN}			3.5					pF
Dynamic characteristics									
Transition time	$t_{TRANSITION}$	R_L = 300 Ω, C_L = 35 pF V_S = 3 V		310	445			565	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF V_{S1} = V_{S2} = 3 V		80		10			ns
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF		30					pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
Channel-to-channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-80					dB
Total harmonic distortion + noise		R_L = 110 Ω, 2.5 V p-p, f = 20 Hz to 20 kHz		0.03					%
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF		85					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-0.28					dB
Source off capacitance	$C_{S\ (Off)}$	V_S = 0 V, f = 1 MHz		33					pF
Drain off capacitance	$C_{D\ (Off)}$	V_S = 0 V, f = 1 MHz		65					pF
Drain and Source on capacitance	$C_{D,\ CS}$ (On)	V_S = 0 V, f = 1 MHz		145					pF
Power requirements		(V_{DD} = +5.5 V, V_{SS} = −5.5 V)							
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}		0.001				1	µA
		Digital inputs = 0 V or V_{DD}		0.001				1	
Negative supply current	I_{SS}	GND = 0 V				±4.5		±16.5	V

See footnote at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

3/ Guaranteed by design, not subject to production test.

4/ V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

5/ V_{DD} = 5 V ± 10%, V_{SS} = -5 V ± 10%, GND = 0 V, unless otherwise noted.

Case X

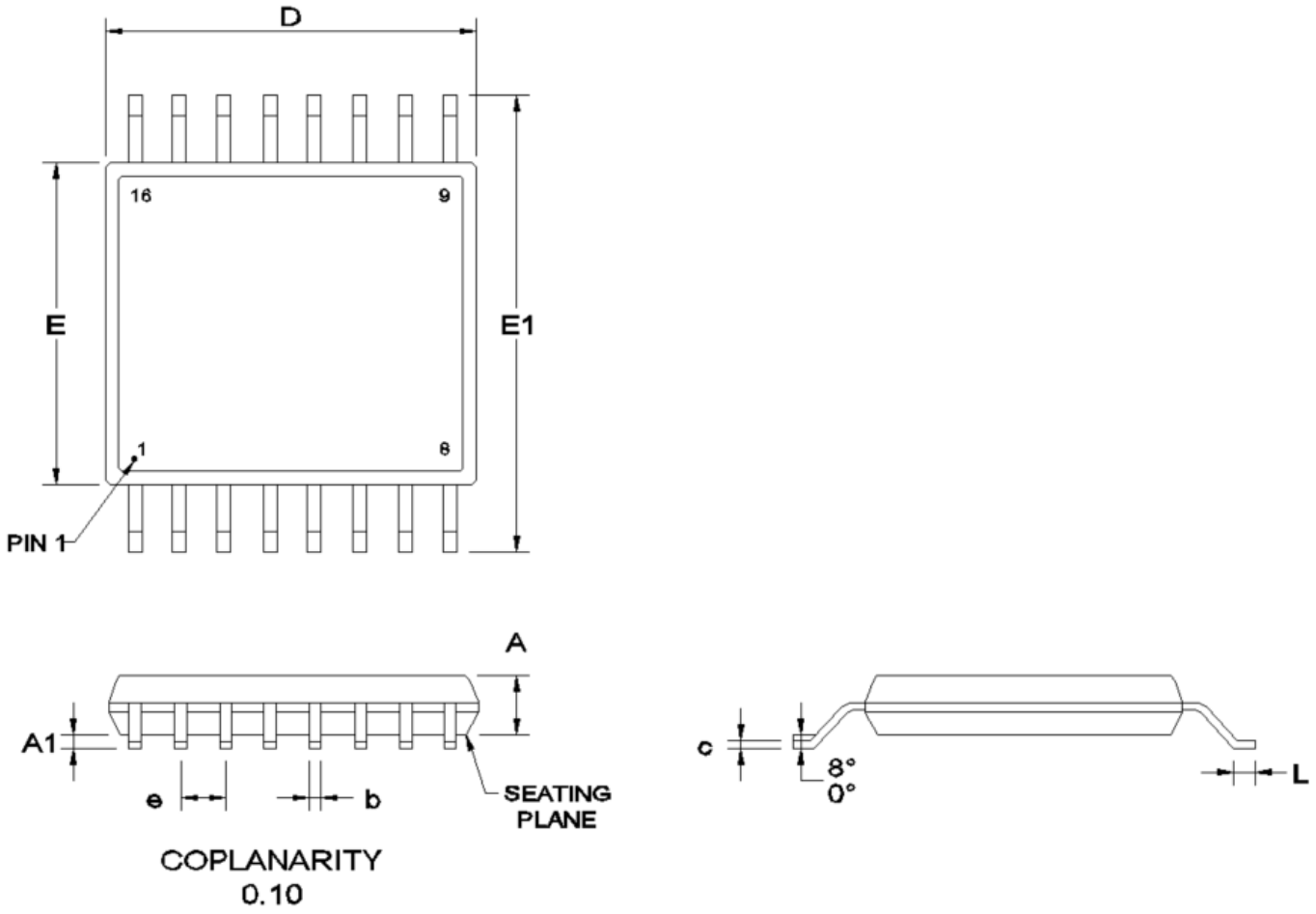
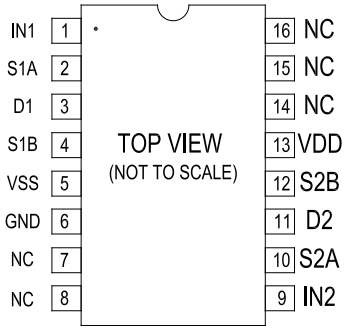


FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.047	---	---	1.20
A1	.002	---	.006	0.05	---	0.15
b	.007	---	.012	0.19	---	0.30
c	.003	---	.008	0.09	---	0.20
D	.193	.197	.201	4.90	5.00	5.10
E	.169	.173	.177	4.30	4.40	4.50
E1	.252 BSC			6.40 BSC		
e	.025 BSC			0.65 BSC		
L	.018	.024	.029	0.45	0.60	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AB.

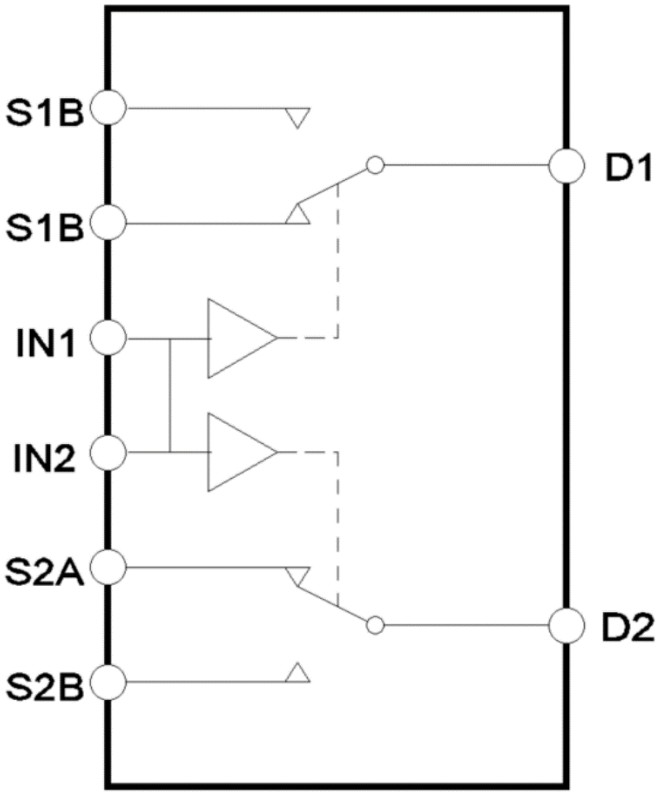
FIGURE 1. Case outline - Continued.



NC = NO CONNECT

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	IN1	Logic control input.
2	S1A	Source terminal. Can be an input or output.
3	D1	Drain terminal. Can be an input or output.
4	S1B	Source terminal. Can be an input or output.
5	V_{SS}	Most negative power supply potential.
6	GND	Ground (0 V) reference.
7	NC	No connection.
8	NC	No connection.
9	IN2	Logic control input.
10	S2A	Source terminal. Can be an input or output.
11	D2	Drain terminal. Can be an input or output.
12	S2B	Source terminal. Can be an input or output.
13	V_{DD}	Most positive power supply potential.
14	NC	No connection.
15	NC	No connection.
16	NC	No connection.

FIGURE 2. Terminal connections.



Switches shown for a one input logic.

FIGURE 3. Functional block diagram.

INx	SxA	SxB
0	Off	On
1	On	Off

FIGURE 4. Truth table for switches.

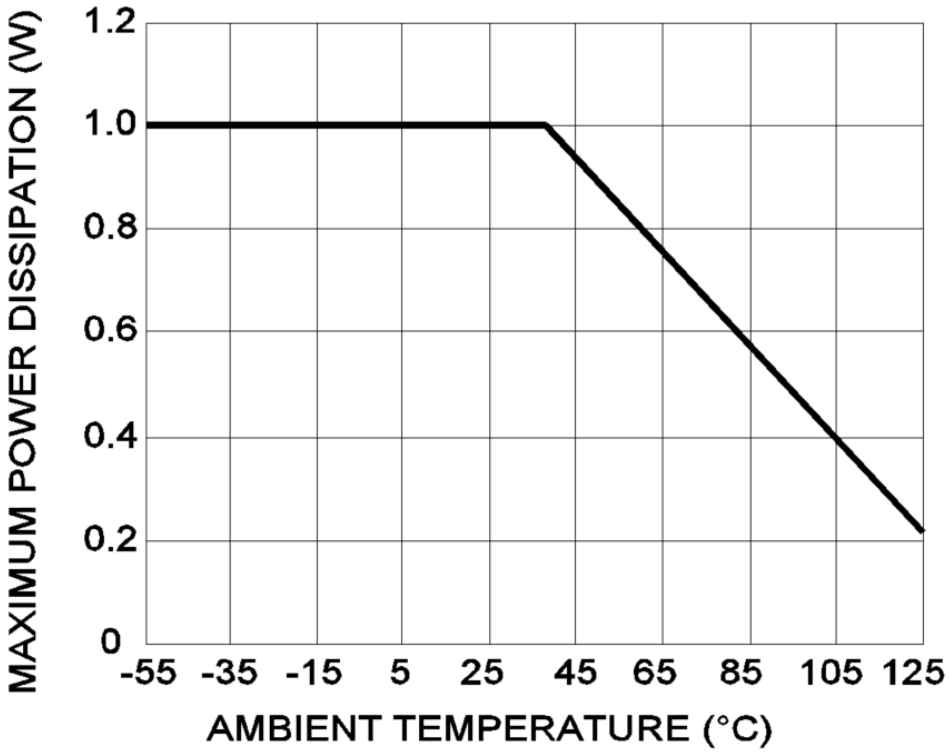


FIGURE 5. Maximum power dissipation versus ambient temperature.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/18618-01XE	24355	Tray, 96 units	ADG1436TRUZ-EP
		Reel, 1000 units	ADG1436TRUZ-EPR7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123