REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

Original date of drawing
YY-MM-DD

18-10-11

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

TITLE

MICROCIRCUIT, DIGITAL-LINEAR, 8-CHANNEL DAS WITH 16 BIT, BIPOLAR INPUT, SIMULTANEOUS SAMPLING ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/18611**

REV

PAGE 1 **OF** 25

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V101-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8 channel data acquisition systems (DAS) with 16 bit, bipolar input, simultaneous sampling analog to digital converter (ADC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/18611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7606-EP	8 channel DAS with 16 bit, bipolar input, simultaneous sampling ADC

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	MS-026-BCD	Low profile quad flat package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

AV_{CC} to AGND	-0.3 V to +7 V
V_{DRIVE} to AGND	-0.3 V to AV_{CC} + 0.3 V
Analog input voltage to AGND	±16.5 V 2/
Digital input voltage to AGND	-0.3 V to V_{DRIVE} + 0.3 V
Digital output voltage to AGND	-0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	-0.3 V to AV_{CC} + 0.3 V
Input current to any pin except supplies	±10 mA 2/
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (TJ)	150°C
Soldering reflow temperature	+260 (0)°C
Thermal resistance, junction to ambient (θ_{JC})	11°C/W 3/
Thermal resistance, junction to ambient (θ_{JA})	45°C/W 3/
Electrostatic discharge (ESD):	
All pins except analog inputs	2 kV
Analog input pins only	7 kV

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.
3/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Analog input current versus input voltage for various temperatures graph. The Analog input current versus input voltage for various temperatures graph shall be as shown in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figures 5 and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance		Unless otherwise specified, input frequency (f_{IN}) = 1 kHz sine wave					
Signal top noise 3/ ratio	SNR	Oversampling by 16, ±10 V range, f_{IN} = 130 Hz	-55°C to +125°C	01	95.5 typical		dB
					93		
		Oversampling by 16, ±5 V range, f_{IN} = 130 Hz			94.5 typical		
					92		
		No sampling, ±10 V range			90 typical		
					87.5		
		No sampling, ±5 V range			89 typical		
					86.5		
Signal to (noise + distortion) (SINAD)		No sampling, ±10 V range	-55°C to +125°C	01	90 typical		dB
					87		
		No sampling, ±5 V range			89 typical		
					86		
Dynamic range		No sampling, ±10 V range	-55°C to +125°C	01	90.5 typical		dB
		No sampling, ±5 V range			90 typical		
Total harmonic distortion	THD		-55°C to +125°C	01	-107 typical		dB
						-93	
Peak harmonic or spurious noise	SFDR		-55°C to +125°C	01	-108 typical		dB
Intermodulation distortion, second order terms	IMD		-55°C to +125°C	01	-110 typical		dB
Intermodulation distortion, third order terms	IMD		-55°C to +125°C	01	-106 typical		dB
Channel to channel isolation		f_{IN} on unselected channels up to 160 kHz	-55°C to +125°C	01	-95 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Analog input filter							
Full power bandwidth	FPBW	-3 dB, ±10 V range	-55°C to +125°C	01	23 typical		kHz
		-3 dB, ±5 V range			15 typical		
		-0.1 dB, ±10 V range			10 typical		
		-0.1 dB, ±5 V range			5 typical		
Group delay time	$t_{GROUP\ DELAY}$	±10 V range	-55°C to +125°C	01	11 typical		µs
		±5 V range			15 typical		
DC accuracy							
Resolution		No missing codes	-55°C to +125°C	01	16		Bits
Differential nonlinearity			-55°C to +125°C	01	±0.5 typical		LSB 4/
						±0.99	
Integral nonlinearity			-55°C to +125°C	01	±0.5 typical		LSB 4/
						±2	
Total unadjusted error	TUE	±10 V range	-55°C to +125°C	01	±6 typical		LSB 4/
		±5 V range			±12 typical		
Positive full scale 5/ error		External reference	-55°C to +125°C	01	±8 typical		LSB 4/
						±34	
		Internal reference			±8 typical		
Positive full scale error drift		External reference	-55°C to +125°C	01	±2 typical		ppm/°C
		Internal reference			±7 typical		
Positive full scale error matching		±10 V range	-55°C to +125°C	01	5 typical		LSB 4/
						32	
		±5 V range			16 typical		
						40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC accuracy – continued.							
Bipolar zero code 6/ error		±10 V range	-55°C to +125°C	01	±1 typical		LSB 4/
						±8	
		±5 V range			±3 typical		
						±14	
Bipolar zero code error drift		±10 V range	-55°C to +125°C	01	10 typical		°C/µV
		±5 V range			5 typical		
Bipolar zero code 6/ error matching		±10 V range	-55°C to +125°C	01	1 typical		LSB 4/
						8	
		±5 V range			6 typical		
						22	
Negative full scale 5/ error		External reference	-55°C to +125°C	01	±8 typical		LSB 4/
						±34	
		Internal reference			±8 typical		
Negative full scale error drift		External reference	-55°C to +125°C	01	±4 typical		ppm/°C
		Internal reference			±8 typical		
Negative full scale error matching		±10 V range	-55°C to +125°C	01	5 typical		LSB 4/
						32	
		±5 V range			16 typical		
						40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Analog input							
Input voltage ranges		RANGE = 1	-55°C to +125°C	01		±10	V
		RANGE = 0				±5	
Analog input current		10 V, see figure 4	-55°C to +125°C	01	5.4 typical		µA
		5 V, see figure 4			2.5 typical		
Input capacitance 7/			-55°C to +125°C	01	5 typical		pF
Input impedance			-55°C to +125°C	01	1 typical		MΩ
Reference input and output							
Reference input voltage range			-55°C to +125°C	01	2.5 typical		V
					2.475	2.525	
DC leakage current			-55°C to +125°C	01		±1	µA
Input capacitance 7/		REF SELECT = 1	-55°C to +125°C	01	7.5 typical		pF
Reference output voltage		REFIN	-55°C to +125°C	01	2.49 typical		V
		REFOUT			2.505 typical		
Reference temperature coefficient			-55°C to +125°C	01	±15 typical		ppm/°C
Logic inputs							
Input high voltage	V_{INH}		-55°C to +125°C	01	0.7 x V_{DRIVE}		V
Input low voltage	V_{INL}		-55°C to +125°C	01		0.3 x V_{DRIVE}	V
Input current	I_{IN}		-55°C to +125°C	01		±2	µA
Input capacitance 7/			-55°C to +125°C	01	5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic outputs							
Output high voltage	V_{OH}	Source current (I_{SOURCE}) = 100 μA	-55°C to +125°C	01	V_{DRIVE} – 0.2		V
Output low voltage	V_{OL}	Sink current (I_{SINK}) = 100 μA	-55°C to +125°C	01		0.2	V
Floating state leakage current			-55°C to +125°C	01	±1 typical		μA
						±20	
Floating state 7/ output capacitance			-55°C to +125°C	01	5 typical		pF
Output coding			-55°C to +125°C	01	Twos complement		
Conversion rate							
Conversion time		All eight channels included, see timing specifications	-55°C to +125°C	01	4.5 typical		μs
Track and hold acquisition time			-55°C to +125°C	01	1.5 typical		μs
Throughput rate		Per channel, all eight channels included	-55°C to +125°C	01		150	kSPS
Power requirements							
Analog supply voltage	AV_{CC}		-55°C to +125°C	01	4.75	5.25	V
Low power supply input	V_{DRIVE}		-55°C to +125°C	01	2.3	5.25	V
Total current,	I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}	-55°C to +125°C	01	16 typical		mA
Normal mode (static)						22	
Total current, 8/	I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE},	-55°C to +125°C	01	20 typical		mA
Normal mode (operational)		f_{SAMPLE} = 150 kSPS				27	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements –continued.							
Total current, Standby mode	I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}	-55°C to +125°C	01	5 typical		mA
						8	
Total current, Shutdown mode	I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}	-55°C to +125°C	01	2 typical		μA
						7	
Power dissipation, Normal mode (static)			-55°C to +125°C	01	80 typical		mW
						115.5	
Power dissipation, 8/ Normal mode (operational)		f_{SAMPLE} = 150 kSPS	-55°C to +125°C	01	100 typical		mW
						142	
Power dissipation, Standby mode			-55°C to +125°C	01	25 typical		mW
						42	
Power dissipation, Shutdown mode			-55°C to +125°C	01	10 typical		μW
						36.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification.		See figures 5 and 6					
Parallel/serial/byte mode.		0.1 x V_{DRIVE} and 0.9 x V_{DRIVE}, logic input levels					
Cycle time	t_{CYCLE}	1/throughout, Parallel mode, reading during or after conversion; or serial mode: V_{DRIVE} = 3.3 V to 5.25 V, reading during a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines	-55°C to +125°C	01		6.65	µs
		Serial mode reading after a conversion; V_{DRIVE} = 2.3 V, $D_{OUT}A$ and $D_{OUT}B$ lines				11.4	
Conversion time	t_{CONV}	Oversampling off	-55°C to +125°C	01	4.5 typical		µs
					4.1	5	
		Oversampling by 2			9.6	11.7	
		Oversampling by 4			20.5	25	
		Oversampling by 8			42	52	
		Oversampling by 16			86	105	
		Oversampling by 32			173	212	
		Oversampling by 64			347	424	
Reset time	t_{RESET}	RESET high pulse width	-55°C to +125°C	01	50		ns
CONVST x high to BUSY high	t1		-55°C to +125°C	01		40	ns
Minimum CONVST x low pulse	t2		-55°C to +125°C	01	25		ns
Minimum CONVST x high pulse	t3		-55°C to +125°C	01	25		ns
BUSY falling edge to $\overline{CS}$ falling edge setup time	t4		-55°C to +125°C	01	0		ns
Maximum delay allowed between CONVST A, CONVST B rising edges	t5 10/		-55°C to +125°C	01		0.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification.		See figures 5 and 6					
Parallel/serial/byte mode- continued. 0.1 x V_{DRIVE} and 0.9 x V_{DRIVE}, logic input levels							
Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge	t6		-55°C to +125°C	01		25	ns
Minimum delay between RESET low to CONVST x high	t7		-55°C to +125°C	01	25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification.		See figures 5 and 6					
Parallel/serial/byte mode.		0.3 x V_{DRIVE} and 0.7 x V_{DRIVE}, logic input levels					
Cycle time	t_{CYCLE}	1/throughout, Parallel mode, reading during or after conversion; or serial mode: V_{DRIVE} = 3.3 V to 5.25 V, reading during a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines	-55°C to +125°C	01		6.65	µs
		Serial mode reading after a conversion; V_{DRIVE} = 2.7 V				11.1	
		Serial mode reading after a conversion; V_{DRIVE} = 2.3 V, $D_{OUT}A$ and $D_{OUT}B$ lines				12.4	
Conversion time	t_{CONV}	Oversampling off	-55°C to +125°C	01	4.5 typical		µs
					4.1	5	
		Oversampling by 2			9.6	11.7	
		Oversampling by 4			20.5	25	
		Oversampling by 8			42	52	
		Oversampling by 16			86	105	
		Oversampling by 32			173	212	
		Oversampling by 64			347	424	
Reset time	t_{RESET}	RESET high pulse width	-55°C to +125°C	01	50		ns
CONVST x high to BUSY high	t1		-55°C to +125°C	01		45	ns
Minimum CONVST x low pulse	t2		-55°C to +125°C	01	25		ns
Minimum CONVST x high pulse	t3		-55°C to +125°C	01	25		ns
BUSY falling edge to $\overline{CS}$ falling edge setup time	t4		-55°C to +125°C	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 10/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification - continued. See figures 5 and 6							
Parallel/serial/byte mode – continued. 0.3 x V_{DRIVE} and 0.7 x V_{DRIVE}, logic input levels							
Maximum delay allowed between CONVST A, CONVST B rising edges	t5 10/		-55°C to +125°C	01		0.5	ns
Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge	t6		-55°C to +125°C	01		25	ns
Minimum delay between RESET low to CONVST x high	t7		-55°C to +125°C	01	25		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, reference voltage (V_{REF}) = 2.5 V external/internal, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, sampling frequency (f_{SAMPLE}) = 150 kSPS, and T_A = -55°C to +125°C.

3/ This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with V_{DRIVE} = 5 V, single to noise ratio (SNR) typically reduces by 1.5 dB and total harmonic distortion (THD) by 3 dB.

4/ LSB means least significant bit. With ±5 V input range, 1 LSB = 152.58 µV. With ±10 V input range, 1 LSB = 305.175 µV.

5/ These specifications include the full temperature range variation and contribution from the internal reference buffer but, do not include the error contribution from the external reference.

6/ Bipolar zero code error is calculated with respect to the analog input voltage.

7/ Sample tested during initial release to ensure compliance.

8/ Operational power and current figure includes contribution when running in oversampling mode.

9/ Unless otherwise specified, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference and internal reference. Sample tested during initial release to ensure compliance. All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.

10/ The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a < 10 LSB performance matching between channel sets.

Case X

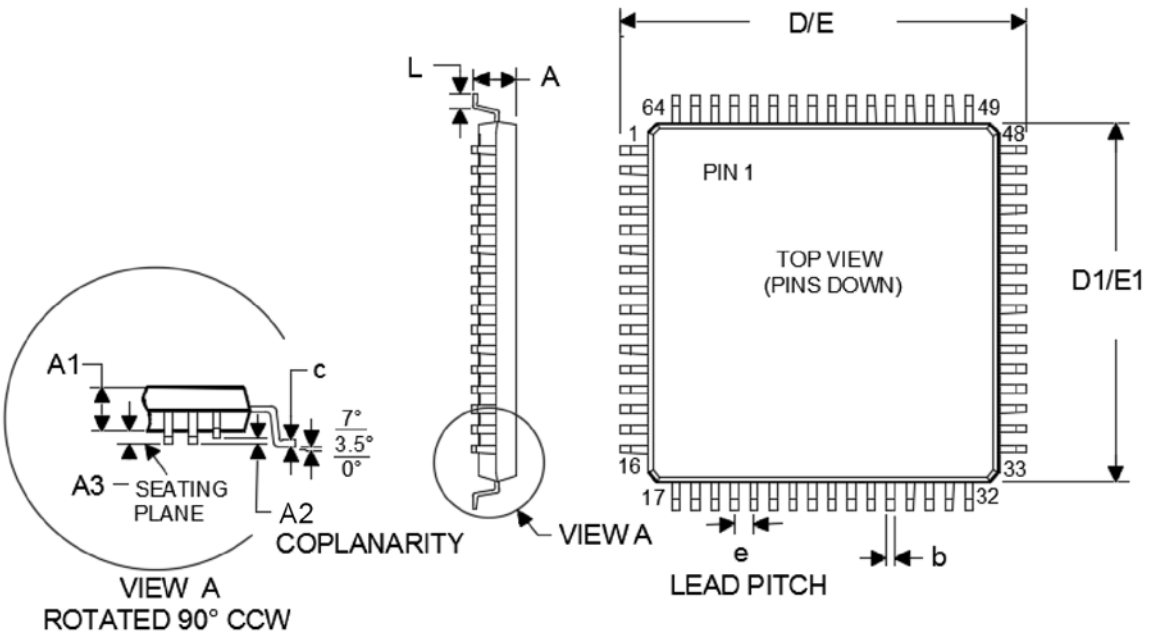


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/18611
		REV	PAGE 15

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.0629	---	---	1.60
A1	.0531	.0551	.0570	1.35	1.40	1.45
A2	.0031 COPLANARITY			0.08 COPLANARITY		
A3	.0019	---	.0059	0.05	---	0.15
b	.0066	.0086	.0106	0.17	0.22	0.27
c	.0035	---	.0078	0.09	---	0.20
D/E	.4656	.4724	.4803	11.80	12.00	12.20
D1/E1	.3858	.3936	.4015	9.80	10.00	10.20
e	.0196 BSC			0.50 BSC		
L	.0177	.0236	.0295	0.45	0.60	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-026-BCD.

FIGURE 1. Case outline - Continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AVCC	17	DB1	33	DB15/ BYTE SEL	49	V1
2	AGND	18	DB2	34	REF SELECT	50	V1GND
3	OS 0	19	DB3	35	AGND	51	V2
4	OS 1	20	DB4	36	REGCAP	52	V2GND
5	OS 3	21	DB5	37	AVCC	53	V3
6	$\overline{\text{PAR}}$/SER/ BYTE SEL	22	DB6	38	AVCC	54	V3GND
7	$\overline{\text{STBY}}$	23	VDRIVE	39	REGCAP	55	V4
8	RANGE	24	DB7/DOUTA	40	AGND	56	V4GND
9	CONVST A	25	DB8/DOUTB	41	AGND	57	V5
10	CONVST B	26	AGND	42	REFIN/ REFOUT	58	V5GND
11	RESET	27	DB9	43	REFGND	59	V6
12	$\overline{\text{RD}}$/SCLK	28	DB10	44	REFCAPA	60	V6GND
13	$\overline{\text{CS}}$	29	DB11	45	REFCAPB	61	V7
14	BUSY	30	DB12	46	REFGND	62	V7GND
15	FRSTDATA	31	DB13	47	AGND	63	V8
16	DB0	32	DB14/HBEN	48	AVCC	64	V8GND

FIGURE 2. Terminal connections.

Terminal symbol	Type	Description
VCC	Power supply	Analog supply voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these supply pins to AGND.
AGND	Power supply	Analog ground. These pins are the ground reference points for all analog circuitry on the device. Refer all analog input signals and external reference signals to these pins. Connect the six AGND pins to the AGND plane of a system.
OS 0, OS 1, OS 2	Digital input	Oversampling mode pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the most significant bit (MSB) control bit, and OS 0 is the least significant bit (LSB) control bit. See the oversample bit decoding table and digital filter section in the manufacturer's data sheet for more details about the logic states and oversampling mode of operation.
$\overline{\text{PAR}}$/SER/BYTE SEL	Digital input	Parallel/Serial/Byte interface selection input. Logic input. See the interface mode selection table in the manufacturer's data sheet. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. Parallel byte interface mode is selected when this pin is logic high and DB15/BYTE SEL is logic high. In serial mode, the $\overline{\text{RD}}$/SCLK pin functions as the serial clock input. The DB7/DOUTA pin and the DB8/DOUTB pin function as serial data outputs. When the serial interface is selected, tie the DB[15:9] and DB[6:0] pins to ground. In byte mode, DB15, in conjunction with $\overline{\text{PAR}}$/SER/BYTE SEL, is used to select the parallel byte mode of operation. DB14 is used as the HBEN pin. DB[7:0] transfer the 16-bit conversion results in two RD operations, with DB0 as the LSB of the data transfers.
$\overline{\text{STBY}}$	Digital input	Standby mode input. This pin is used to place the device into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin. When in standby mode, all circuitry, except the on-chip reference, regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down. See the power-down mode selection table in the manufacturer's data sheet.
RANGE	Digital input	Analog input range selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended for fast throughput rate applications. See the analog input section in the manufacturer's data sheet for more information

FIGURE 2. Terminal connections.

Terminal symbol	Type	Description
CONVST A, CONVST B	Digital input	Conversion start input A, Conversion start input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together, and a single convert start signal can be applied. Alternatively, CONVST A can be used to initiate simultaneous sampling: V1, V2, V3, and V4 for the device. CONVST B can be used to initiate simultaneous sampling on the other analog inputs: V5, V6, V7, and V8 for the device. This is possible only when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end, track-and-hold circuitry for the respective analog inputs is set to hold.
RESET	Digital input	Reset Input. When set to logic high, the rising edge of RESET resets the device. The device receives a RESET pulse directly after power-up. The RESET high pulse is typically 50 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers rest to all zeros.
$\overline{RD}$/SCLK	Digital input	Parallel data read control input when parallel interface selected ($\overline{RD}$)/serial clock input. When serial interface selected (SCLK). When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the DOUTA and DOUTB data output lines output lines out of the tree state and clocks out of the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the DOUTA and DOUTB serial data outputs. See the control section in the manufacturer's data sheet for more information.
$\overline{CS}$	Digital input	Chip select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the DB[15:0] output bus is enabled, and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
BUSY	Digital output	Busy output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read after t_4. Any data read while BUSY is high must be completed before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high
FRSTDATA	Digital output	Digital output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel, byte, or serial interface. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{RD}$ corresponding to the result of V1 then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{RD}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{CS}$ because this pin clocks out the MSB of V1 on DOUTA. FRSTDATA returns low on the 16th SCLK falling edge after the $\overline{CS}$ falling edge. See the conversion control section in the manufacturer's data sheet for more information

FIGURE 2. Terminal connections - continued.

Terminal symbol	Type	Description
DB[6:0]	Digital output	Parallel output data bits, DB6 to DB0. When $\overline{\text{PAR}}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input and output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB6 to DB0 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1, tie these pins to AGND. When operating in parallel byte interface mode, DB[7:0] outputs the 16-bit conversion result in two $\overline{\text{RD}}$ operations. DB7 (pin 24) is the MSB and DB0 is the LSB. See pin 24 description for additional information.
VDRIVE	Power supply	Logic power supply input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, digital signal processor and field programmable gate array)
DB7/DOUTA	Digital output	Parallel output data bit 7 (DB7)/Serial interface data output pin (DOUTA). When $\overline{\text{PAR}}$/SER/ BYTE SEL = 0, this pin acts as a three-state parallel digital input and output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1, this pin functions as DOUTA and outputs serial conversion data. When operating in parallel byte mode, DB7 is the MSB of the byte. See the conversion control section in the manufacturer's data sheet for more information.
DB8/DOUTB	Digital output	Parallel output data bit 8 (DB8)/Serial interface data output pin (DOUTB). When $\overline{\text{PAR}}$/SER/ BYTE SEL = 0, this pin acts as a three-state parallel digital input and output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1, this pin functions as DOUTB and outputs serial conversion data. See the conversion control section in the manufacturer's data sheet for more information.
DB[13:9]	Digital output	Parallel output data bits, DB13 to DB9. When $\overline{\text{PAR}}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input and output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1, tie these pins to AGND.
DB14/HBEN	Digital output/ digital input	Parallel output data bit 14 (DB14)/High Byte Enable (HBEN). When $\overline{\text{PAR}}$ SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB14 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the device operates in parallel byte interface mode. In parallel byte mode, the HBEN pin is used to select whether the MSB or the LSB of the conversion result is output first. When HBEN = 1, the MSB is output first, followed by the LSB. When HBEN = 0, the LSB is output first, followed by the MSB. In serial mode, tie this pin to GND.
DB15/BYTE SEL	Digital output/ digital input	Parallel output data bit 15 (DB15)/Parallel Byte Mode Select (BYTE SEL). See the interface mode Selection table in the manufacturer's data sheet. When $\overline{\text{PAR}}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB15 of the conversion result. When $\overline{\text{PAR}}$/SER/BYTE SEL = 1, the BYTE SEL pin is used to select between serial interface mode and parallel byte interface mode. When $\overline{\text{PAR}}$/SER/ BYTE SEL = 1 and DB15/BYTE SEL = 0, the device operates in serial interface mode. When $\overline{\text{PAR}}$/SER/ BYTE SEL = 1 and DB15/BYTE SEL = 1, the device operates in parallel byte interface mode.
REF SELECT	Digital input	Internal/external reference selection input. Logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
REGCAP	Power supply	Decoupling capacitor pin for voltage output from internal regulator. Decouple these output pins separately to AGND using a 1 µF capacitor. The voltage on these pins is in the 2.5 V to 2.7 V range.
REFIN/ REFOUT	Reference	Reference input (REFIN)/reference output (REFOUT). See the internal/external reference section in the manufacturer's data sheet for more information. The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Apply a 10 µF capacitor from this pin to ground close to the REFGND pins.

FIGURE 2. Terminal connections - continued.

Terminal symbol	Type	Description
REFGND	Reference	Reference ground pins. Connect these pins to AGND.
REFCAPA, REFCAPB	Reference	Reference buffer output force and sense pins. Connect these pins together, and decouple these pins to AGND using a low ESR, 10 µF ceramic capacitor. The voltage on these pins is typically 4.5 V.
V1	Analog input	Analog input 1. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V1GND	Analog input ground	Analog input V1 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V2	Analog input	Analog input 2. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V2GND	Analog input ground	Analog input V2 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V3	Analog input	Analog input 3. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V3GND	Analog input ground	Analog input V3 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V4	Analog input	Analog input 4. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V4GND	Analog input ground	Analog input V4 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V5	Analog input	Analog input 5. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V5GND	Analog input ground	Analog input V5 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V6	Analog input	Analog input 6. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V6GND	Analog input ground	Analog input V6 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V7	Analog input	Analog input 7. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V7GND	Analog input ground	Analog input V7 ground pin. Connect all analog input AGND pins to the AGND plane of a system.
V8	Analog input	Analog input 8. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
V8GND	Analog input ground	Analog input V8 ground pin. Connect all analog input AGND pins to the AGND plane of a system.

FIGURE 2. Terminal connections - continued.

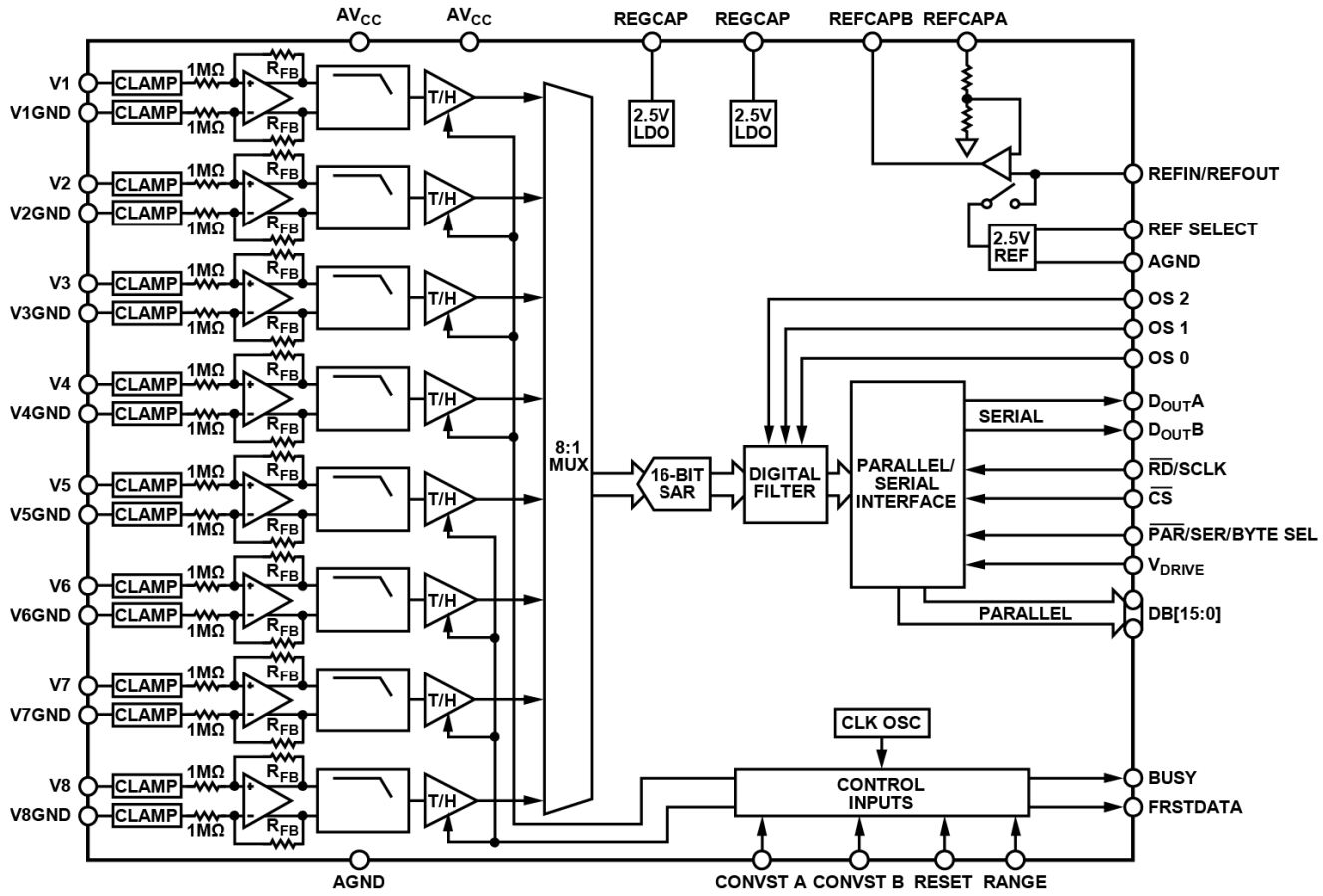


FIGURE 3. Logic diagram.

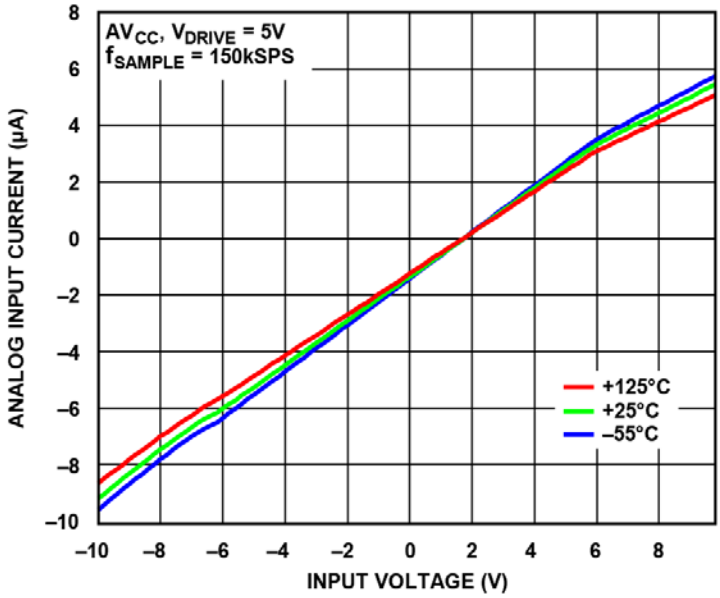


FIGURE 4. Analog input current versus input voltage for various temperatures.

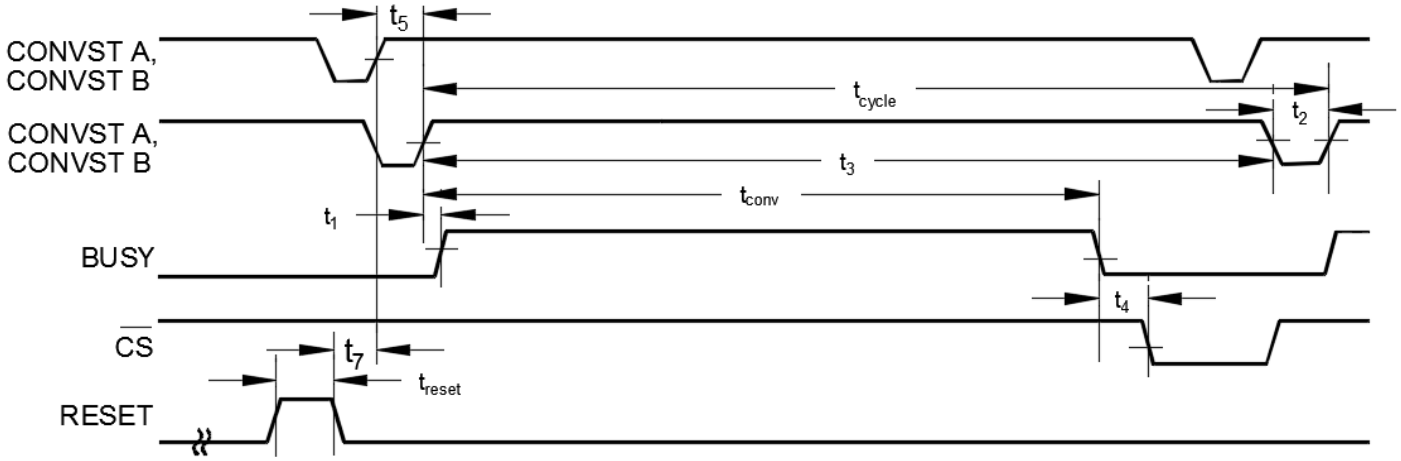
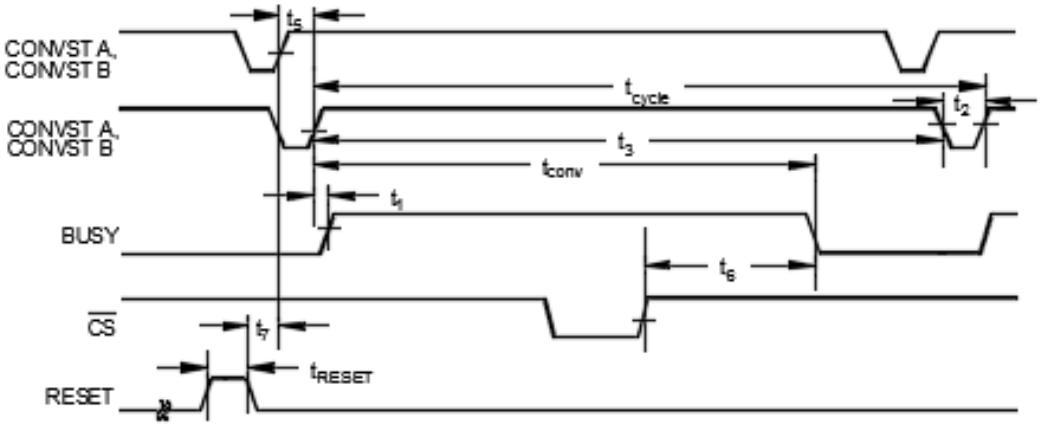


FIGURE 5. CONVST x timing – reading after a conversion.



FIGUIRE 6. CONVST x timing – reading during a convsrsion.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/18611-01XE	24355	Tube, 160 units	AD7606TSTZ-EP
V62/18611-01XE	24355	Reel, 1500 units	AD7606TSTZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland